Progress of the AIDA-2020 Trigger Logic Unit (TLU)

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

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Introduction

- During beam-test frequently want to:
  - synchronize a detector under test (DUT) with external signals
    - E.g. scintillators to trigger on beam particles
    - Cherenkov detectors (for PID)
    - Accelerator (e.g. Spill signals, max-energy)
  - Synchronize with other detectors
    - E.g. With beam-telescope

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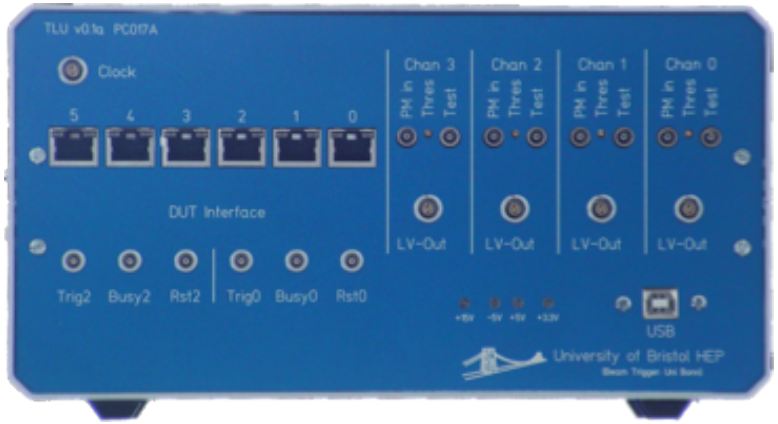
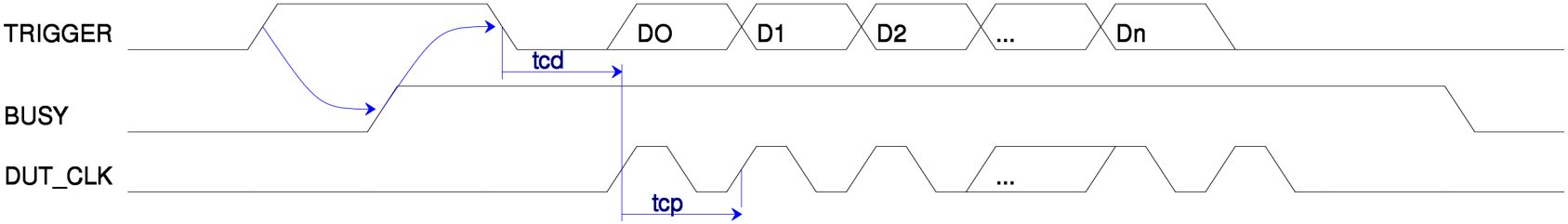
EUDET TLU

- Originally designed for use with beam-telescope with low beam rate
- Handshake designed to allow independent clocks
  - (Optional) transfer trigger number from TLU → DUT





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AIDA-2020 TLU

- Originally ILC users. Designed round “rolling shutter” MAPS pixel sensors (Mimosa family).
  - Trigger rate of EUDET system limited by frame readout to ~ 5kHz
    - → increasing use of beam telescopes by LHC detectors. Want higher trigger rate
  - No common clock → Difficult to interface to self-triggering detectors
    - E.g. some calorimeters.
  - FPGA inside EUDET TLU becoming obsolete.
- →New TLU designed as part of AIDA-2020 project
  - Open hardware, Open firmware (https://www.ohwr.org/projects/fmc-mtlu)

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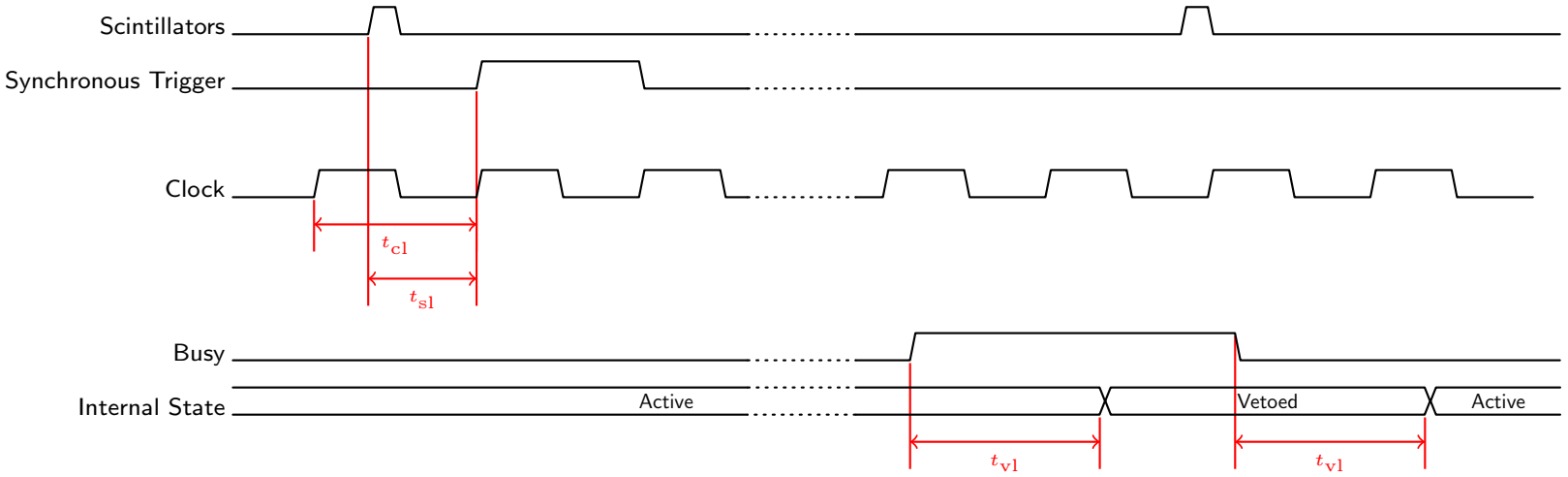
AIDA-2020 TLU

- Uses CoTS FPGA module with FMC (standard) interface
  - Xilinx Artix
- Synchronous interface
  - Clock , trigger , busy , sync
- … but can be backward compatible with EUDET TLU



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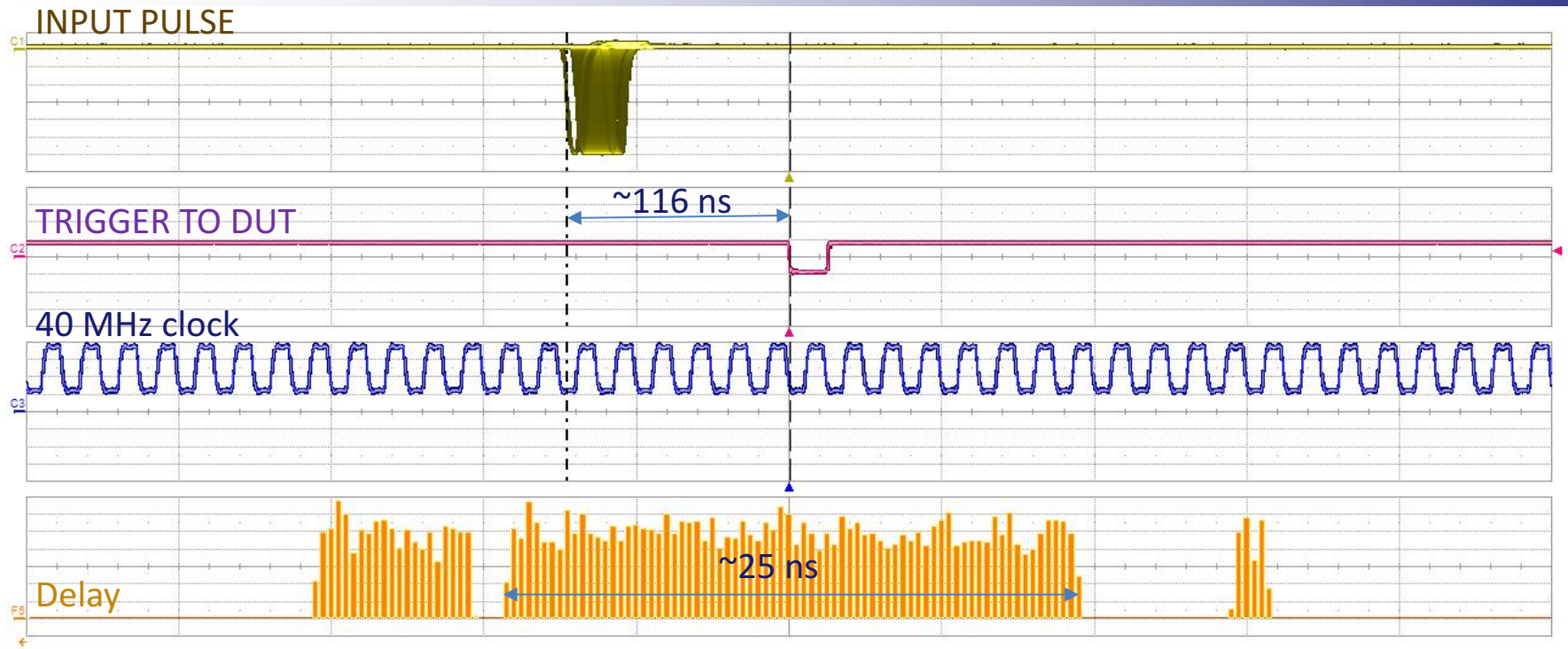
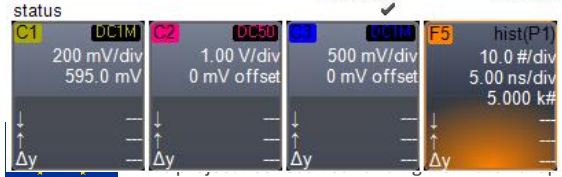
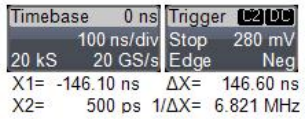
Synchronous Interface

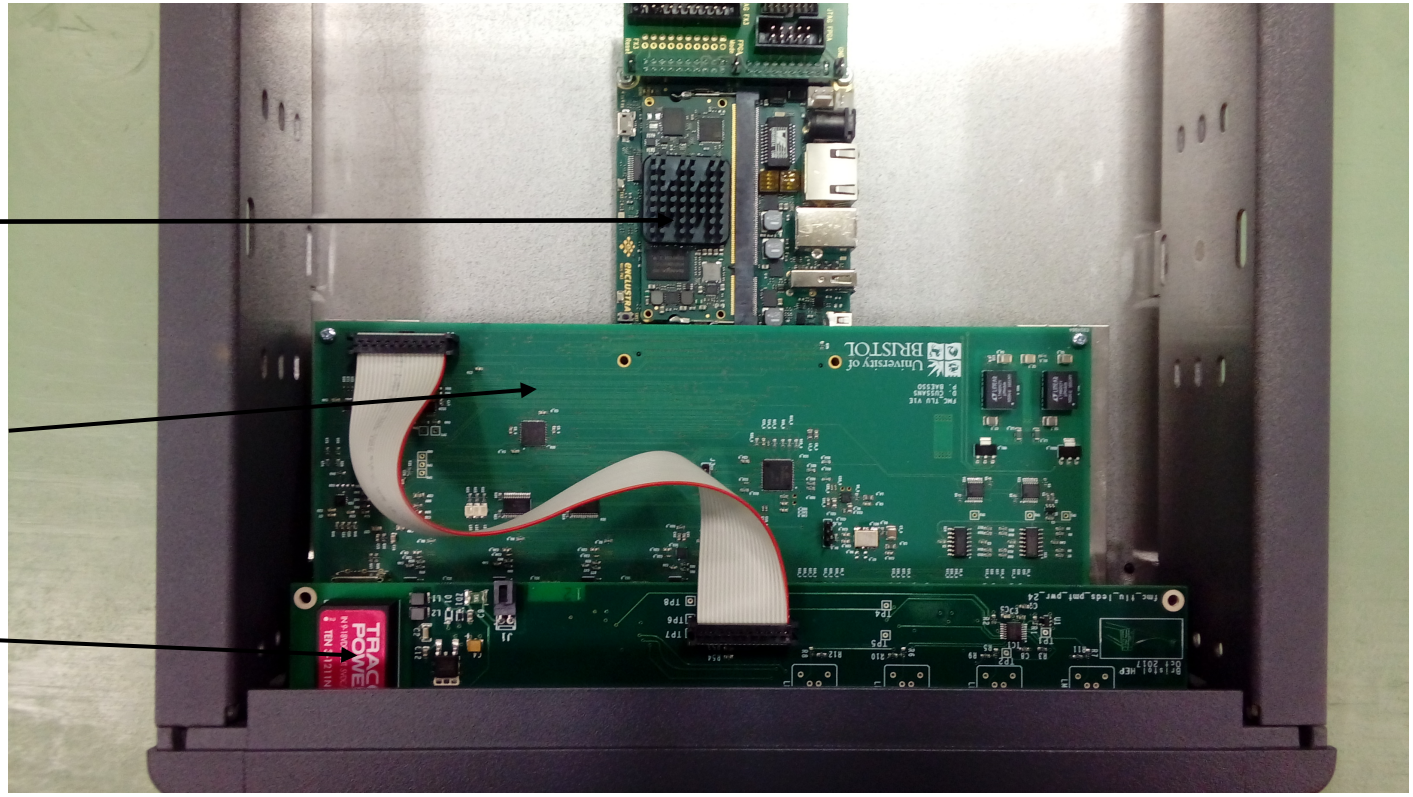


Measure	P1:dt@lv(C1,C2)	P2:freq(C4)	P3:- - -	P4:- - -	P5:freq(C4)	P6:- - -	P7:- - -	P8:- - -
value	135.0389 ns	39.6383 MHz						
mean	128.499 ns	40.0063 MHz						
min	114.7949 ns	38.8166 MHz						
max	146.1616 ns	41.2087 MHz						
sdev	7.984 ns	271.6 kHz						
num	14.050e+3	607.737e+3						
status	✔	⚠						





TLU Assembly



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AIDA 2020
PMT POWER
1
2
3
4
SFP
1
2
3
4
DUT INTERFACES
CLOCK I/O
1
2
3
4
5
6
TRIGGER INPUTS
POWER
+5 V
-5 V
TRIGGER LOGIC UNIT - v1E

TLU Parameters

- Four Device Under Test (DUT) Interfaces
  - Five LVDS signals on HDMI connectors
    - (chosen to be compatible with CALICE)
    - Converted by passive “dongle” to RJ45 interface used by EUDET TLU
- Six trigger inputs
  - +/- 5V range
  - Adjustable threshold +/- 1.3V
  - Fully configurable trigger “mask”
- Clock input or output
  - Adjustable frequency, typically 40MHz
  - Clock input on either LVDS on 2-pole ”Lemo” or HDMI

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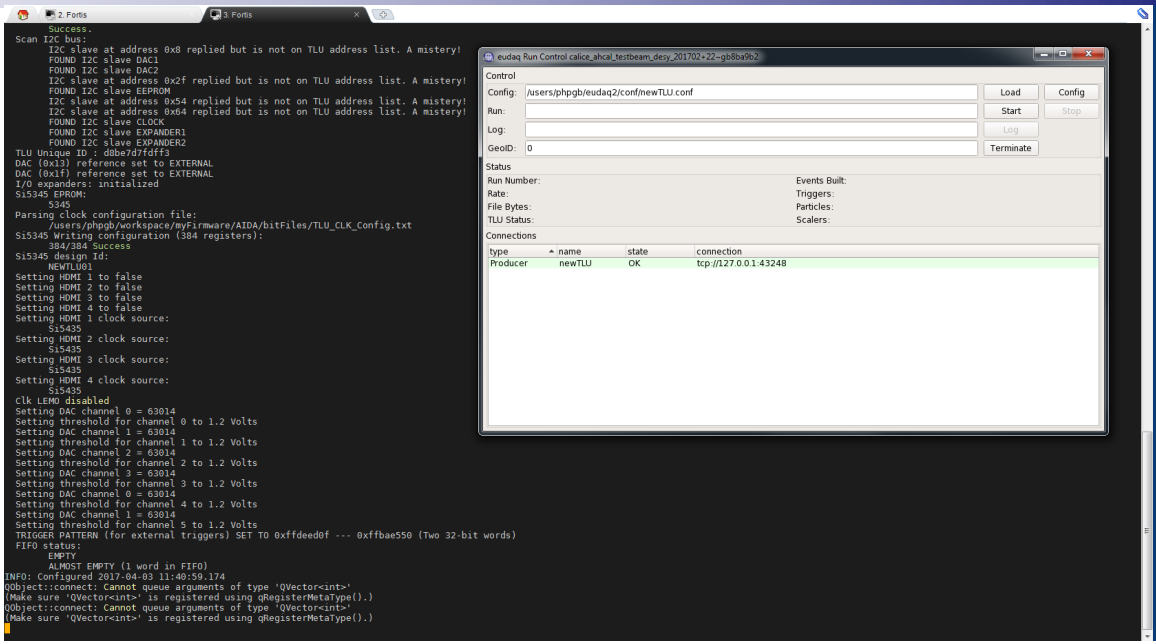
TLU hardware status

- 10 boards produced
- One in CERN, One in DESY (for tests)
  - No indicator LEDS. New board produced with LEDs.
    - LED boards arrived, Testing under way.
- Two TLUs will be delivered to DESY, one to CERN an AIDA-2020 “deliverable”
- Available to other groups at Euro 2.2k each.
  - New batch being produced this month – let me know if you want one ….
- Completed porting of firmware from old to new hardware
  - Maintain all functionality from old TLU
  - Tested new functionality (clock generator, discriminators, trigger)
  - Still need to implement CDR functionality

TLU integration with EUDAQ2



- Integrated with EUDAQ2:
  - Current version of TLU producer stable and working with EUDAQ2
  - Allows to configure the TLU and read data
  - Tested at CERN and DESY
  - Aiming for up to 1MHz average trigger rate
  - Testing/debugging ongoing

Tests

- DESY, October 2017
  - Interfaced AIDA-2020 TLU with Mimosa telescope
    - Used EUDET (trigger/busy/trigger-number) hand-shake
  - Successfully took data with telescope
    - Demonstrated backwards compatibility with EUDET TLU

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Tests

- CERN, PS (East Area) T9, November 2017
  - Interfaced AIDA-2020 TLU with
    - Mimosa telescope (EUDET handshake)
    - FE-I4 fast pixel plane (EUDET handshake)
      - Thanks to Andre Rumler
    - “TORCH” project (AIDA / Synchronous handshake)
      - AIDA/Synchronous handshake
  - Successfully took data with telescope, FE-I4 and TORCH
  - TLUProducer took data
    - Records time-stamp of each trigger issued (25ns)
    - Records fine-grained time-stamp of each trigger input
    - Records which inputs fired (trigger mask may not demand all inputs fire)
      - Some inputs connected to Cherenkov detectors.

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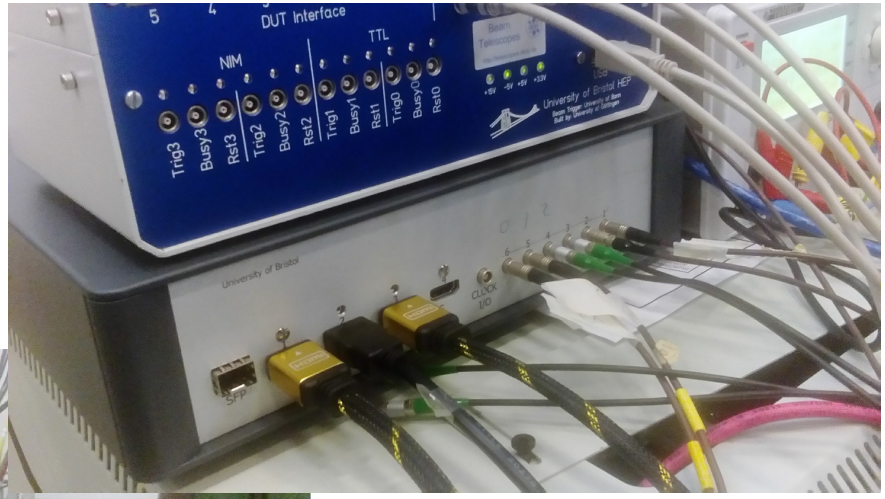
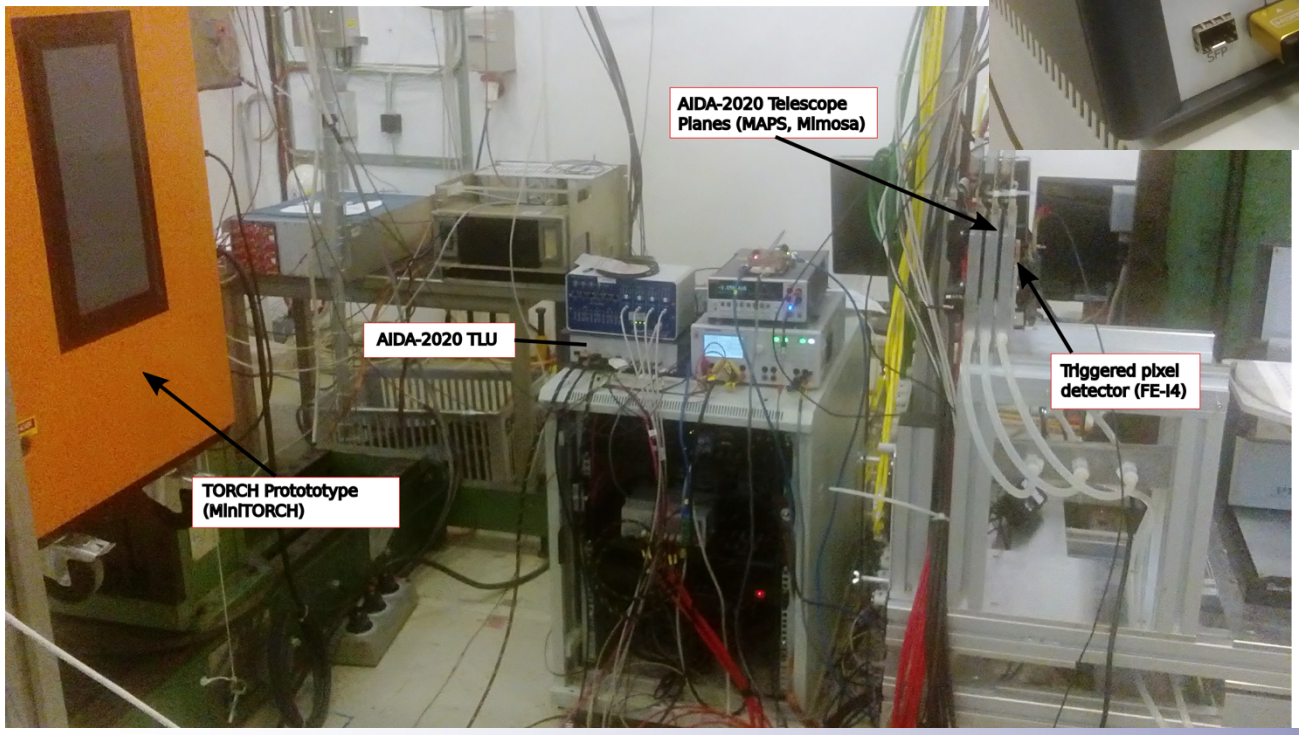
TLU Tests
CERN East Area T9

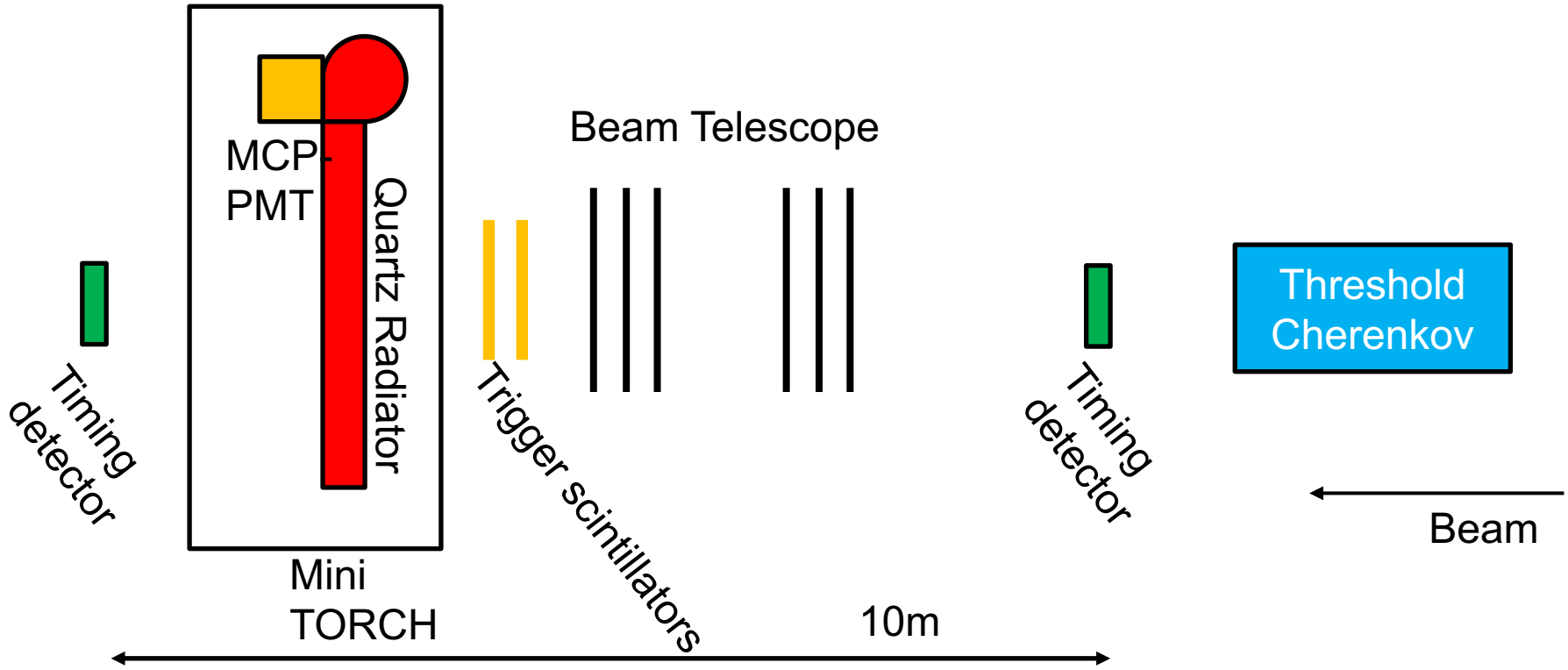




- Used to provide clock and trigger to non-AIDA2020 beam-test readout (TORCH)

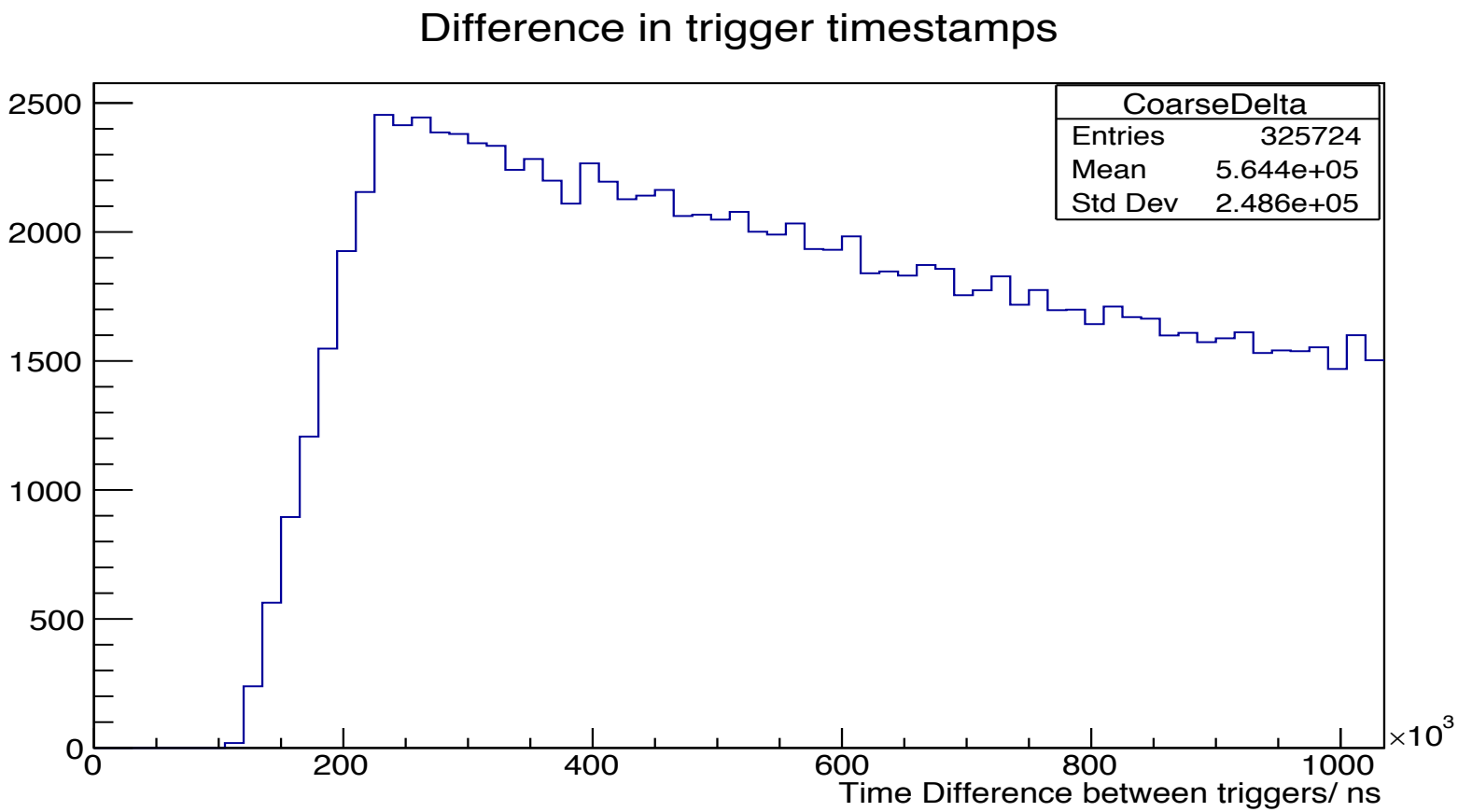
AIDA 2020 AIDA Beam Telescope + TORCH

- TORCH project doing R&D on particle PID by ToF
  - Cherenov light in thin quartz sheet perpendicular to beam
  - Guided by TIR to edges.
  - Read out by pixelated Micro-Channel Plate based PMTs



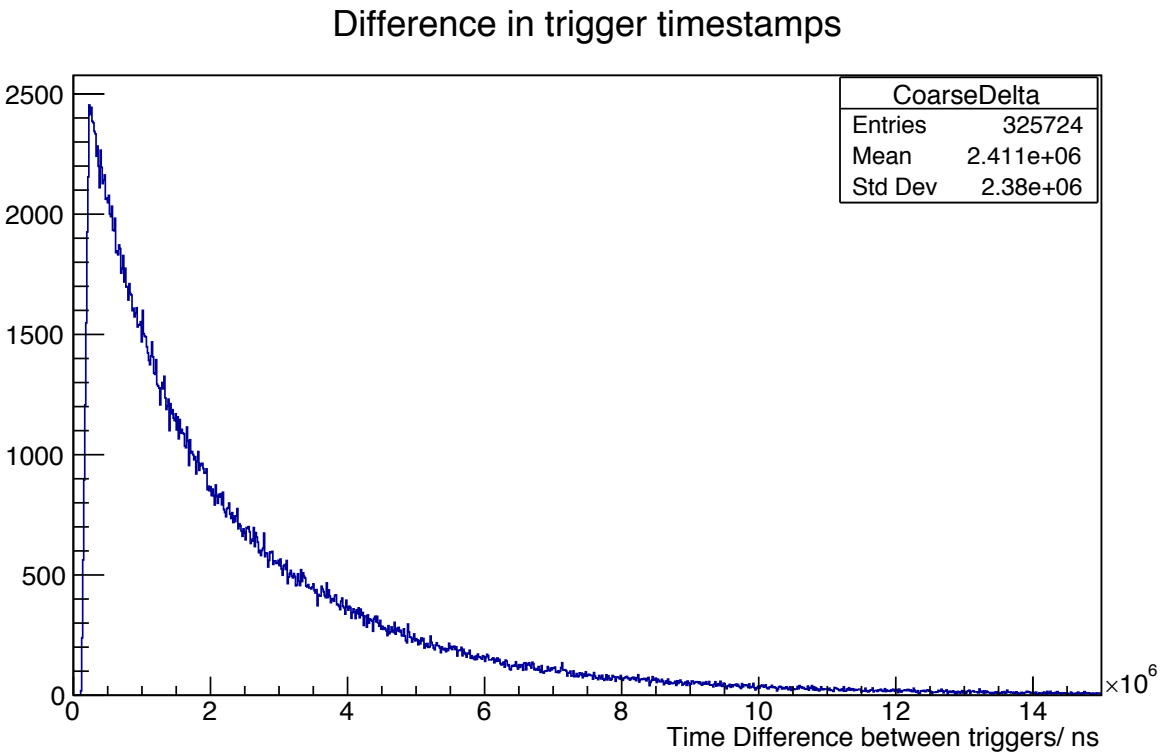
Difference between timestamps

- Mimosa telescope sets busy until two frames read out (minimum time 115μs, max 230μs)



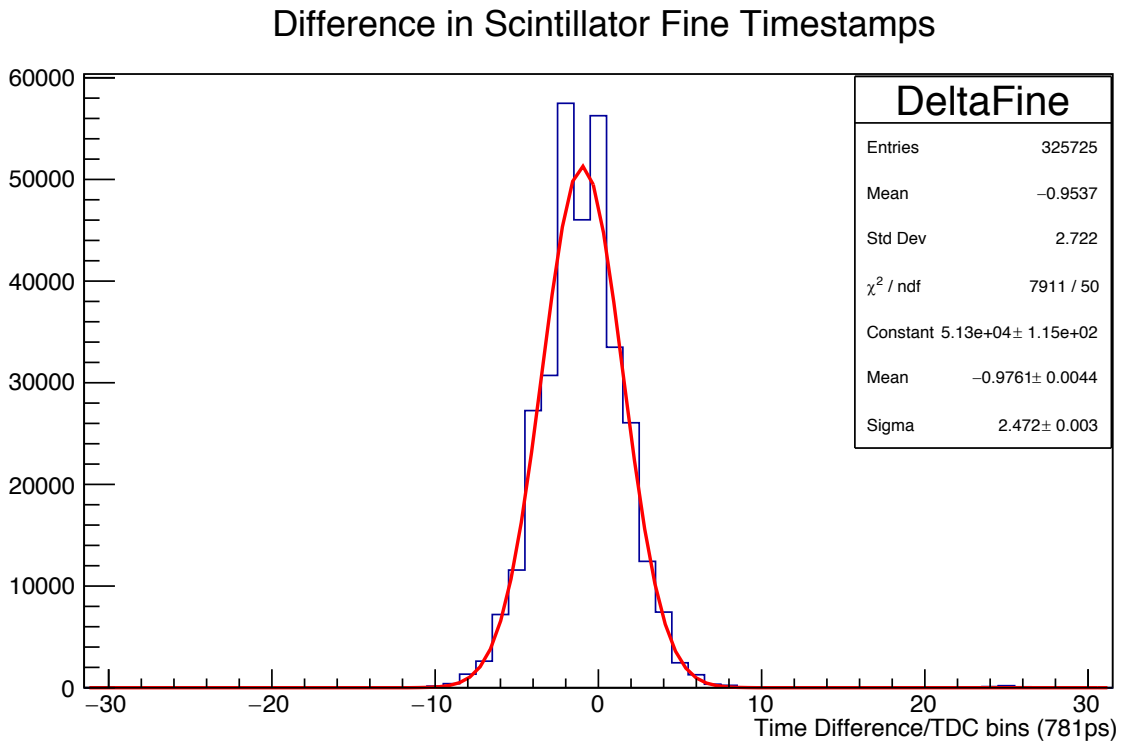
Difference between timestamps

- Telescope scintillators in coincidence with downstream timing detector
- Low trigger-rate
  - Most frames contain a particle, few point to timing detector



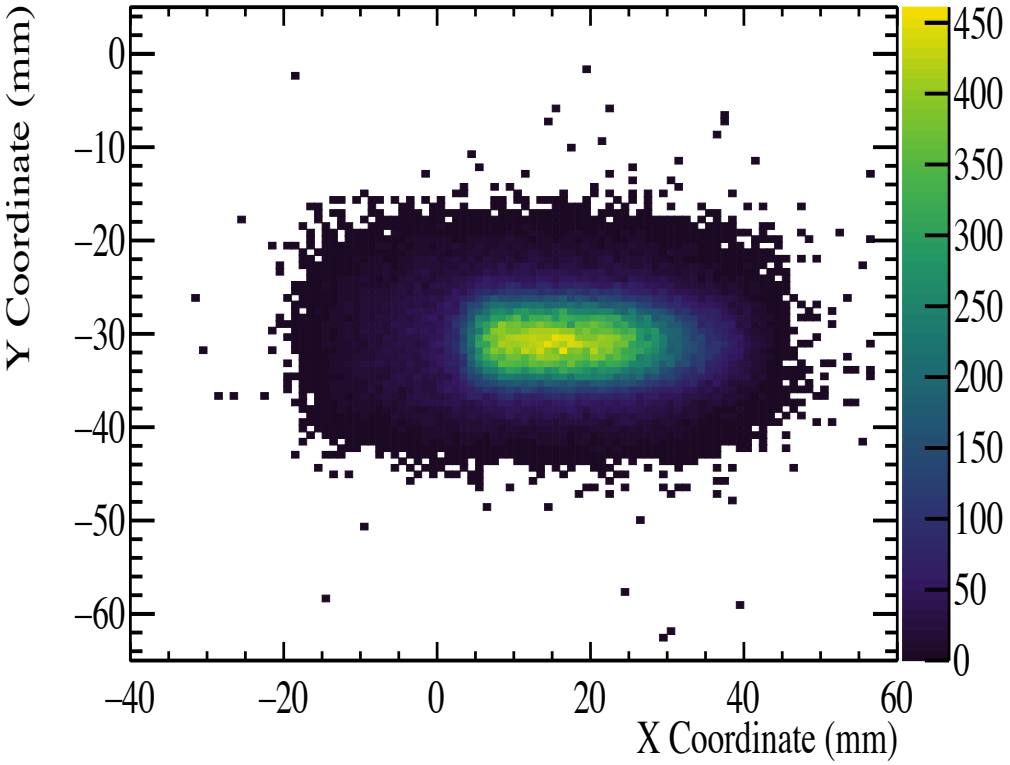
TLU Timing

- TLU time-stamps triggers with 780ps bins
- Take difference between pulses from two trigger scintillators
  - Telescope scintillators, CERN East Area T9
- Precision of single scintillator = 1.5ns



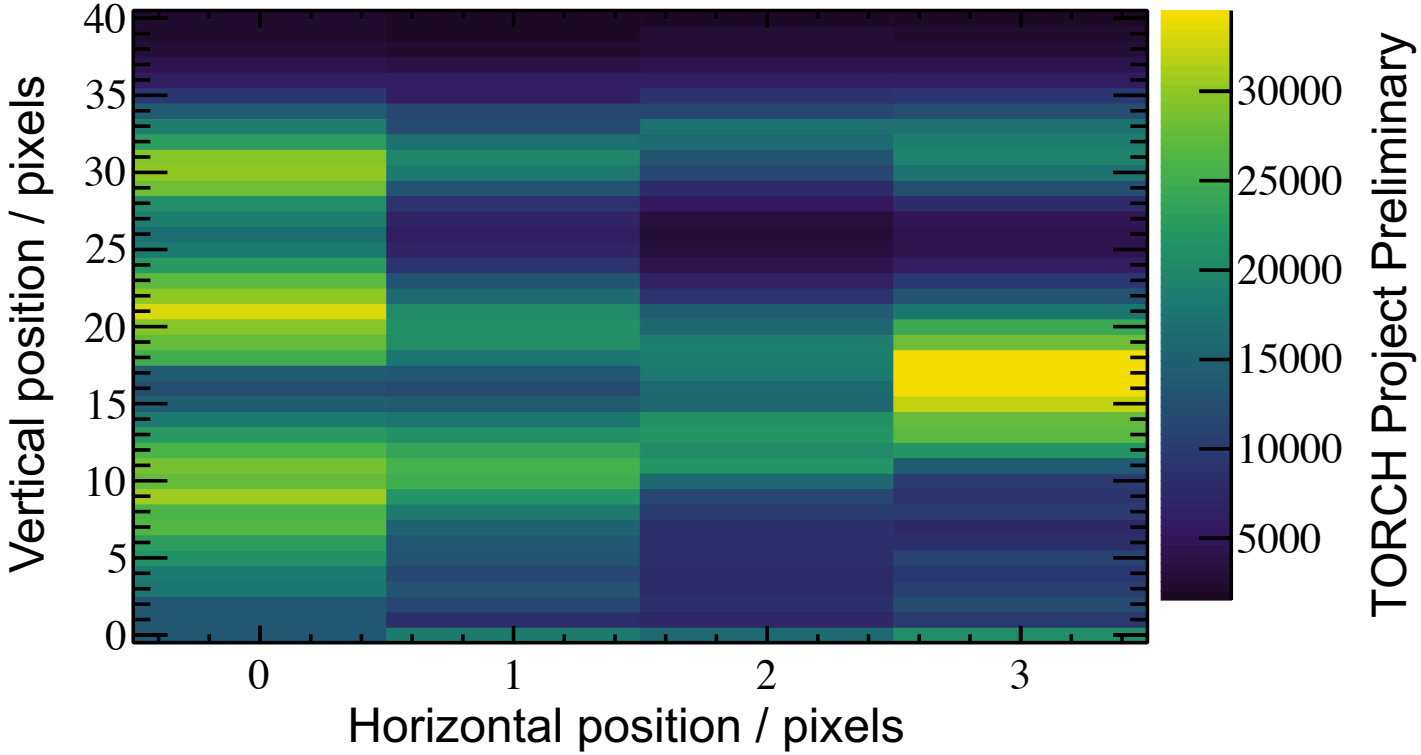
Extrapolated Tracks

- Reconstruct data from Mimosa telescope with EUTelescope
- Select events with only one track
  - Average of ~ 1.5 tracks per event
- Extrapolate from telescope to position of timing detector
- See outline of timing detector
- See talk on East Area



AIDA 2020 TORCH

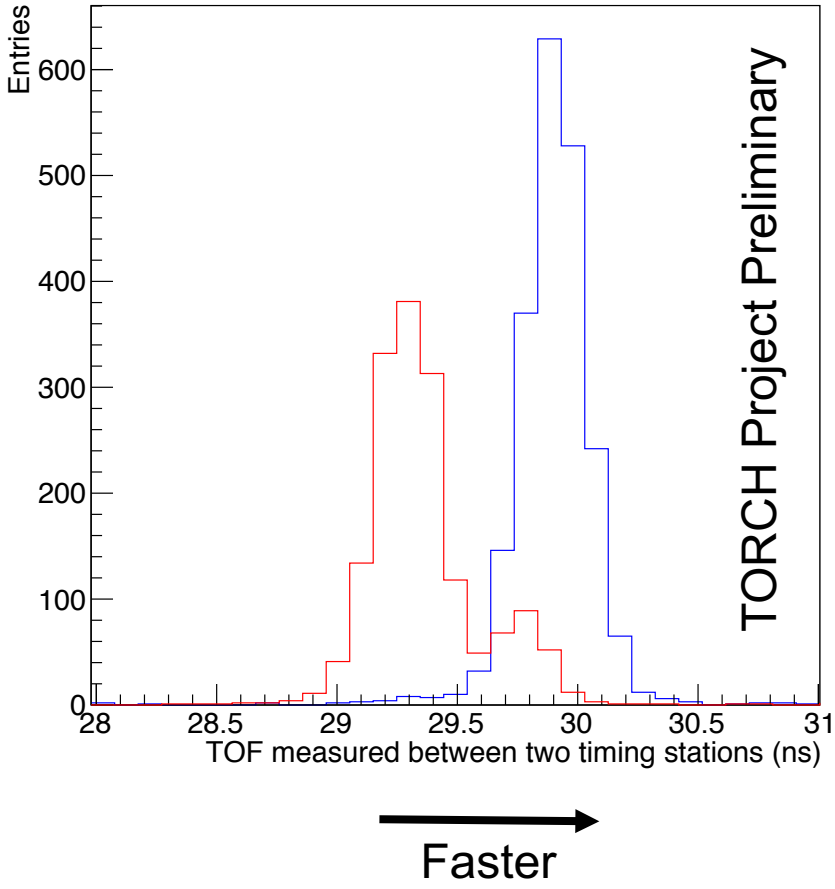
- Cone of Cherenkov photons trapped by TIR, guided to end of quartz sheet and focused on to MCP-PMT
- Projection of cone folded by reflection at edges



AIDA 2020 TORCH

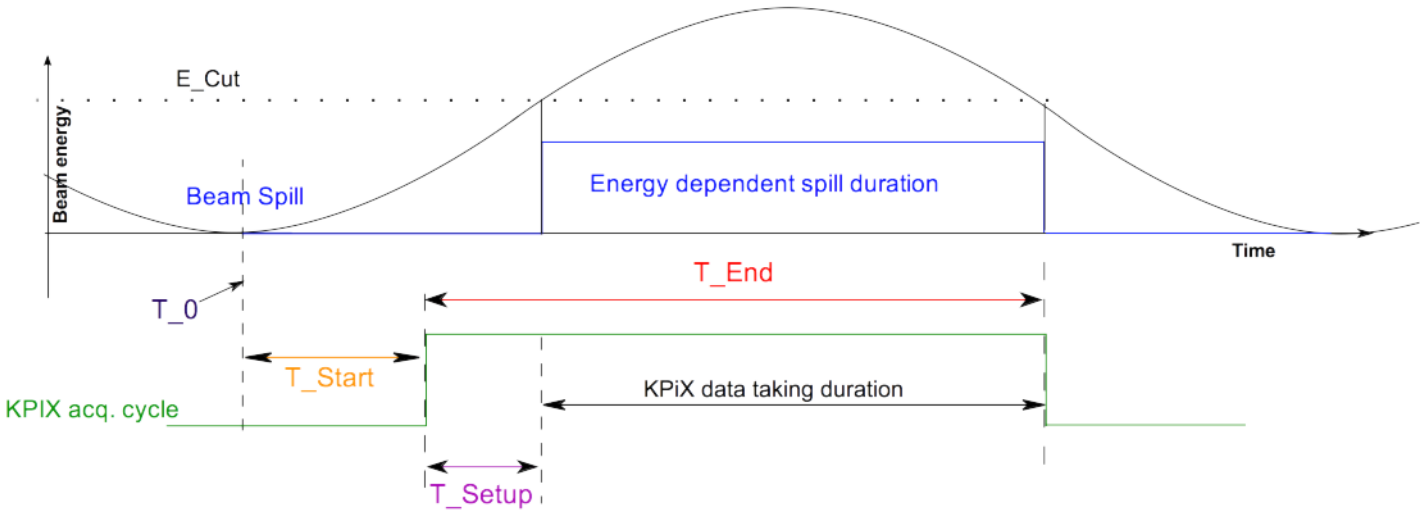
- Aiming to measure single photons with a precision of σ ~ 70ps
  - →Need to know impact point of particle to O(mm)
- For some analysis want to know particle type (p/π)
  - Time of flight measured by small dedicated detectors
  - Threshold Cherenkov detectors in beam
    - Get signal for π , but not for protons
    - Fed into TLU. Tag event by event
  - Compare ToF with/without Chernkov tag:

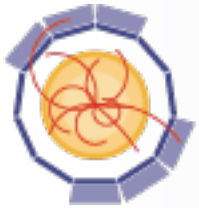
Blue – light in Cherenkov
Red – no light in Cherenkov



Interface to AIDA-2020 Silicon Tracker

- Readout chip designed for ILC
  - → Short active time, then readout
  - More details here
- To reduce dead-time, take data only when particles are present
  - Sinusoidal energy ramp in DESY accelerator.
    - Get particles in beam-line only at peak energy of accelerator





Interface to Accelerator

- Provide a “spill” signal to SiTra
  - Use one of TLU inputs to monitor accelerator signal.
  - Parameters adjustable by setting registers.
  - Could be used at CERN PS/SPS
  - Could be used with Calorimeter readout systems
- Firmware due Feb/March

Beam Telescope: Multiple tracks per frame

- Can configure TLU to ignore BUSY from an DUT with EUDET handshake
  - E.g. Mimosa telescope + FE-4I:
    - Ignore busy from telescope
    - →Can have more than one trigger sent to FE-I4 during frame readout of Mimosa
    - Keep global trigger number (Same trigger number sent out to both Mimosa + FE-I4)
  - Whether DUT BUSY vetoes triggers is configurable.
    - For DUT where BUSY vetoes triggers, read out consecutive trigger numbers
    - For DUT where BUSY does not veto triggers, read out non-consecutive trigger numbers (if >1 particle per frame)
  - Firmware tested in lab
  - Plans to test at DESY
  - Can reconstruct > 10 tracks per Mimosa frame
    - → Can increase trigger rate to > 50 kHz

Summary

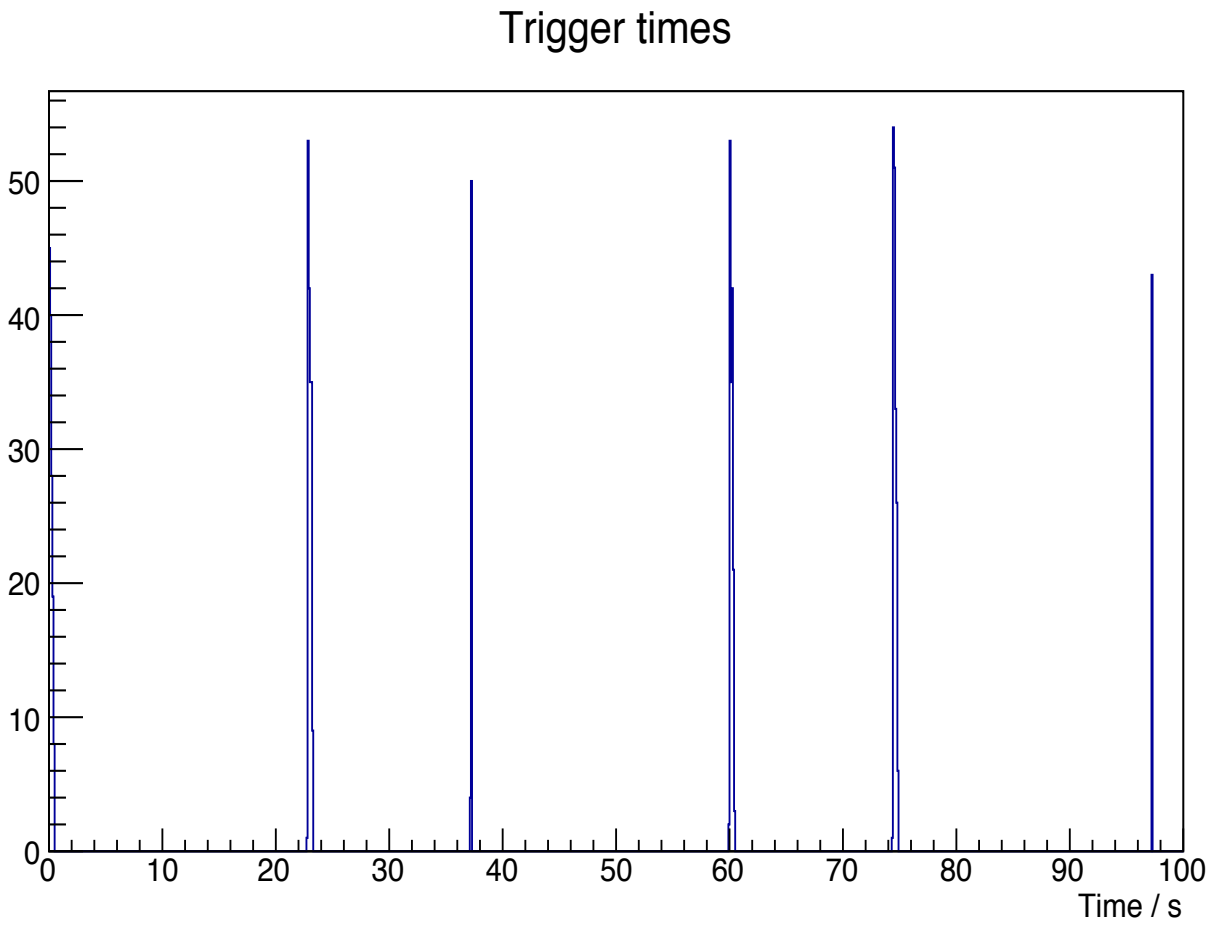
- First batch of “production” AIDA-2020 TLUs being assembled
  - A new batch will be manufactured soon
- Have tested with Mimosa Telescope and FEI-4
- Have tested simultaneous use of trigger/busy(EUDET) and synchronous(AIDA) interface
- Firmware in place to allow multiple triggers per Mimosa telescope frame
  - Tested in lab
  - Plans to test at DESY
  - Plans to test in beam
  - Order of magnitude higher trigger rate from AIDA beam telescopes
- Have tested simultaneous use of trigger/busy(EUDET) and synchronous(AIDA) interface
  - (Mimosa telescope + FE-I4) + TORCH
  - Could use to interface beam telescope with CALICE calorimeter.
- Firmware being written to interface with accelerator
  - Programmable “spill” signal
  - allow interface with AIDA-2020 Silicon tracker.

Backup Slides

Backup Slides

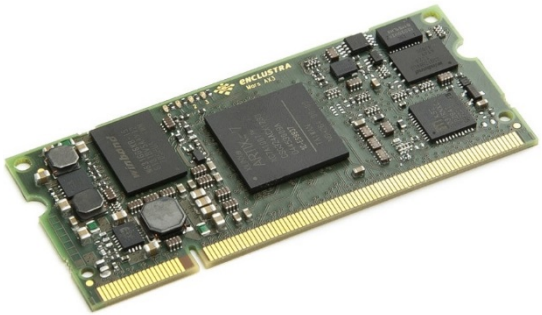
SPS Spill Structure

- Trigger time-stamps of first few spills in a run



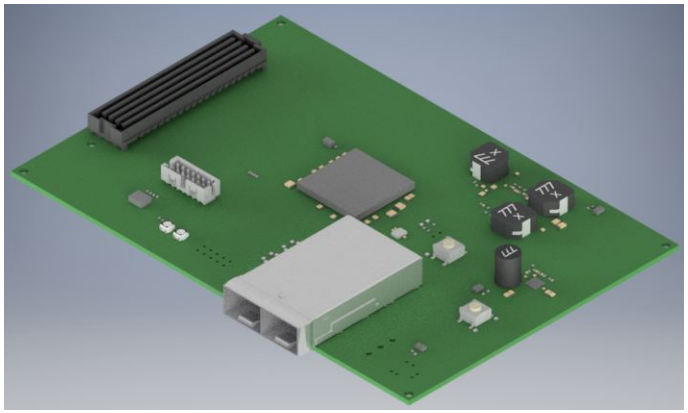
TLU logic

- Transition from FPGA Xilinx Series 6 (miniTLU) to Series 7 (v1C and later)

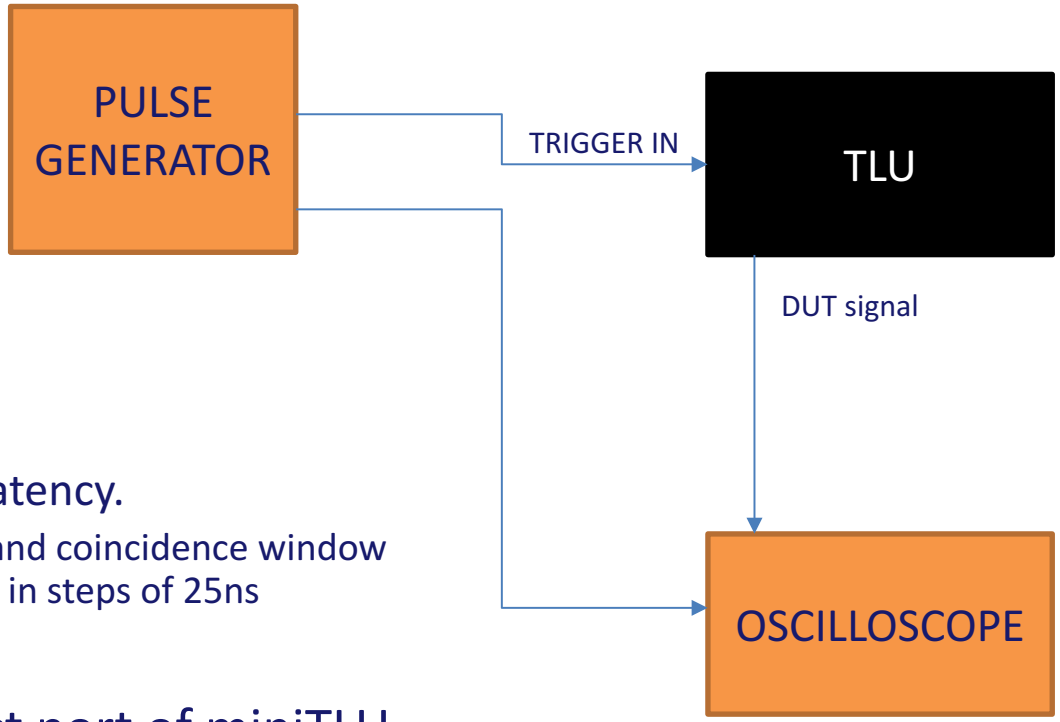


- Currently working on bench with Enclustra AX3 FPGA

- **ARTIX TRIVIAL FMC CARRIER (ATFC)**
  HTTP://WWW.OHWR.ORG/PROJECTS/ATFC
  - Designed by Samer Al-Kilani (UCL)
  - Stand-alone
    - … but design will eventually be be included in TLU
  - Bare PCBs produced
  - Waiting for components,
    - Then assembly of first two at UCL

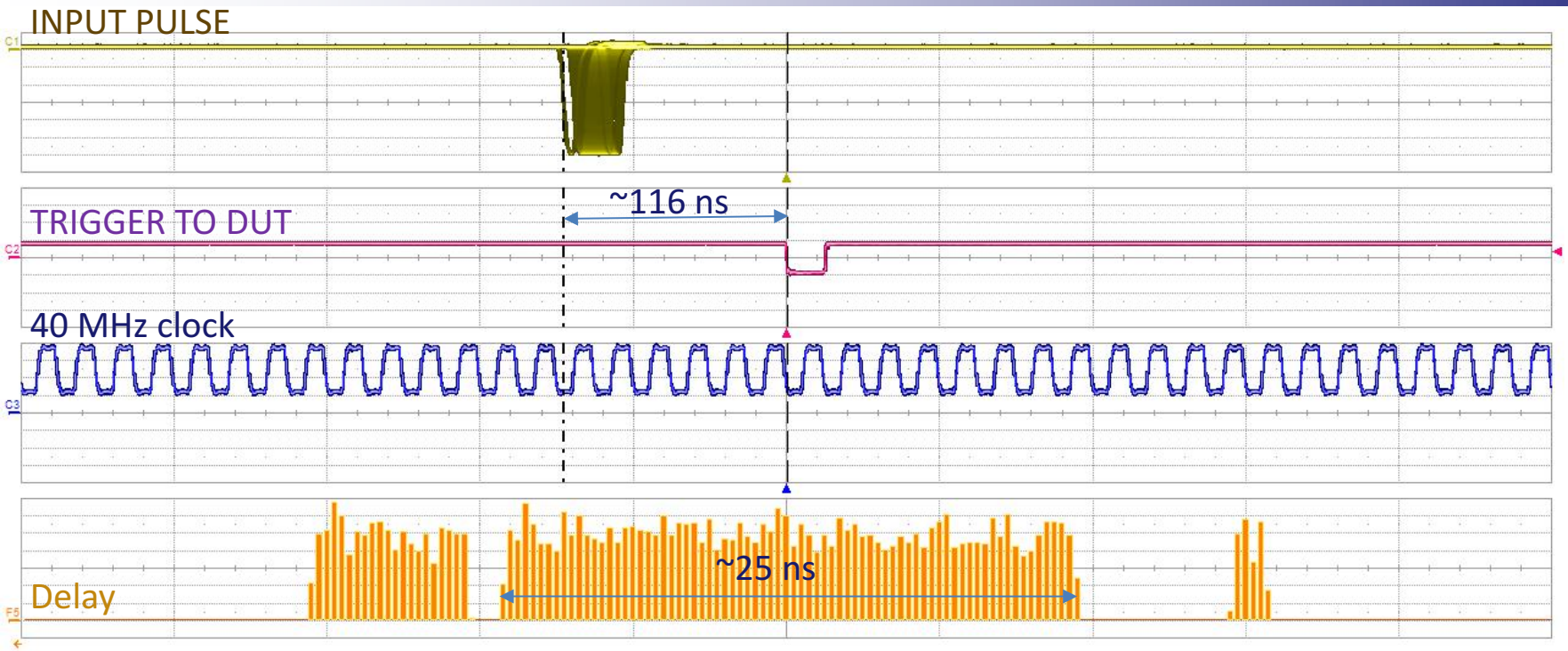


Latency test



- Testing TLU latency
  - Measuring minimum latency.
    - Latency of each input and coincidence window adjustable up to 400ns in steps of 25ns
- Current firmware direct port of miniTLU
  - Includes multiple registers to suppress meta-stability
  - Not yet optimized to reduce latency

Latency test



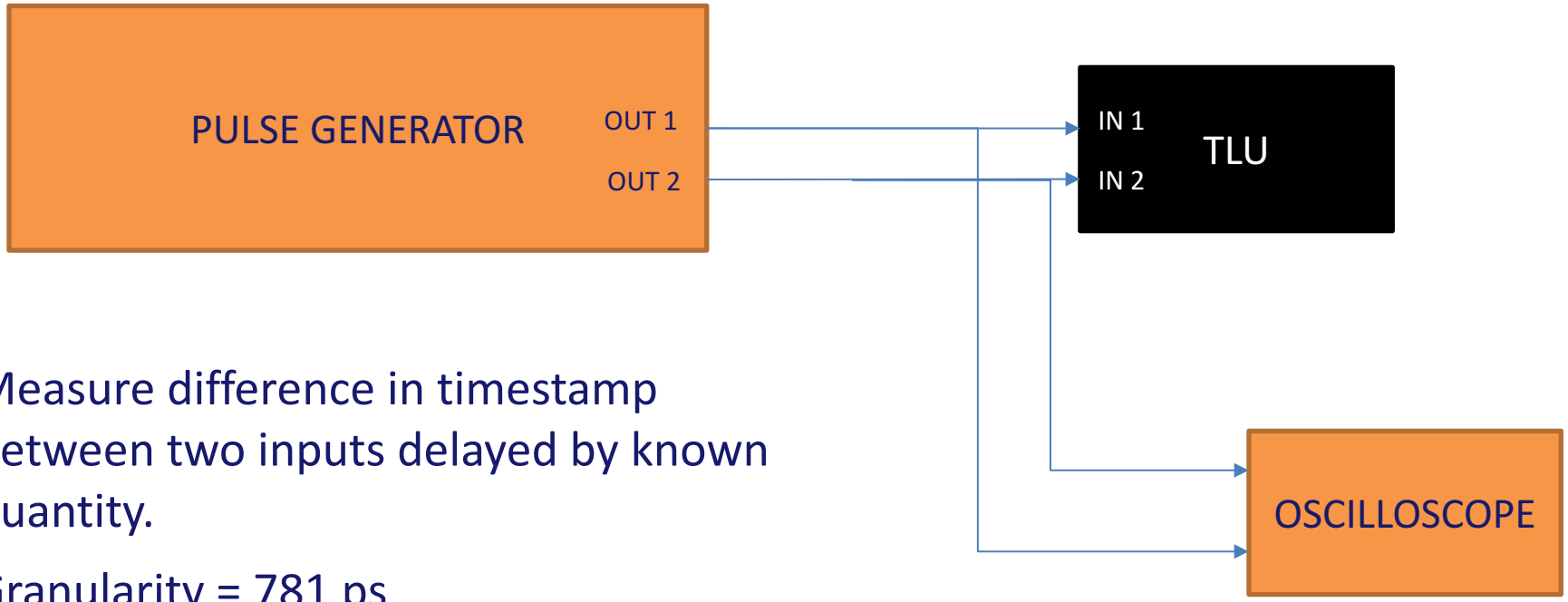
Measure	P1:dt@lv(C1,C2)	P2:freq(C4)	P3:- - -	P4:- - -	P5:freq(C4)	P6:- - -	P7:- - -	P8:- - -
value	135.0389 ns	39.6383 MHz						
mean	128.499 ns	40.0063 MHz						
min	114.7949 ns	38.8166 MHz						
max	146.1616 ns	41.2087 MHz						
sdev	7.984 ns	271.6 kHz						
num	14.050e+3	607.737e+3						
status	✔	⚠						

C1 DC1M 200 mV/div 595.0 mV | C2 DC50 1.00 V/div 0 mV offset | C3 DC1M 500 mV/div 0 mV offset | F5 hist(P1) 10.0 #/div 5.00 ns/div 5.000 k#

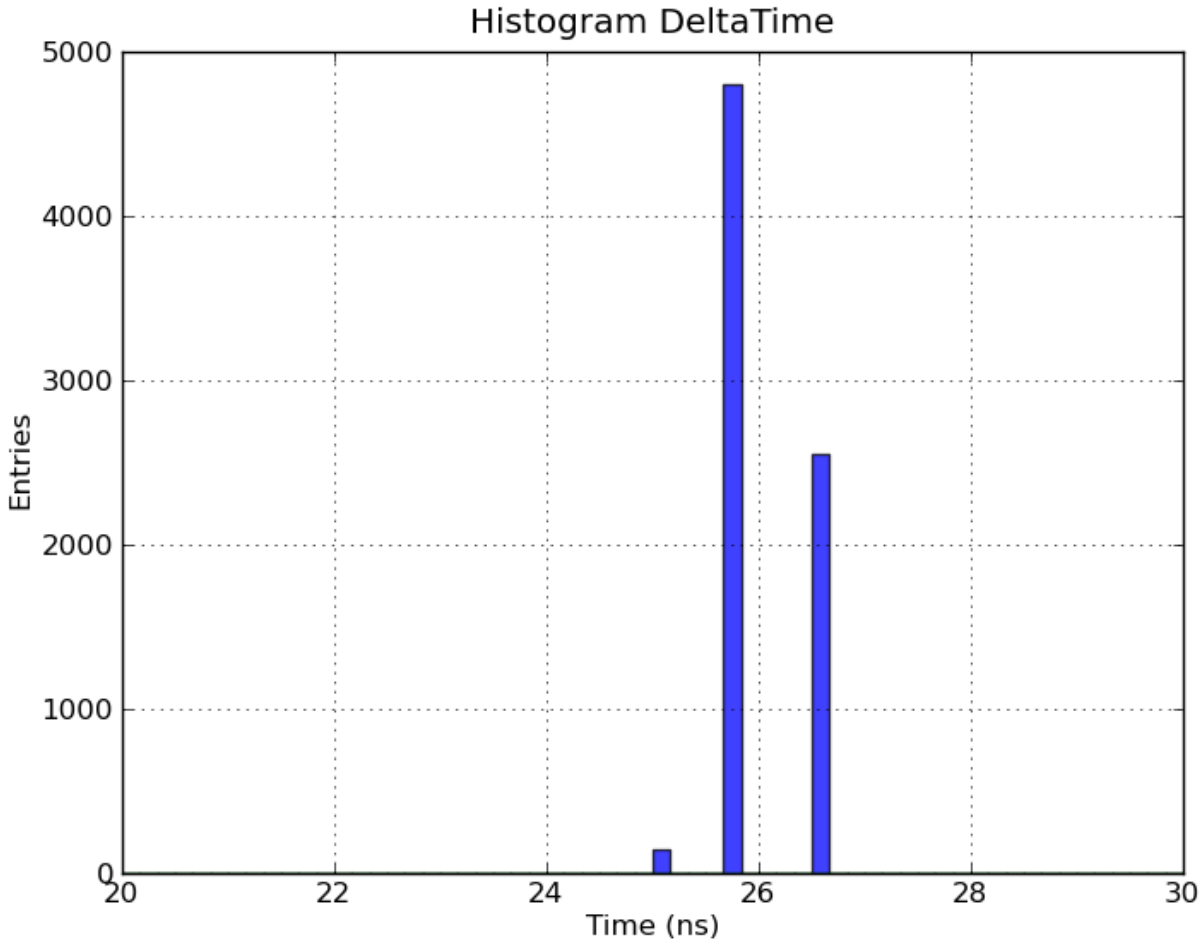
Timebase 0 ns 100 ns/div 20 kS 20 GS/s | Trigger C2 DC Stop 280 mV Edge Neg

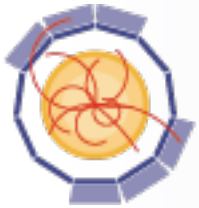
X1= -146.10 ns ΔX= 146.60 ns
X2= 500 ps 1/ΔX= 6.821 MHz

Time resolution test



- Measure difference in timestamp between two inputs delayed by known quantity.
- Granularity = 781 ps
- Work in progress


Histogram DeltaTime
Entries
Time (ns)
0
1000
2000
3000
4000
5000
20
22
24
26
28
30



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