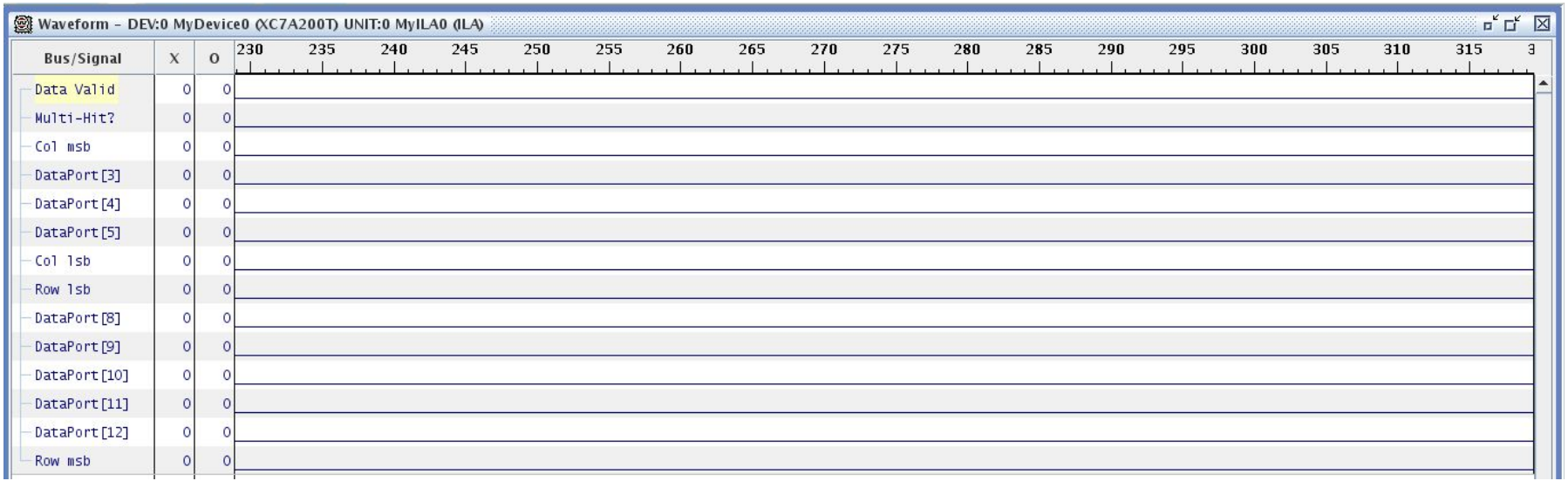
UBC STATUS UPDATE

Previously...

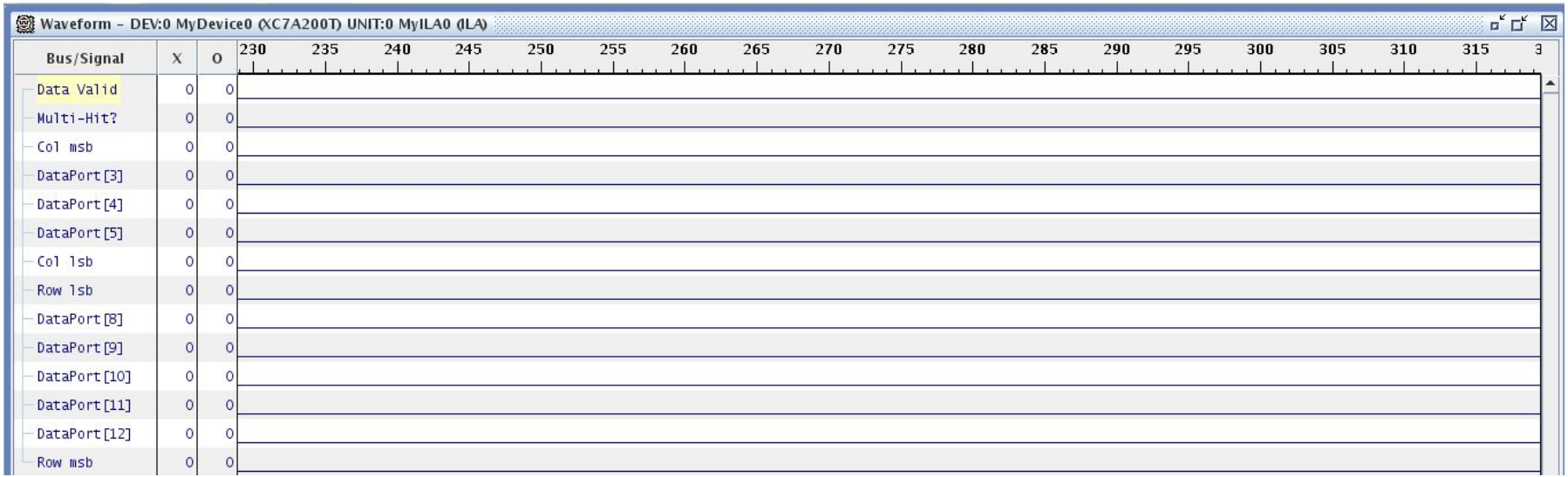
Enable Comparator on All Pixels: 0.758 A

- All Data goes to zeroes, which is what we expect



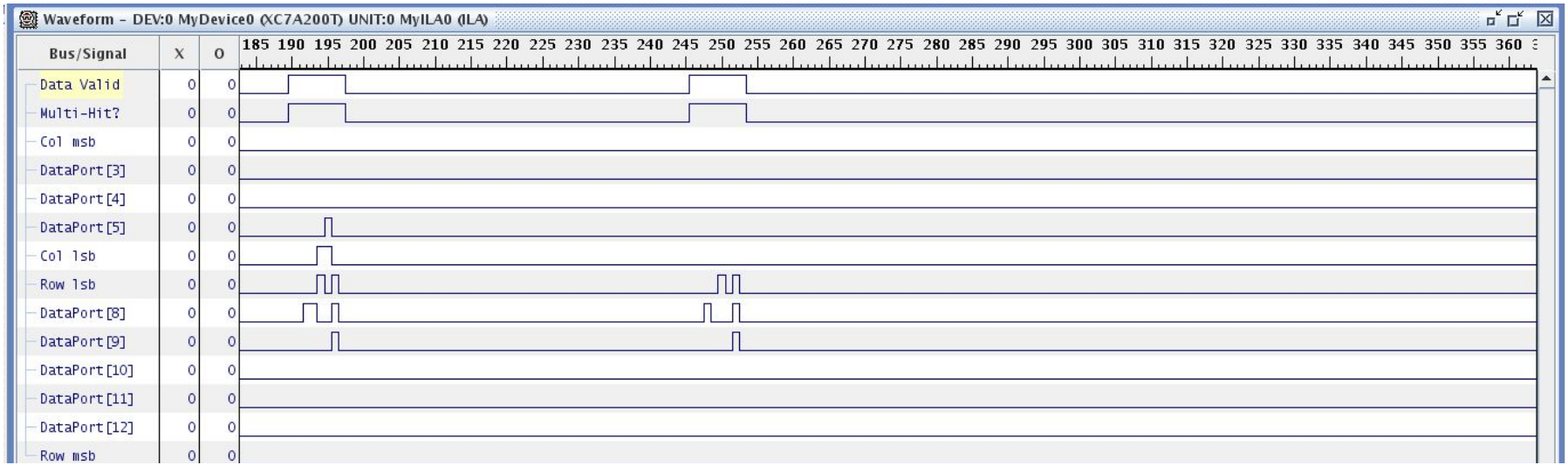
Enable Test Mode: 0.758 A

- However, test mode doesn’t appear to work



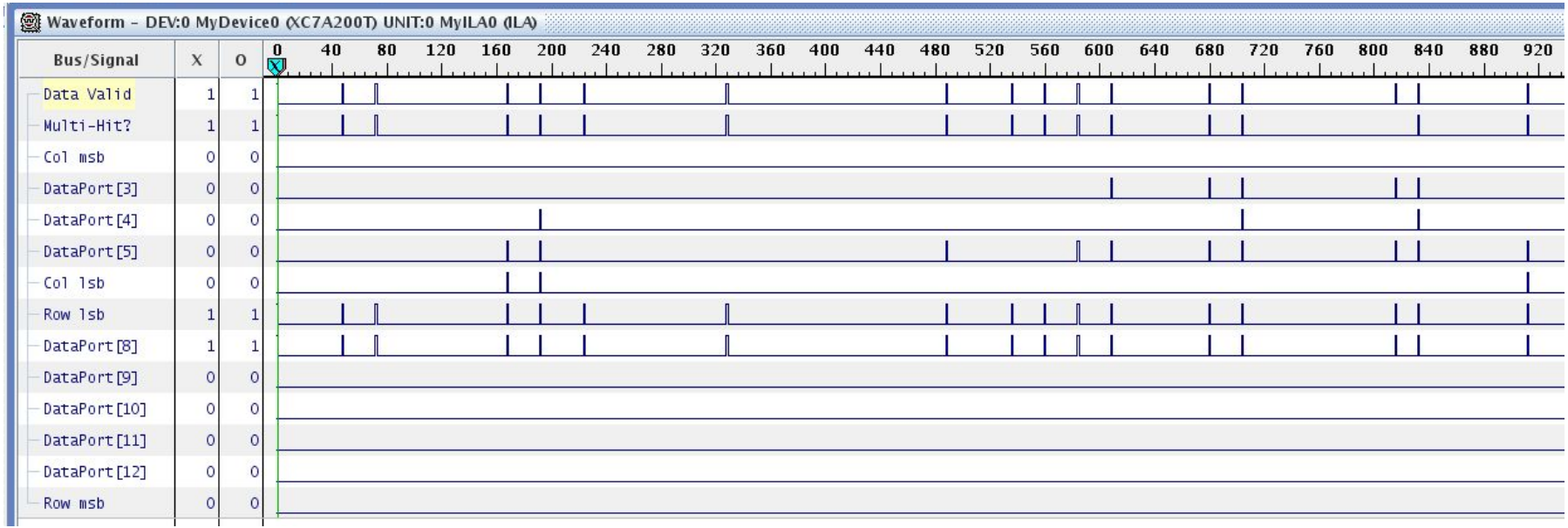
Disable Comparator on All Pixels: 0.830 A

- If we disable comparators, we begin to get back data



Test Mode Enable Row 3

- Row data is correct, column data is still bad and multi-hit is still on



Since then:

- We got test mode to work properly by cutting the 320/40MHz clocks in half to 160/20MHz
- However this throws off the timing in the rest of the firmware, which is what we ultimately want to debug
- We decided to set up the SLAC firmware and use it to debug CHESS-2

Reasoning behind using SLAC carrier/ firmware:

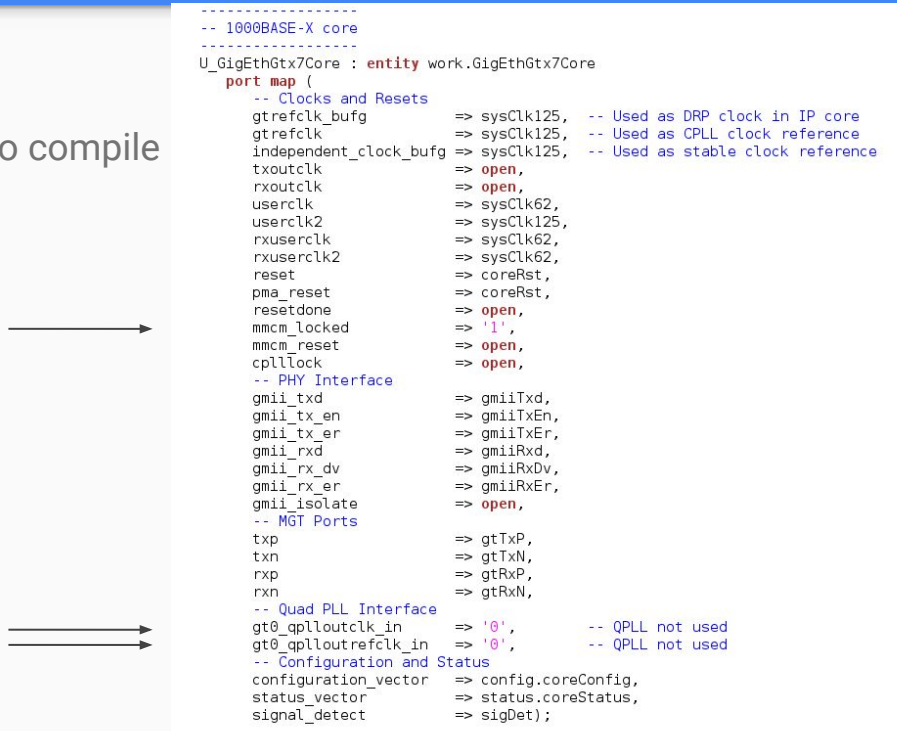
- We will have access to all 3 pixel arrays (perhaps the one we have access to is broken, but the others are working)
- We can check if somehow our setup/configuration is not working
  - Did cross check against defaults.yml

Building the firmware according to the directions on Confluence results in the following error

```
*****************************************************
*****************************************************
*****************************************************
The following error(s) were detected during synthesis:
 near character '1' ; 3 visible types match here [/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/rtl/GigEthGtx7.vhd:175]
 near character '0' ; 3 visible types match here [/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/rtl/GigEthGtx7.vhd:192]
 near character '0' ; 3 visible types match here [/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/rtl/GigEthGtx7.vhd:193]
ERROR: [Common 17-69] Command failed: Synthesis failed - please see the console or run log file for details
*****************************************************
*****************************************************
*****************************************************
```

The lines in question:

- They are all attempting to set a port to 1 or 0
- There are similar lines elsewhere in the file that do compile



```
------------------
-- 1000BASE-X core
------------------
U_GigEthGtx7Core : entity work.GigEthGtx7Core
   port map (
      -- Clocks and Resets
      gtrefclk_bufg          => sysClk125,  -- Used as DRP clock in IP core
      gtrefclk               => sysClk125,  -- Used as CPLL clock reference
      independent_clock_bufg => sysClk125,  -- Used as stable clock reference
      txoutclk               => open,
      rxoutclk               => open,
      userclk                => sysClk62,
      userclk2               => sysClk125,
      rxuserclk              => sysClk62,
      rxuserclk2             => sysClk62,
      reset                  => coreRst,
      pma_reset              => coreRst,
      resetdone              => open,
      mmcm_locked            => '1',
      mmcm_reset             => open,
      cplllock               => open,
      -- PHY Interface
      gmii_txd               => gmiiTxd,
      gmii_tx_en             => gmiiTxEn,
      gmii_tx_er             => gmiiTxEr,
      gmii_rxd               => gmiiRxd,
      gmii_rx_dv             => gmiiRxDv,
      gmii_rx_er             => gmiiRxEr,
      gmii_isolate           => open,
      -- MGT Ports
      txp                    => gtTxP,
      txn                    => gtTxN,
      rxp                    => gtRxP,
      rxn                    => gtRxN,
      -- Quad PLL Interface
      gt0_qplloutclk_in      => '0',        -- QPLL not used
      gt0_qplloutrefclk_in   => '0',        -- QPLL not used
      -- Configuration and Status
      configuration_vector   => config.coreConfig,
      status_vector          => status.coreStatus,
      signal_detect          => sigDet);
```

Vivado project doesn’t have the source linked to this component

Tried adding source manually in Vivado

Source: /home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/dcp/coregen/GigEthGtx7Core.xci

Get a new error (appears related to the same core):

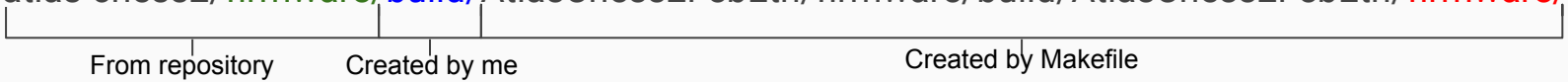
```
WARNING: [Vivado 12-4802] The synthesis checkpoint for IP '/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/dcp/coregen/GigEthGtx7Core.xci' is not generated
and IP is locked. An out-of-context (OOC) run will be created and/or launched, but synthesis may not be able to complete or could result in incorrect behavior.
Please select 'Report IP Status' from the 'Tools/Report' menu or run Tcl command 'report_ip_status' for more information.
WARNING: [Project 1-576] IP '/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/dcp/coregen/GigEthGtx7Core.xci' in run GigEthGtx7Core_synth_1 is locked, no out
-of-context (OOC) run will be launched. The run may not be able to complete.
Please select 'Report IP Status' from 'Tools/Report' or run the Tcl command 'report_ip_status' for more information.
CRITICAL WARNING: [IP_Flow 19-4739] Writing uncustomized BOM file '/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/dcp/coregen/GigEthGtx7Core.xml'
WARNING: [Project 1-576] IP '/home/ibmayer/SLAC/atlas-chess2/firmware/submodules/surf/ethernet/GigEthCore/gtx7/dcp/coregen/GigEthGtx7Core.xci' in run GigEthGtx7Core_synth_1 is locked, no out
-of-context (OOC) run will be launched. The run may not be able to complete.
Please select 'Report IP Status' from 'Tools/Report' or run the Tcl command 'report_ip_status' for more information.
[Wed Jun 21 16:08:00 2017] Launched GigEthGtx7Core_synth_1...
Run output will be captured here: /home/ibmayer/SLAC/atlas-chess2/firmware/build/AtlasChess2FebEth/AtlasChess2FebEth_project.runs/GigEthGtx7Core_synth_1/runme.log
[Wed Jun 21 16:08:00 2017] Launched synth_1...
Run output will be captured here: /home/ibmayer/SLAC/atlas-chess2/firmware/build/AtlasChess2FebEth/AtlasChess2FebEth_project.runs/synth_1/runme.log
launch_runs: Time (s): cpu = 00:00:09 ; elapsed = 00:00:09 . Memory (MB): peak = 1359.336 ; gain = 51.070 ; free physical = 1510 ; free virtual = 11346
[Wed Jun 21 16:08:00 2017] Waiting for synth_1 to finish...
[Wed Jun 21 16:08:18 2017] synth_1 finished
wait_on_run: Time (s): cpu = 00:00:17 ; elapsed = 00:00:18 . Memory (MB): peak = 1363.195 ; gain = 3.859 ; free physical = 1513 ; free virtual = 11350
```

- This says that “IP is locked”
- This seems to indicate that we do not have access to some Xilinx IP core (or perhaps a 3rd party IP core)

The Makefile is creating a strange infinite-link directory loop

```
[ibmayer@ubc-itk-daq AtlasChess2FebEth]$ ls -ld firmware/build/AtlasChess2FebEth/
drwxrwxr-x. 8 ibmayer ibmayer 4096 Jun 21 13:56 firmware/build/AtlasChess2FebEth/
[ibmayer@ubc-itk-daq AtlasChess2FebEth]$ ls -ld firmware/build/AtlasChess2FebEth/firmware
lrwxrwxrwx. 1 ibmayer ibmayer 40 Jun 21 13:22 firmware/build/AtlasChess2FebEth/firmware -> /home/ibmayer/SLAC/atlas-chess2/firmware
[ibmayer@ubc-itk-daq AtlasChess2FebEth]$ pwd
/home/ibmayer/SLAC/atlas-chess2/firmware/build/AtlasChess2FebEth
[ibmayer@ubc-itk-daq AtlasChess2FebEth]$
```

- I create atlas-chess2/firmware/build/ (as per the Confluence instructions)
- The makefile creates (in the build/ dir): AtlasChess2FebEth/firmware/build/AtlasChess2FebEth/firmware/
- The firmware/ in red is a link to the firmware/ in green
- atlas-chess2/firmware/build/AtlasChess2FebEth/firmware/build/AtlasChess2FebEth/firmware/



Software Question from Robin

I've been looking through slack software/firmware package: https://github.com/slaclab/atlas-chess2

The configure pixel payload is inverted:

Is this correct?

```
@staticmethod
def configPixel(enable, chargeInj, trimI):
    # Default value: disable pixel, no charge injection, all trim bits disabled
    value = 0x00
    # Check if pixel is enabled
    if enable:
        value |= 0x20
    # Check if enabling charge injection
    if chargeInj:
        value |= 0x01
    # Set the trim current source
    value |= ((trimI & 0xF) << 1)
    # Return the inverted value
    return((~value)&0x3F)
```

Link to method