

Configurable Crossbar Switch for Deterministic, Low-latency Inter-blade Communications in a MicroTCA Platform

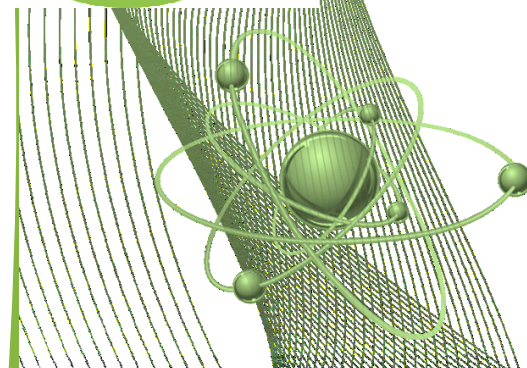
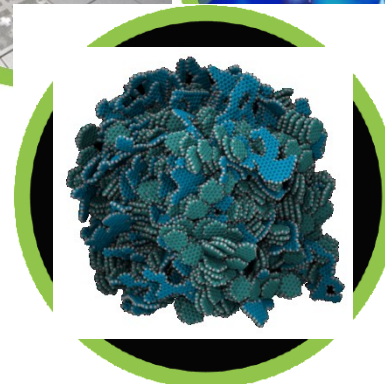
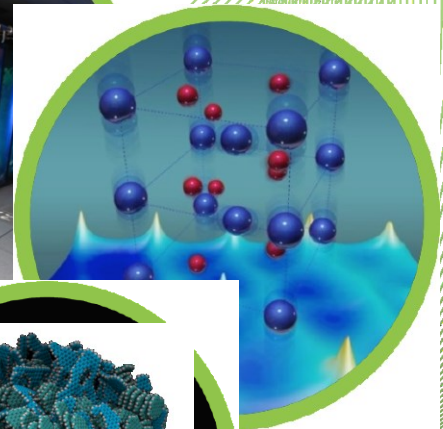
Eric Breeding

Spallation Neutron Source
Oak Ridge National Laboratory

Presented to

6th MicroTCA Workshop for Industry and
Research

December 7, 2017
DESY, Hamburg



Outline of Presentation

- Introduction to the Spallation Neutron Source (SNS)
- SNS Fast Protection System (FPS)
 - Purpose
 - Architecture
- Crossbar Overview
- Concluding Remarks
- Appendix: MicroTCA Development at SNS

The Spallation Neutron Source (SNS) Provides the Most Intense Pulsed Neutron Beams in the World for Scientific R&D



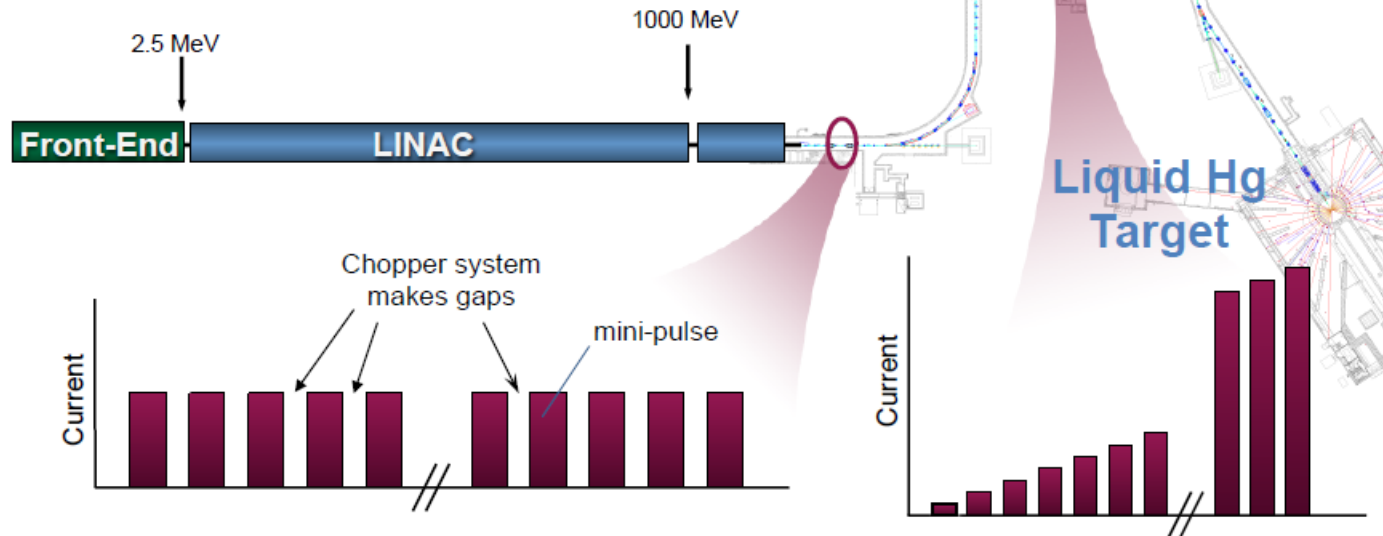
- Operational since 2007, but built with “1990s” electronics
- Obsolescence is driving new developments at SNS

SNS Accelerator Complex

Front-End:
Produce a 1-msec
long, chopped,
H⁺ beam

**1 GeV
LINAC**

**Accumulator
Ring:** Compress 1
msec long pulse to
700 nsec



Production Run Parameters:

- Peak current: 38 mA
- Repetition rate: 60 Hz
- Macro-pulse length: 0.85 – 0.975 ms
- Average power: 1.2 – 1.4 MW

High Beam Power Is Accompanied by Significant Hazards

- Hazards

- Uncontrolled energy release (beam loss)
- hardware systems failure

- Threats

- physical damage
- radio-activation

- Mitigation

- monitor systems for problems - magnets, RF, Vacuum, etc...
- “quickly” terminate beam production when a problem (fault) occurs



MEBT Chopper Target Rupture: FY2014

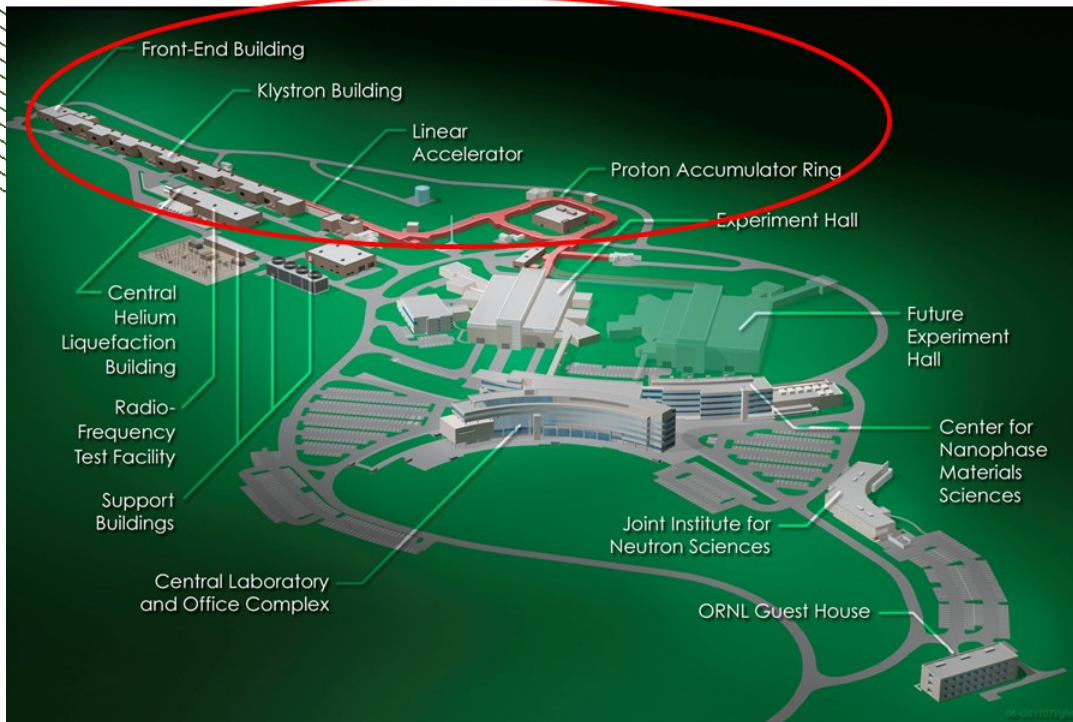
Example of a Fault-causing Occurrence



Raccoon in 13 kV switchgear. 15 % of FY 2010 AC systems downtime (4 hours). Allegedly tastes like chicken.

Photo and remark courtesy of John Galambos: JAS14 (USPAS), Long Beach CA

FPS Purpose: Mitigate Hazards that Threaten Accelerator Components

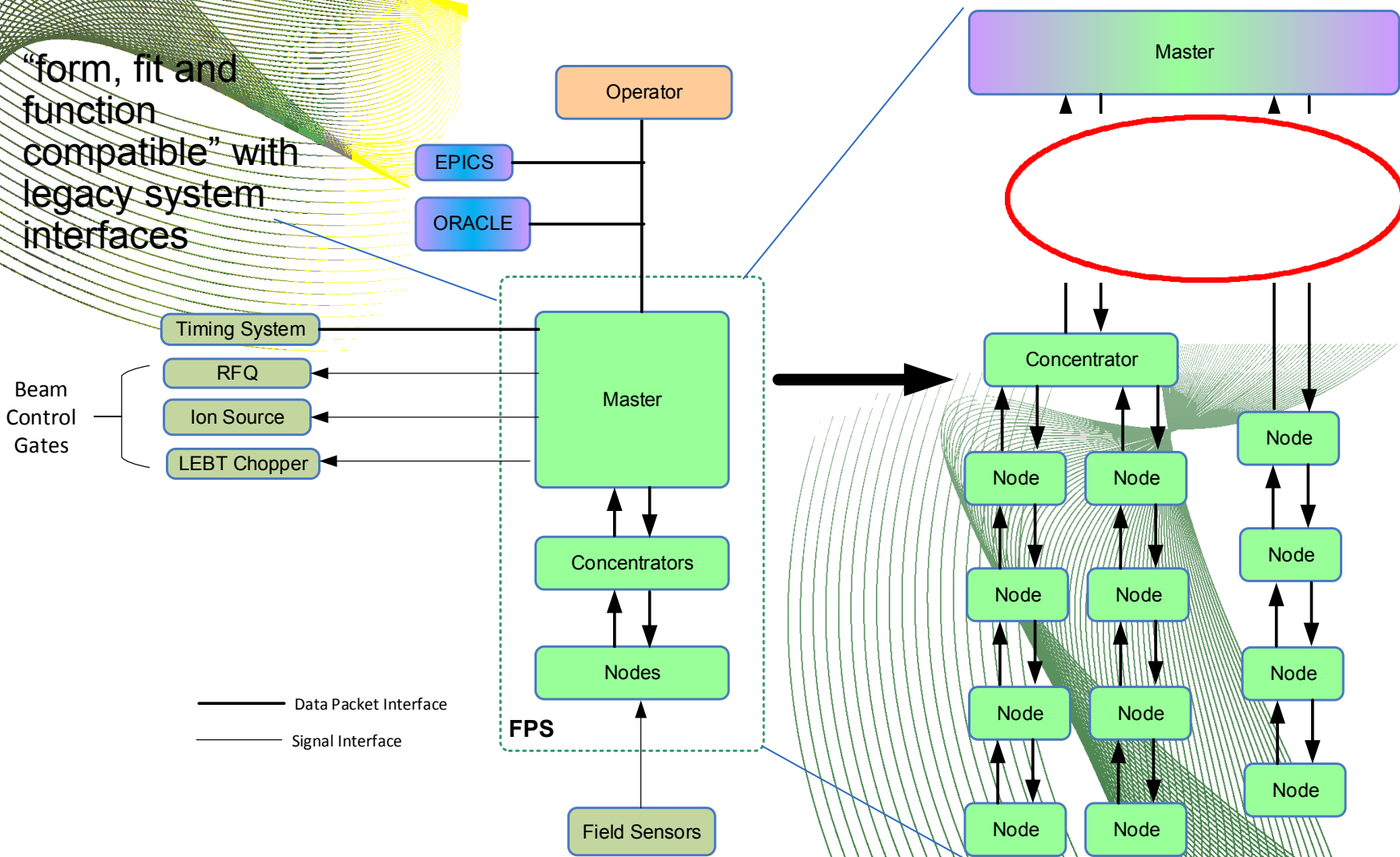


- FPS monitors more than 1000 sensors covering a large area
- FPS terminates beam generation if a qualified fault occurs
- Response to a detected fault must be less than **20 usec**

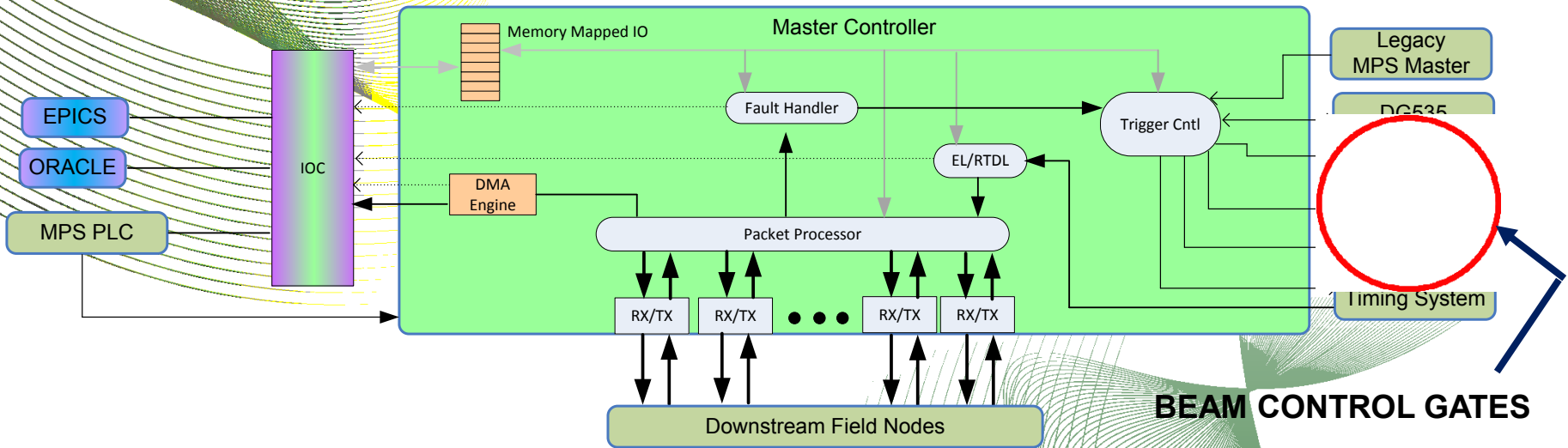
**FPS must be a system with: (1) a fast response time
(2) a reliable (deterministic) response time**

New FPS: Low-latency, Distributed Architecture

“form, fit and function compatible” with legacy system interfaces

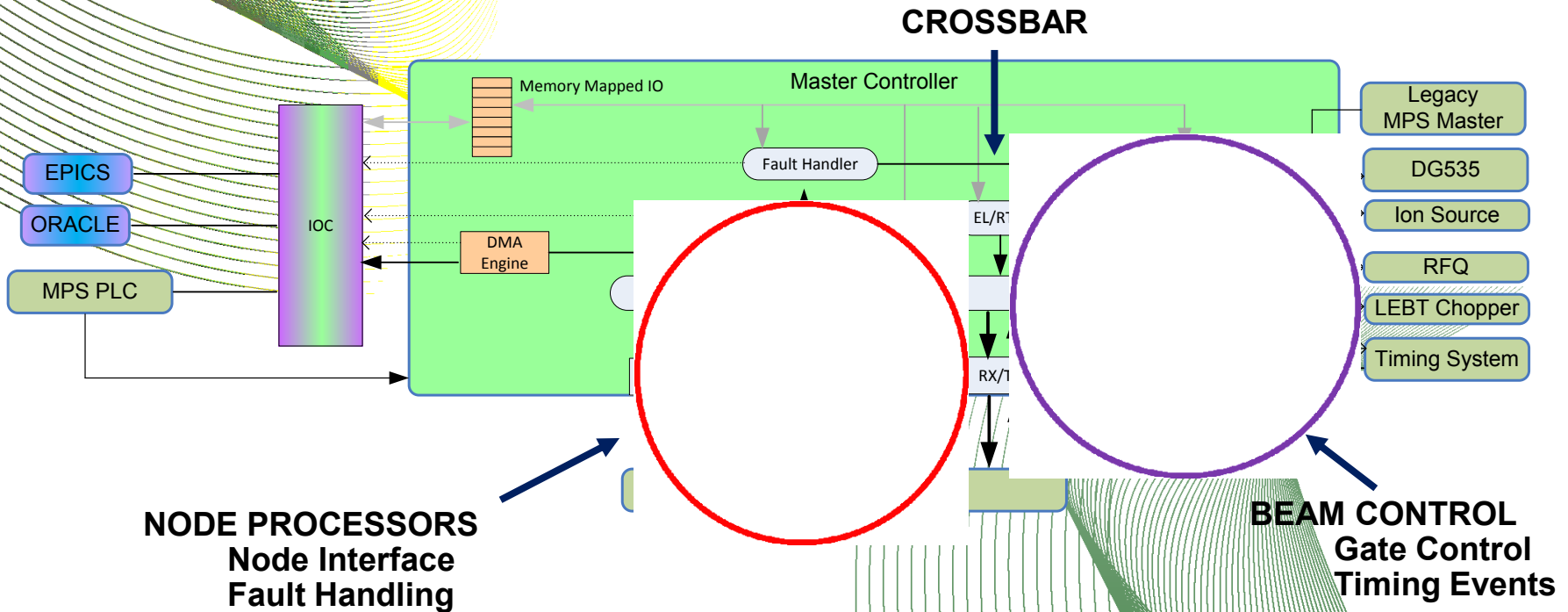


Master Controller Is the Principal Subsystem of the FPS



- Master controller uses gates to control the beam generation. It terminates beam if:
 - a qualified fault condition is received from downstream node
 - beam power exceeds the operating envelope
 - beam power exceeds that allowed for a particular machine mode.

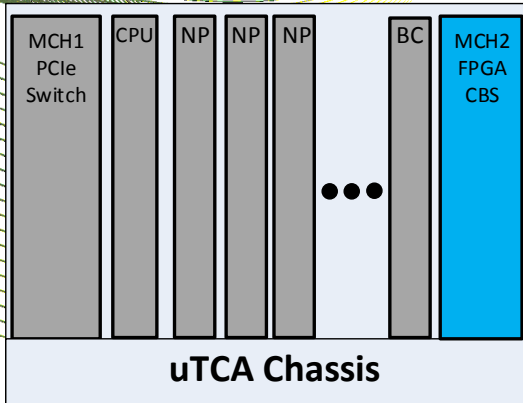
Master Controller Functionality Maps to Three Types of (uTCA) Modules



- Why do we need a Crossbar?

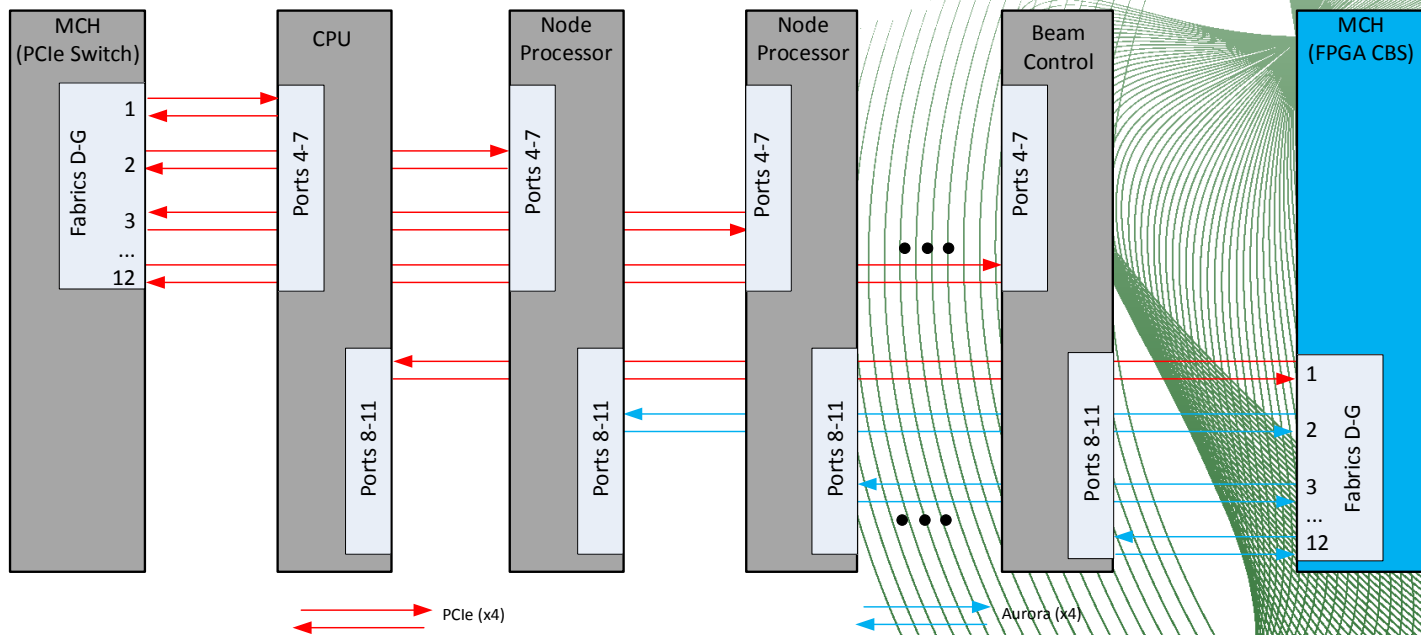
ALL NODES NEED “SIMULTANEOUS” ACCESS TO BEAM CONTROLLER and TIMING INFORMATION

Master Controller: MicroTCA Platform with a Special MCH



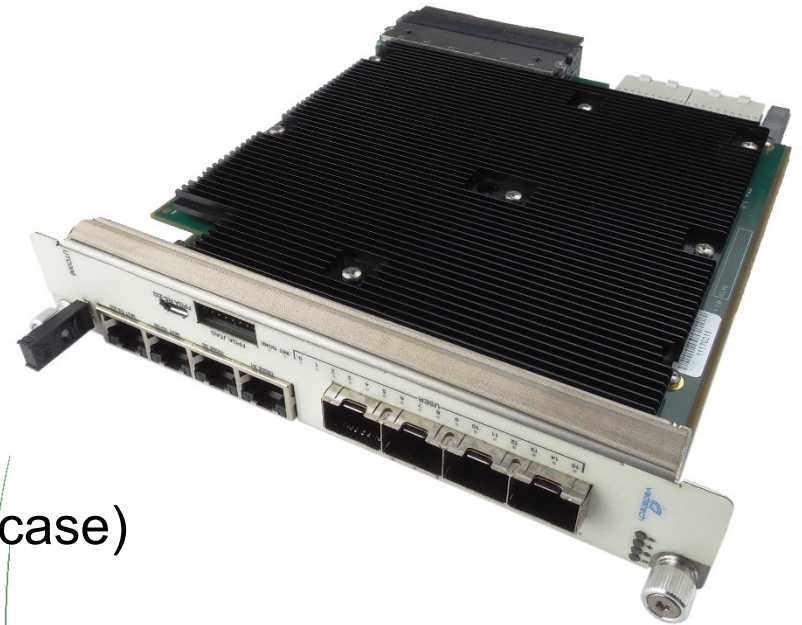
AMC {

- MCH1: PCIe Switch
- CPU: Processor, Intel Core i7 (Linux)
- NP: Node Processor (up to 10)
- BC: Beam Control
- MCH2: FPGA Crossbar (CBS)

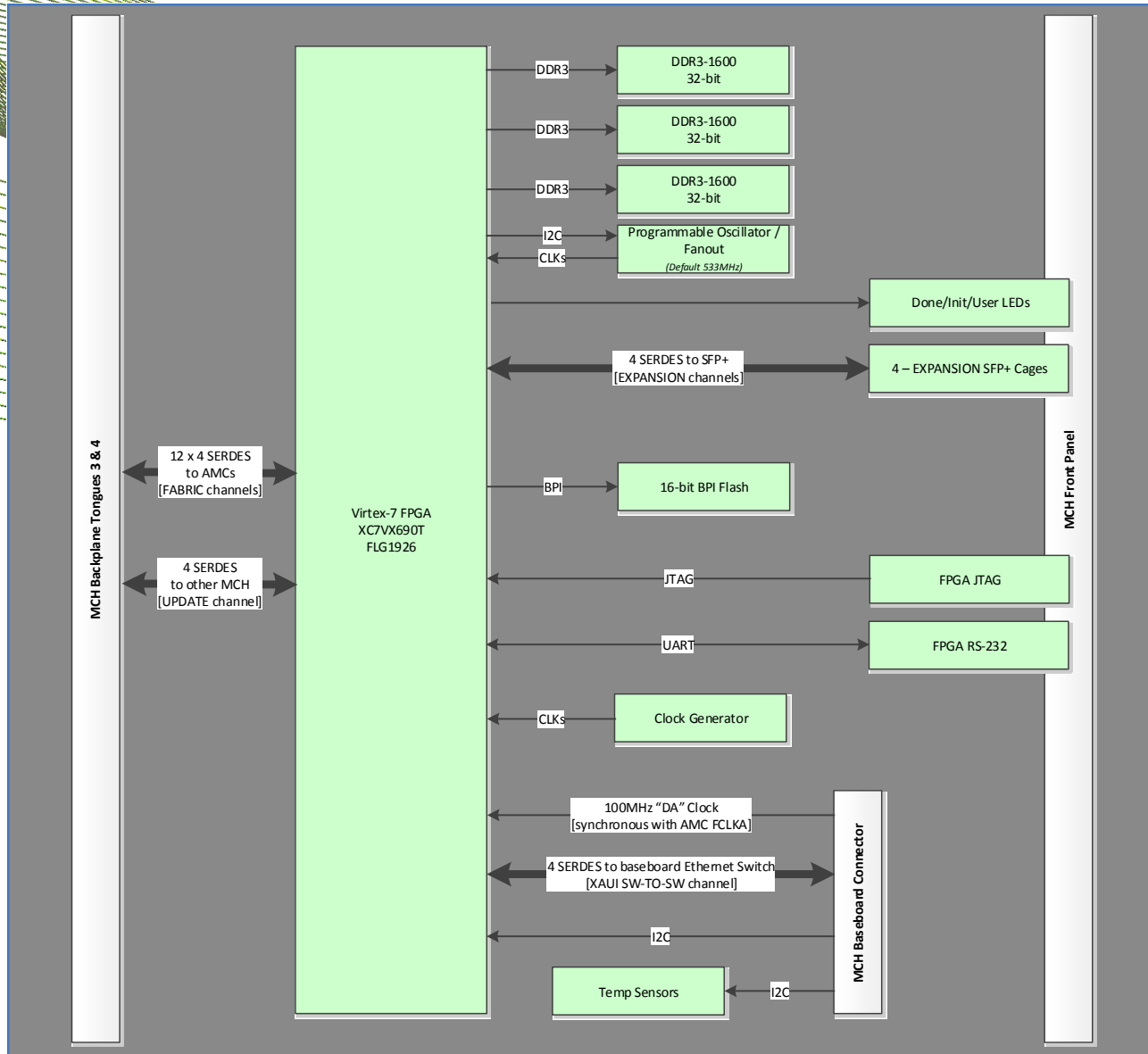


FPGA CBS: Configurable MCH for User-defined Protocols for Interfacing AMC Modules

- Vadatech UTC006-100-000-000
 - Xilinx Virtex-7 FPGA (XC7V690T)
 - 12 ports x 4 (lanes/ port)
 - 4 SFP+ on Front-panel
 - 3 GB DDR
 - 48 GB/s Aggregate BW (ORNL use case)

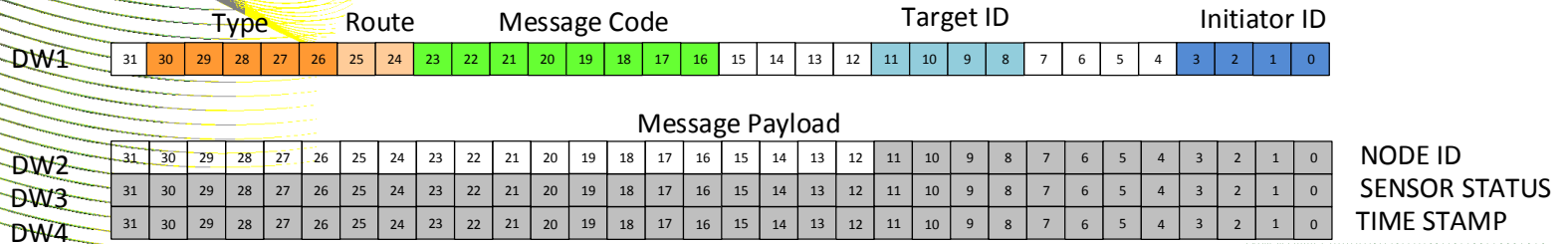


Vadatech UTC006-100 Block Diagram



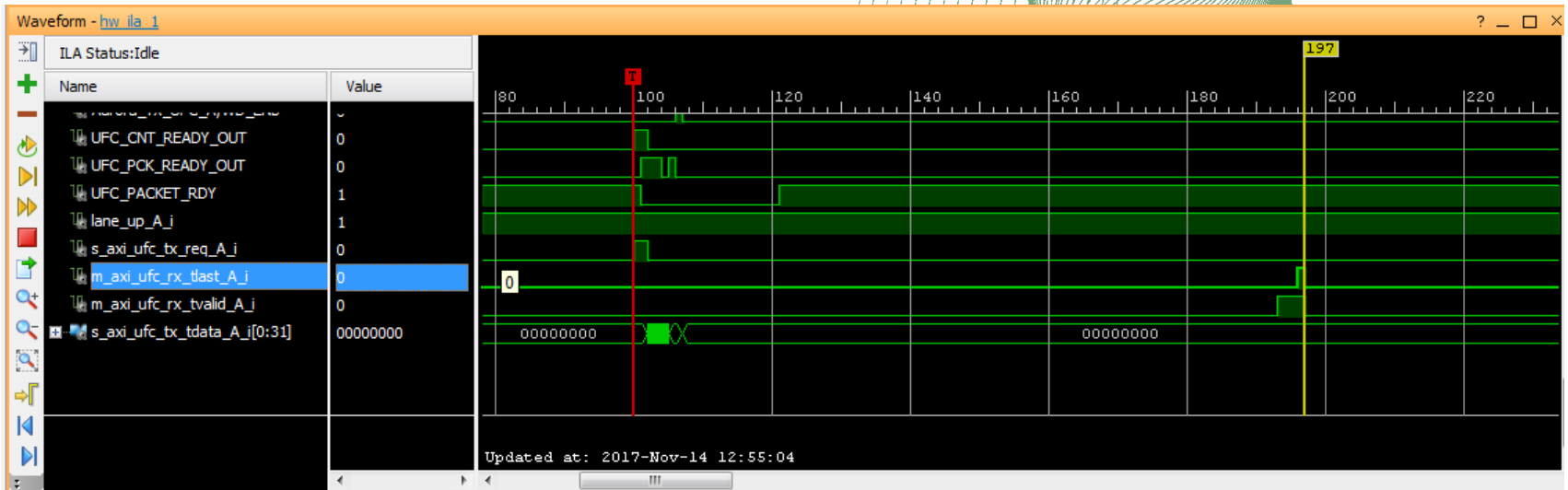
Aurora 8B/10B Protocol Provides Deterministic Performance for Fault Messages

- User Flow Control (UFC): 16-byte message

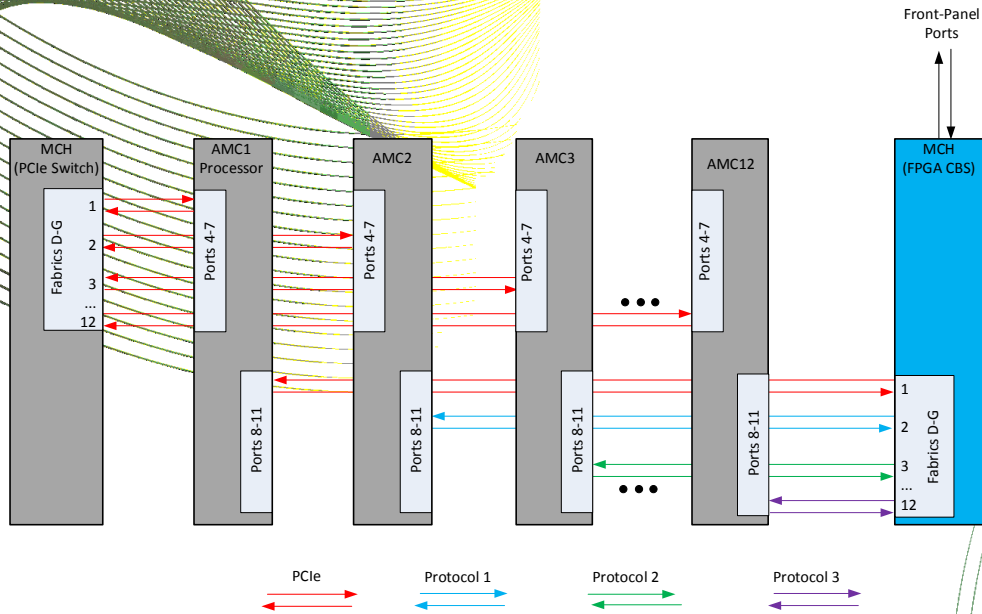


- Latency:

$$97 \times (\sim 6.4 \text{ ns}) = \sim 620 \text{ ns}$$



FPGA CBS Represents a Significant Breakthrough in Inter-blade Communications



- Point-to-point (P2P)
 - Any slot to any slot
 - Standard backplane
 - Low latency
 - Carrier-to-carrier
 - Multi-protocol
- “Intelligent” Switching
 - “Many-to-one”
 - “One-to-many”
 - Data reduction

Type			Route			Message Code			Target ID Mask			Initiator ID																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Message Payload																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

For More Information...

- Embedded Systems Magazine, July 2017

– <http://eecatalog.com/atca/2017/07/17/configurable-crossbar-switch-for-deterministic-low-latency-inter-blade-communications-in-a-microtca-platform/>

- Contact: Eric Breeding (breedingj@ornl.gov)

- www.vadatech.com

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Configurable Crossbar Switch for Deterministic, Low-latency Inter-blade Communications in a MicroTCA Platform

Machine Protection—Using a MicroTCA-based platform to protect the Spallation Neutron Source's particle accelerator from its own high energy beam

By Eric Breeding, Oak Ridge National Laboratory, David Karamov, Vadatech, Inc., and Alan Astic, Oak Ridge National Laboratory

INTRODUCTION
The Spallation Neutron Source (SNS) provides the highest neutron flux in the world for scientific research and industrial development. The high power generated by the SNS particle accelerator (Figure 1) is inherently accompanied by hazards of uncontrolled energy release (beam loss), uncontrolled power rise, and failure of hardware systems. These hazards pose a significant threat to accelerator components, physical damage and radioactivity. To mitigate the risks associated with these hazards, the accelerator utilizes a Machine Protection System (MPS). The MPS monitors more than 1,000 sensors throughout the accelerator complex for potential problems. When such problems are detected, the MPS must terminate beam production within 20 microseconds to prevent accelerator components. A highly reliable MPS is critical to maintaining the demanding availability requirements for the SNS facility. The existing MPS is functional and operational, however, its reliability and maintainability are declining due to aging hardware and component obsolescence. Consequently, a new MPS system is being developed to replace the current MPS. This system is based on the MicroTCA

Due to the large physical area covered by the sensors, the new MPS employs a distributed architecture interconnected with high-speed serial communication links. The stringent beam control demands require both cross-shelf and cross-blade links to be low latency and deterministic. Legacy bus architectures complicated inter-blade communications using dedicated parallel buses across the backplane. Because of limited fabric resources on its backplane, MicroTCA uses discrete bus (MCB) for this purpose. Deterministic MCBs protect from external sources are limited to standard bus protocols such as PCI Express, Serial RapidIO, and IEEE Gigabit Ethernet (GbE). While these protocols have exceptional throughput capability, they are neither deterministic nor memory-to-memory. The development of an MCB with a user-configurable switch fabric overcomes this limitation, allowing the system architect/developer complete


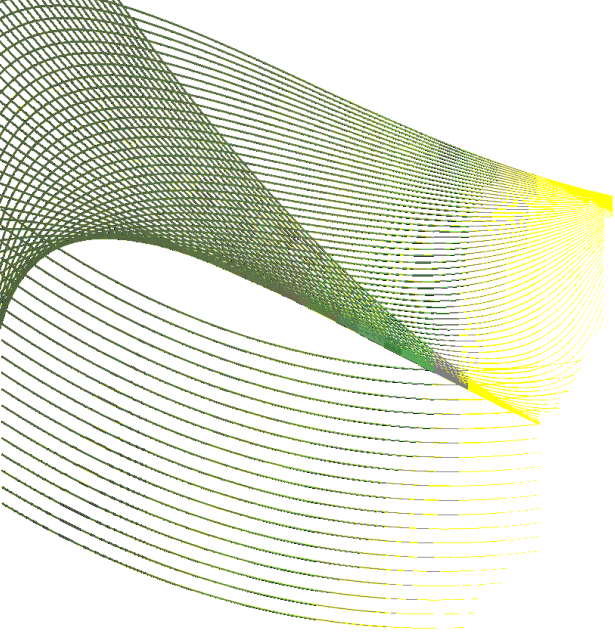


Figure 1. Oak Ridge National Laboratory's Spallation Neutron Source uses a linear accelerator and accelerator ring to generate a 1.8-MeV neutron proton beam.

34 | EMBEDDED SYSTEMS ENGINEERING • July 2017



Appendix



Additional MicroTCA Development at SNS



New MicroTCA Ring LLRF System Deployed for Neutron Production (October 2017)

Status


Overview
Beam
Diagnostics
Log

As of 01:09 on December 06, 2017,
Beam to Target
1213 kW
 Neutron production is underway.

As of 07:58 on December 06, 2017,
 Reactor Power is at
83 MW
 The reactor is currently operating at
 100% power for fuel cycle 476.

SNS Energy Plot

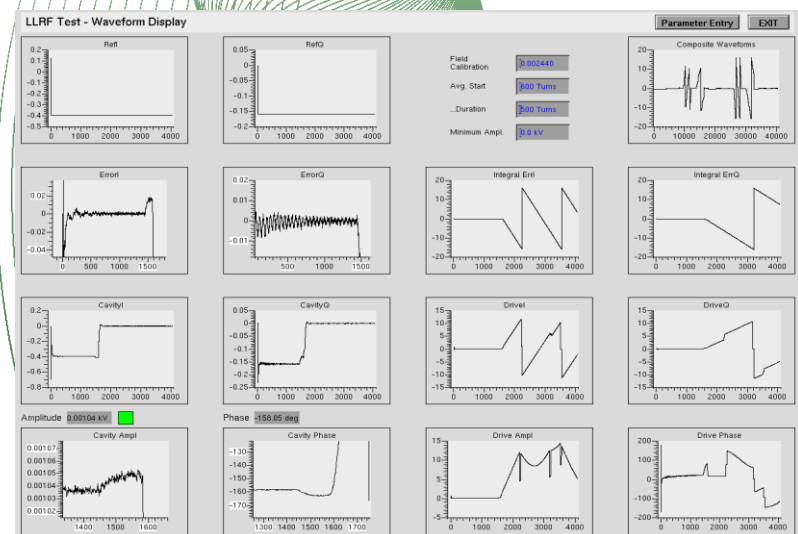
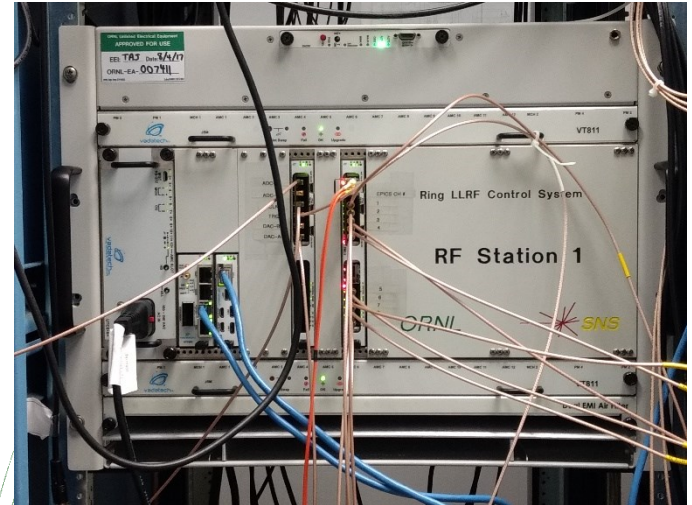


Accelerator Messages

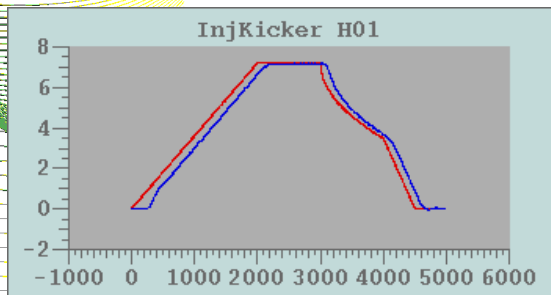
SNS - Beam SNS beam is on target at 1.2 MW.
Status Update
 2017-12-06
 07:25

HFIR - Status Update
 2017-12-04
 20:49

Reactor is on at ~84 MW. The end of run cycle 476 is expected on Friday 12/8 between 1300 and 1500 hours.



Development of MicroTCA Injection Kicker Waveform Monitor Nearing Completion



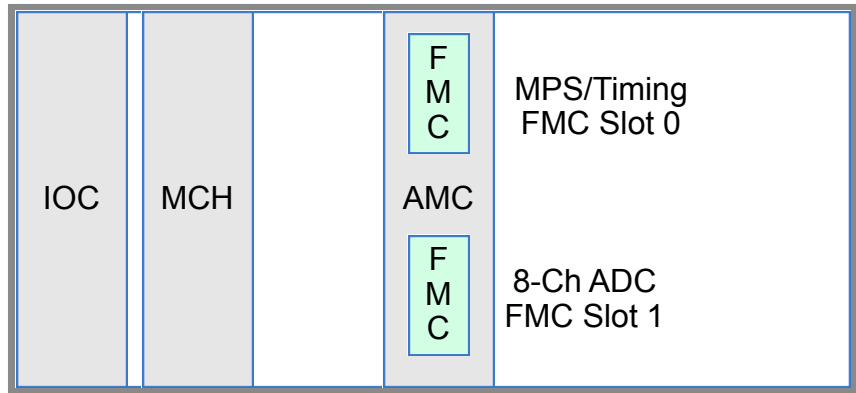
LeCroy Scope
GT&FS ❌

LeCroy Scope
Diagnostic ❌

LeCroy Scope
Diagnostic ❌

LeCroy Scope
WFM ❌

LeCroy Scope
WFM ❌



Single Card Solution:
 8-Channel ADC (2.5 MSPS)
 Single Link interface
 12 user-defined interrupts
 Dual-channel DMA





Thank you for your attention!

Questions?

