Complete MRF Timing System on MicroTCA.4 Platform

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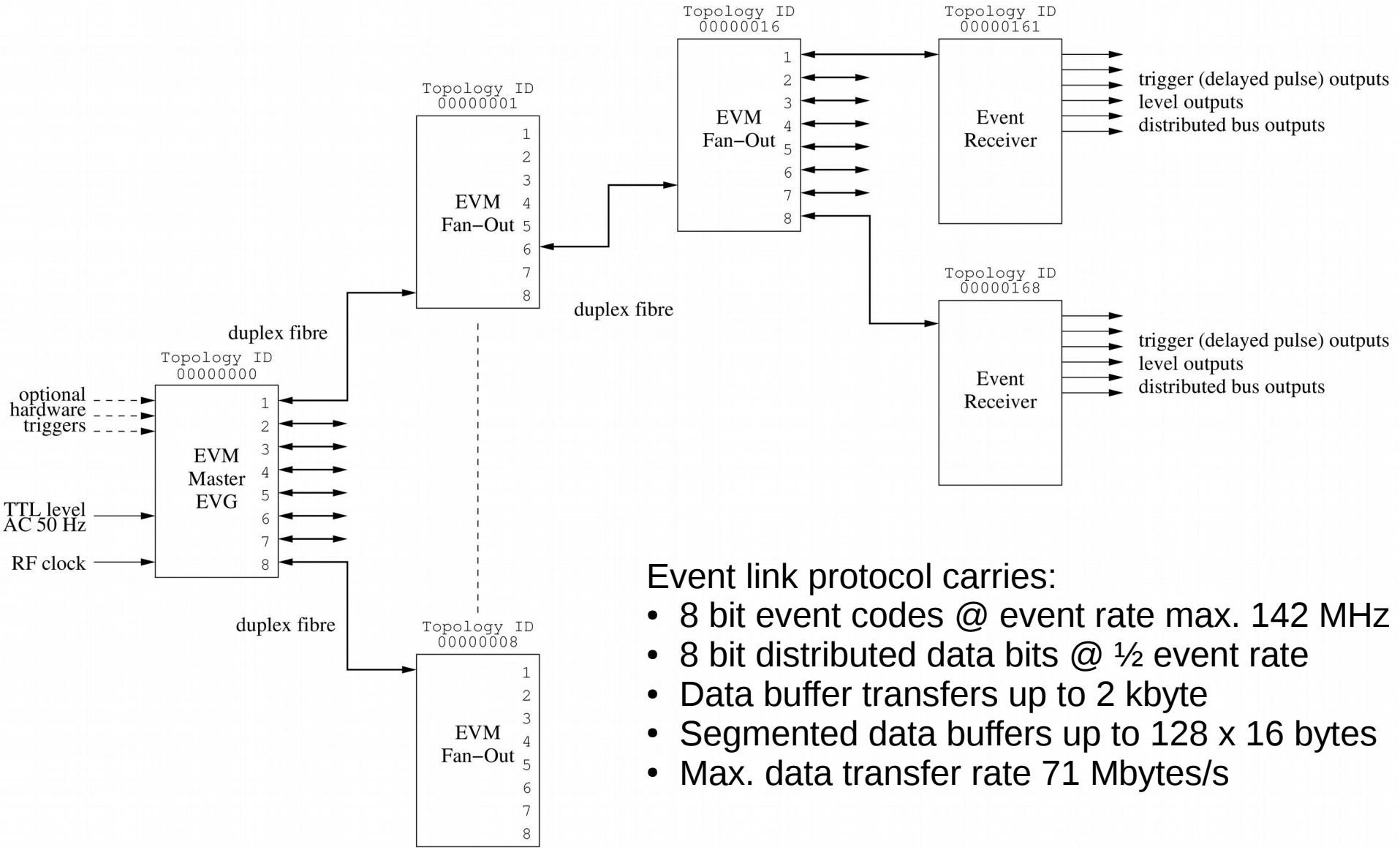
MRF Timing System

- MRF Timing System was originally developed for the Swiss Light Source (PSI) in 1999 and was designed to be software compatible with the APS (Argonne National Labs) timing system
- Based on a central Event Generator (EVG) and Event Receivers (EVR) in star topology and “passive” fan-outs
- Newest generation of MRF timing system is the Delay Compensation version which is available on VME, PCIe (EVR only) and MicroTCA (EVR and more to come in 2018) and requires active fan-outs and duplex fibers
- Based on 8B10B encoding
- Synchronous to an externally supplied RF reference
- Event Receivers are phase locked to RF reference

Delay Compensation (DC) Typical System Layout



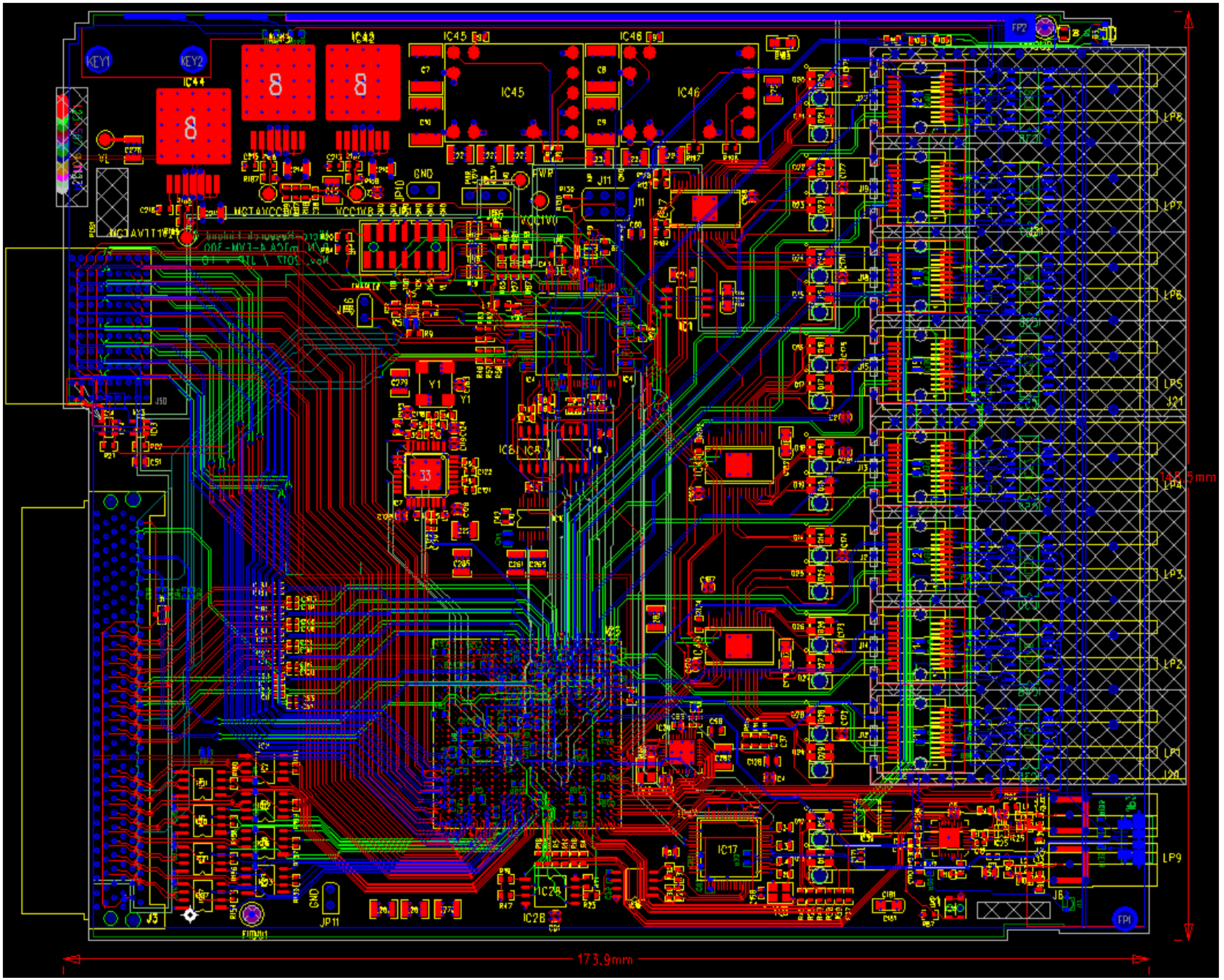
Event link protocol carries:

- 8 bit event codes @ event rate max. 142 MHz
- 8 bit distributed data bits @ ½ event rate
- Data buffer transfers up to 2 kbyte
- Segmented data buffers up to 128 x 16 bytes
- Max. data transfer rate 71 Mbytes/s

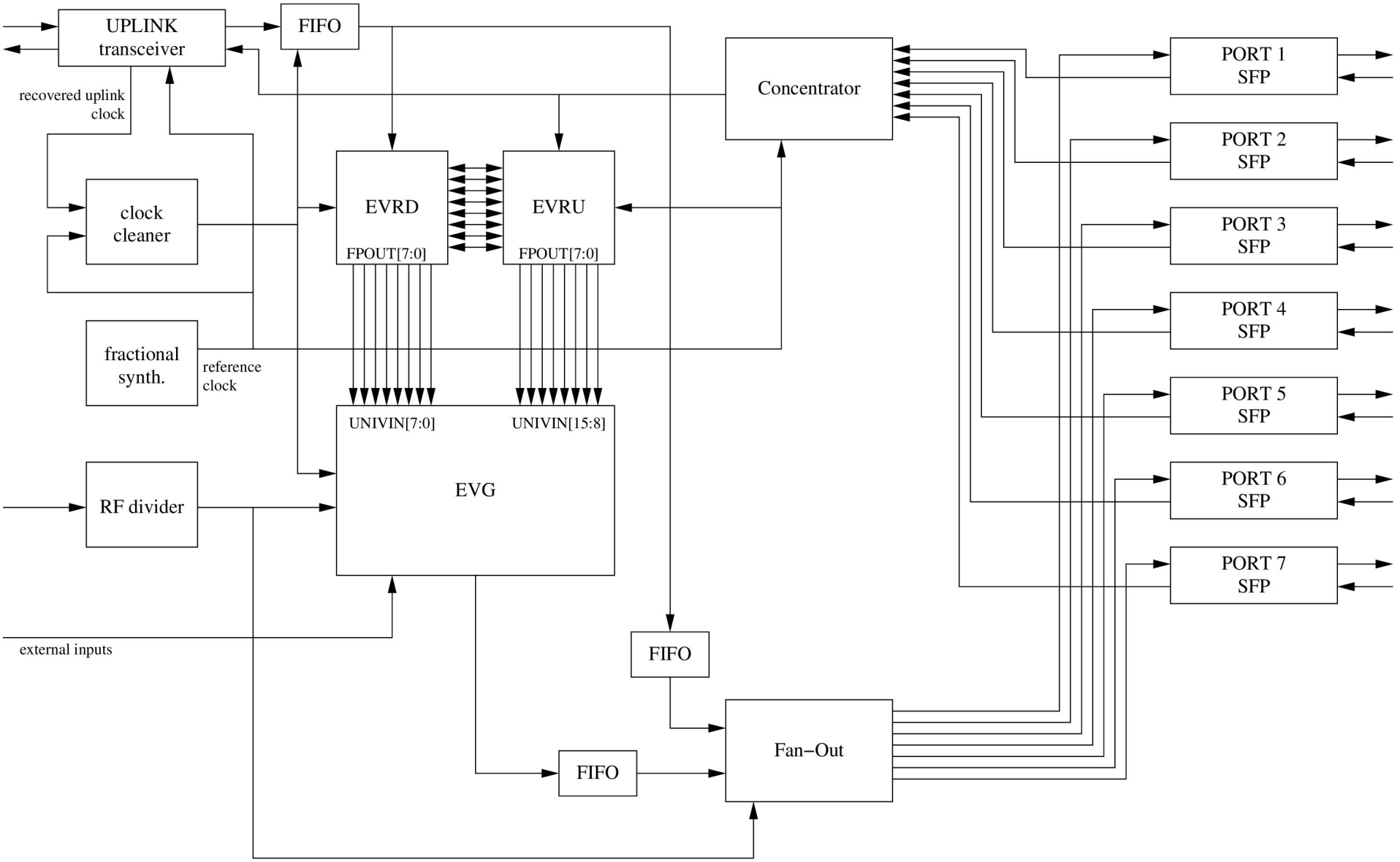
MTCA.4 Event Master in Development

- Event Generator (EVG)
  - 2 sequencers with maskable events
    - Max. 2047 events/sequence
    - 32 bit timestamp
  - 8 multiplexed counters
  - data buffer up to 2k bytes
  - segmented data buffer
    - 127 segments, 16 bytes each
- 7-Way Fan-Out/Concentrator (optionally additional 4 backplane point-to-point ports)
- Two Event Receivers (EVR)
  - 8 internal pulse outputs
  - one sequencer
- Event rate conversion (with some data buffer related limitations)
- Limited front panel size compared to VME
  - RF input
  - TTL input
  - Option for RTM
- I/O on backplane shared bus lines

MTCA.4 Event Master PCB Layout

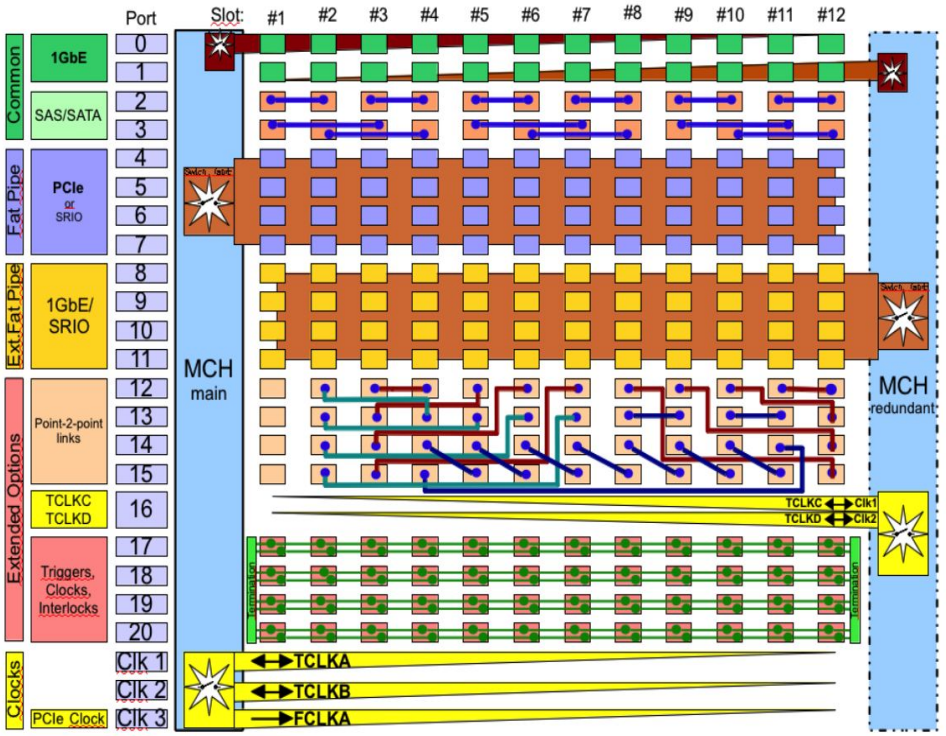


mTCA-EVM-300 Block Diagram



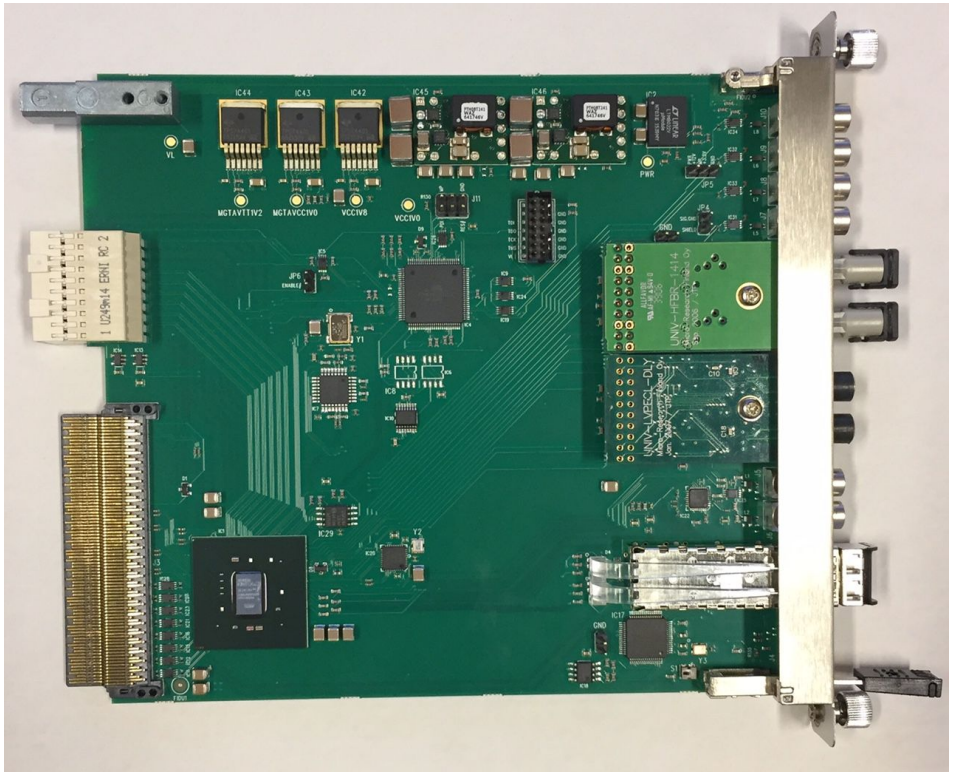
MTCA.4 Event Master

- Possibility to use backplane point-to-point links (port 12-15) for additional fanout ports or to connect other devices that will decode event stream by themselves
- MRF has plans to release an open source version of the Event Receiver

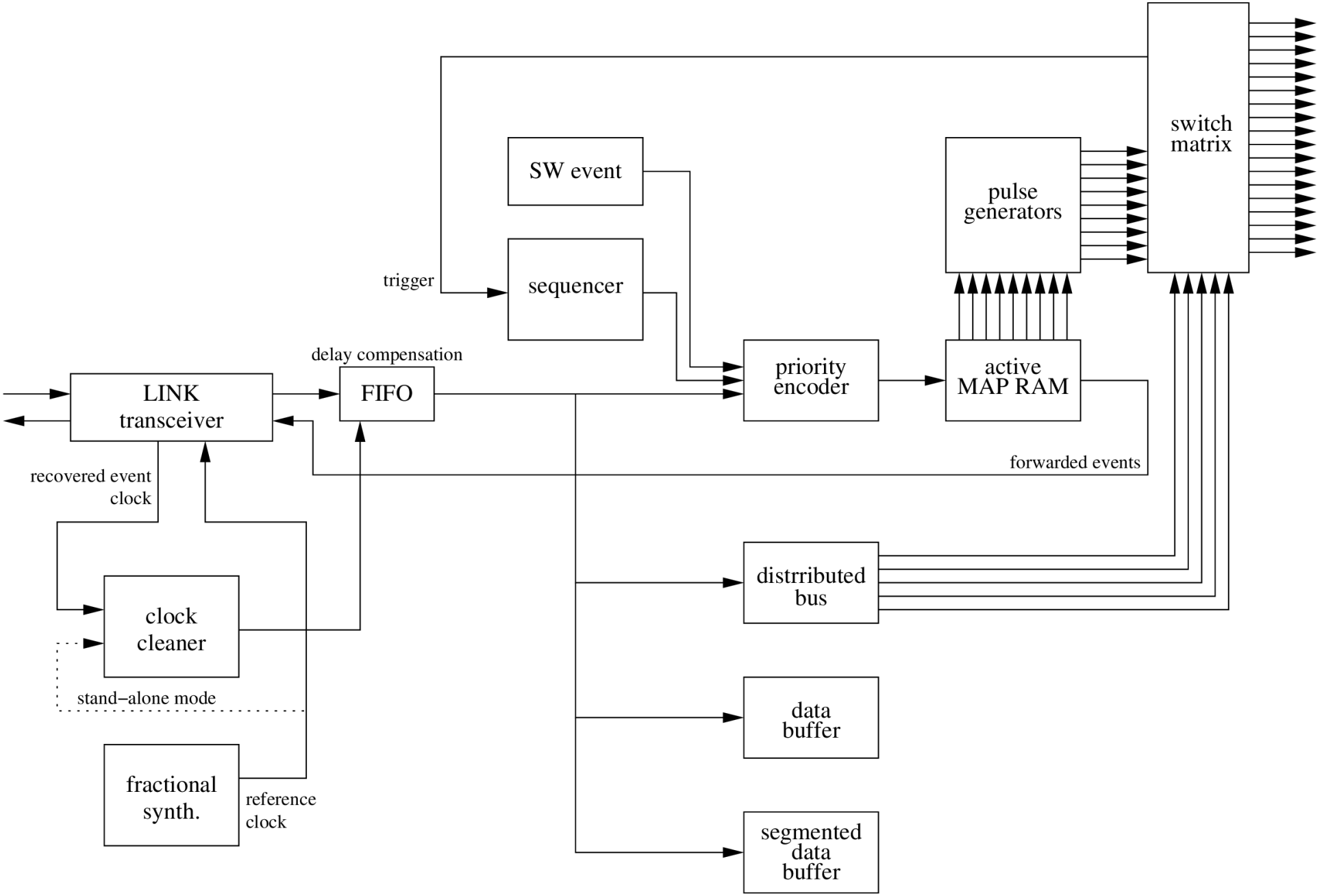


MTCA.4 Event Receiver mTCA-EVR-300U

- Two Universal I/O slots in front panel
  - Due to offset of front panel the distance between PCB has to be reduced using 8 mm spacer instead of a earlier used 10 mm spacer
  - Usable but fit is not perfect, also filler panel mounting suffers from a reduced front panel thickness



EVR Simplified Block Diagram



Universal I/O Modules

- 25.4 mm x 52 plug-in units
- two outputs or inputs each
- Module specification available on-line for custom module development

Optical HFBR-1414

820 nm

Optical HFBR-1528

650 nm
1 mm POF

NIM Output

LVTTL Output

TTL Input

LVPECL Output

LVPECL Output

10 ps step
Delay
tuning

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