Design of SLAC ATCA Accelerator Control systems for LCLS-II

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U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

The ATCA Common Platform

Developed at SLAC for high performance distributed control systems

Based on the Advanced Telecommunications Computing Architecture (ATCA)

- Growing multi-billion dollar market
- Continuously improving technology

High density, backplane carries all global signals

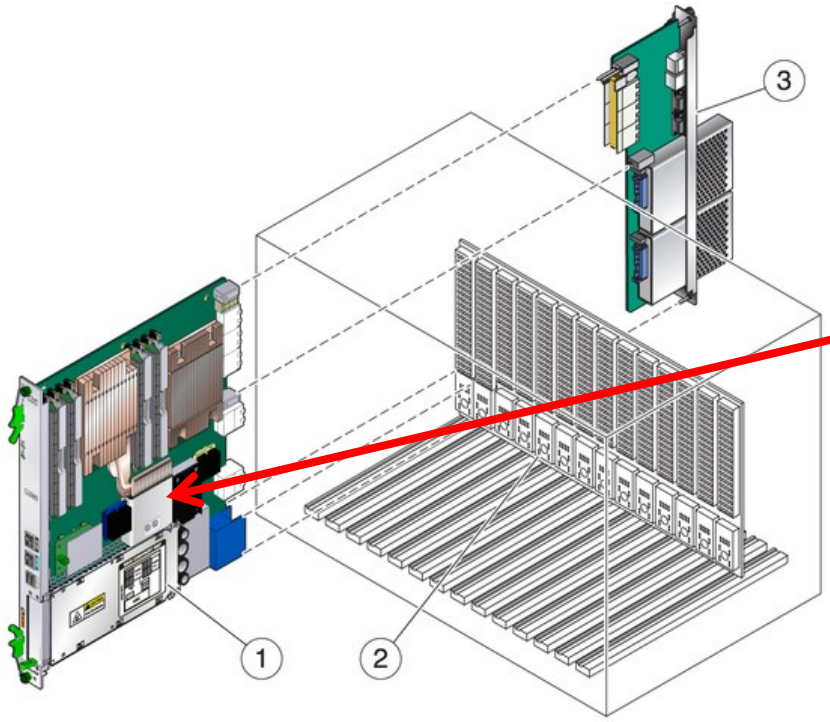
ATCA Crate "shelf"

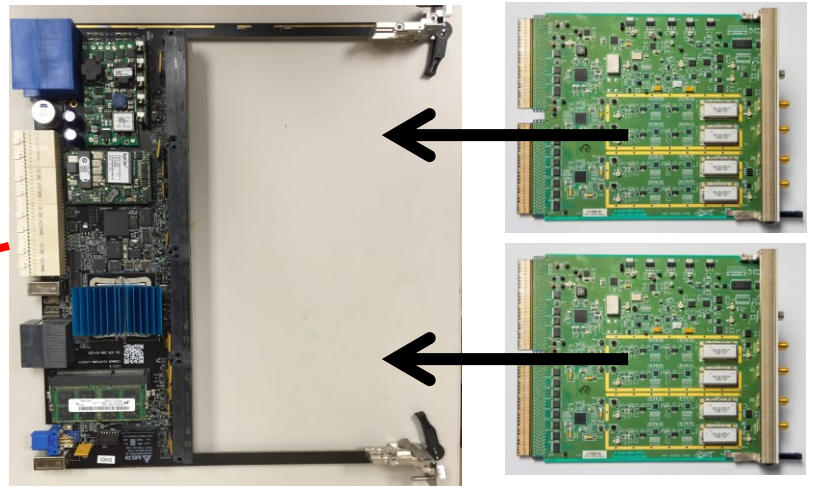
Standard hardware, SLAC application:

- Available from 1 slot to 16 slot
- Power supply with hot swap
- Management
- Networks
- Cooling
- Designed for high-reliability applications

Common Platform

SLAC hardware and software application on ATCA





1: Carrier Card
2: Crate
3: RTM
Each carrier supports 2 AMC application cards

Carrier card: FPGA, memory, backplane connections

AMC cards: ADCs, DACs, high performance front end electronics

RTM: General purpose IO, extra networks, miscellaneous

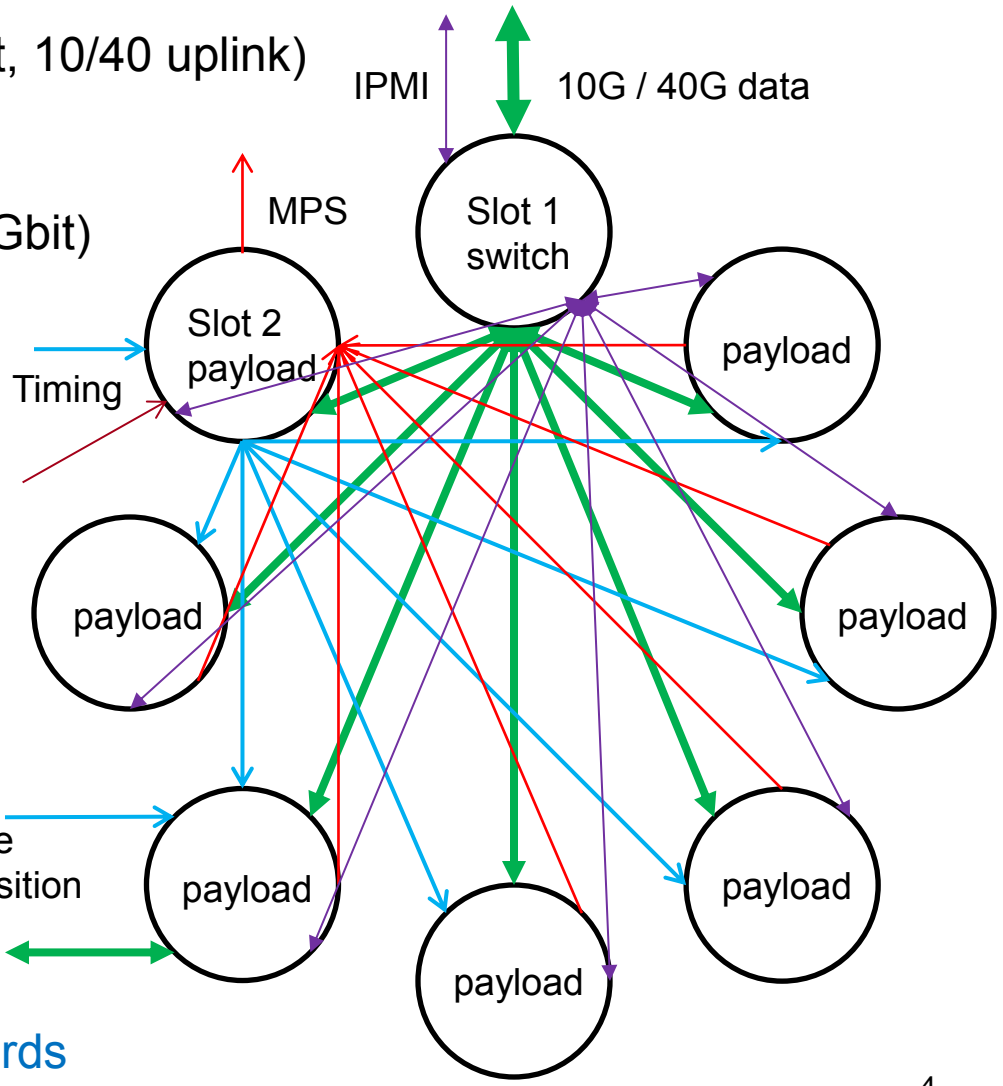
ATCA Backplane
(As used in SLAC Common Platform)

Ethernet for data / control (10Gbit, 10/40 uplink)

Timing data stream (3.75Gbit)

Machine protection / uplink (1.25Gbit)

IPMI management network



All carrier cards can also serve as slot 2 nodes

For most applications, all networks are carried on the backplane, minimal external connections

Single cards can be used with rear transition module networking

Crates available from 1 to 16 cards

More on Backplane Networks

IPMI provides control to power cycle and hot-swap individual cards.

- Operates independently of FPGAs on carrier cars.

Ethernet network used for normal control and data.

- 10Gbit to each card from switch
- 10 or 40Gbit uplink to main network

Timing data stream provides synchronization

- Each carrier card decodes the data stream to generate internal or external triggers. Multiple data streams supported:
  - Micro-Research “event receiver”
  - SLAC LCLS-II “timing system”
  - Straightforward to support other serial timing systems

Machine Protection / uplink

- Used at SLAC LCLS-II to provide an independent uplink path for interlock data.
- Available for other real-time uplink use if MPS is not required

For typical applications there is one set of networks connected to the crate, but no networks to the individual cards

Carrier Card

AMC ADC/DAC cards

DRAM

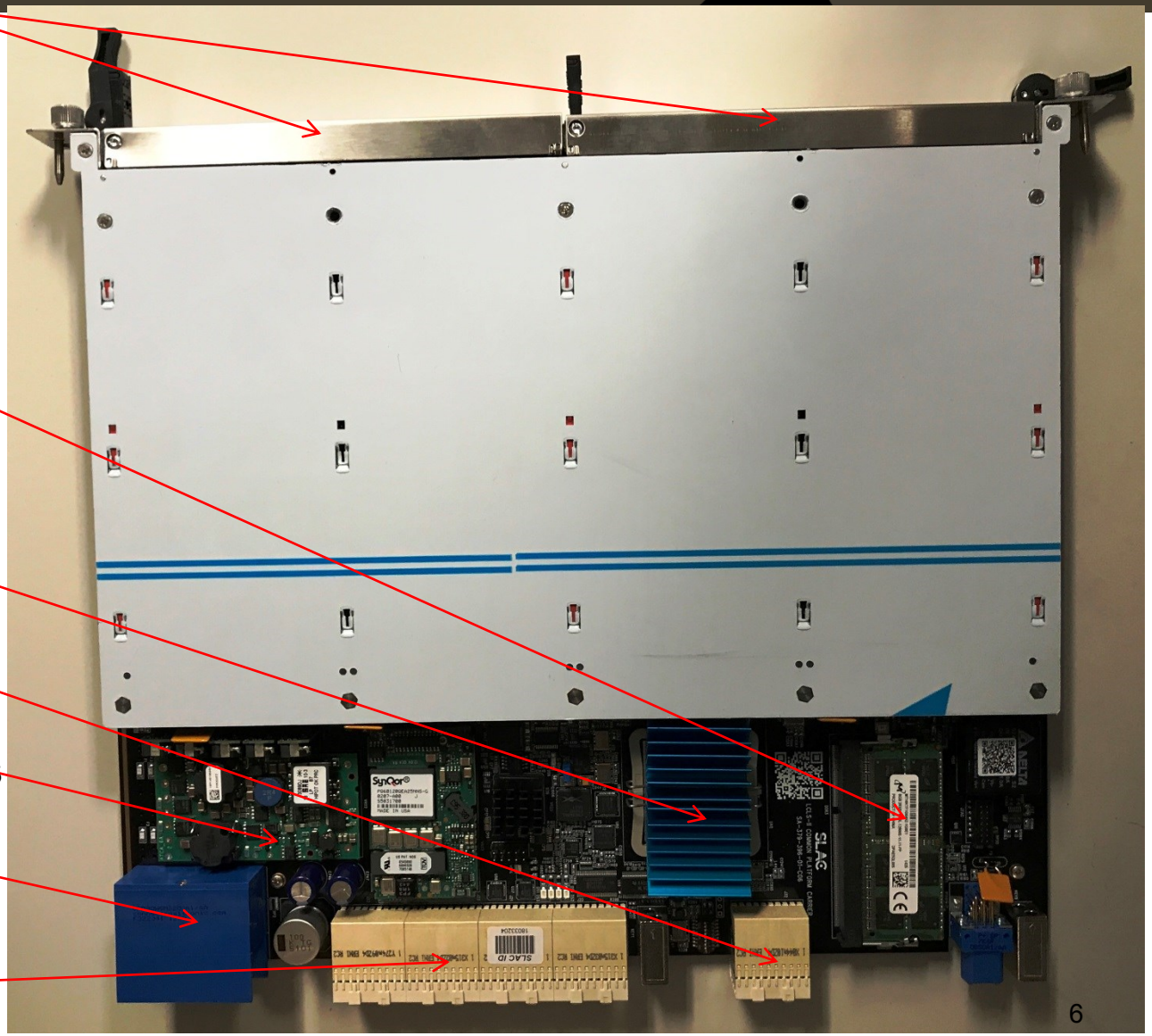
FPGA

Connector to RTM

Power supplies for AMCs

Power connector

Connector to backplane



Carrier Card

Xilinx “Kintex Ultrascale” FPGA

- KCU040 or KCU060: 2760 DSP slices, 200Gbit bidirectional bandwidth for ADC / DACs

Power supplies for AMC cards

- +3V, +4V, +/- 6V, +/-15V, +12V (9A)
- No switching supplies required on AMCs for most applications

8GB DDR3 memory (in addition to 3MB on-chip fast memory)

Supports Common Platform networks and management

Carrier card is very complex but a single design is used for all applications

AMC Cards

AMC = Advanced Mezzanine Card

ATCA double width, full height AMC card.

- Fully backwards compliant with AMC standards, with additional features
- Full height card provides space for RF shielding and daughter cards

Combined ADC / DAC and analog front end

- ADC/DAC requirements usually tied to a specific front end design
- Analog engineers can work independently of digital engineers

A variety of AMC cards have been developed

- ADC/DAC, Loopback test, Beam position monitor, Parallel Digital IO, High speed serial IO, Precision trigger generator. Low level RF system, high performance ADC/DAC

Some example AMC cards shown on the next slides

General Purpose A-D / D-A card

4X 16 bit 370 Ms/s ADC
- TI ADC16DX370
- One channel for read back of timing system for precision synchronization (sub-sample)

2X 16 bit 370Ms/s DAC
- TI DAC37J82

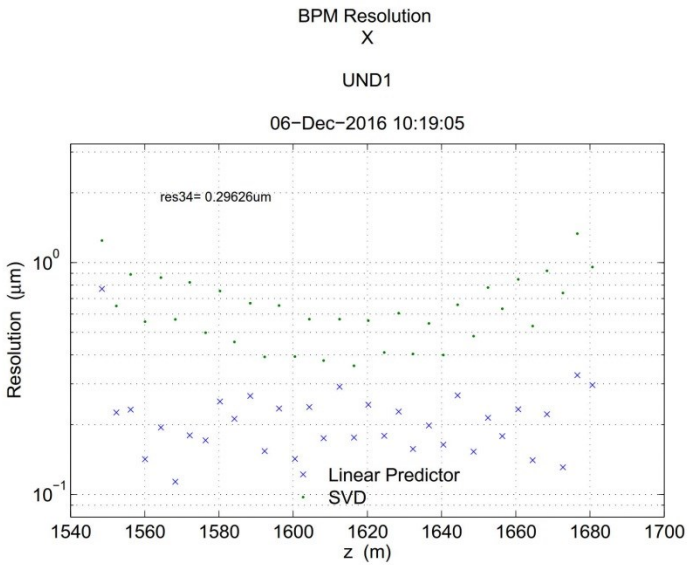
ADC/DAC clock
- DAC driven VCXO for locked or unlocked operation
- Low phase noise clock oscillator

Fast trigger reference output

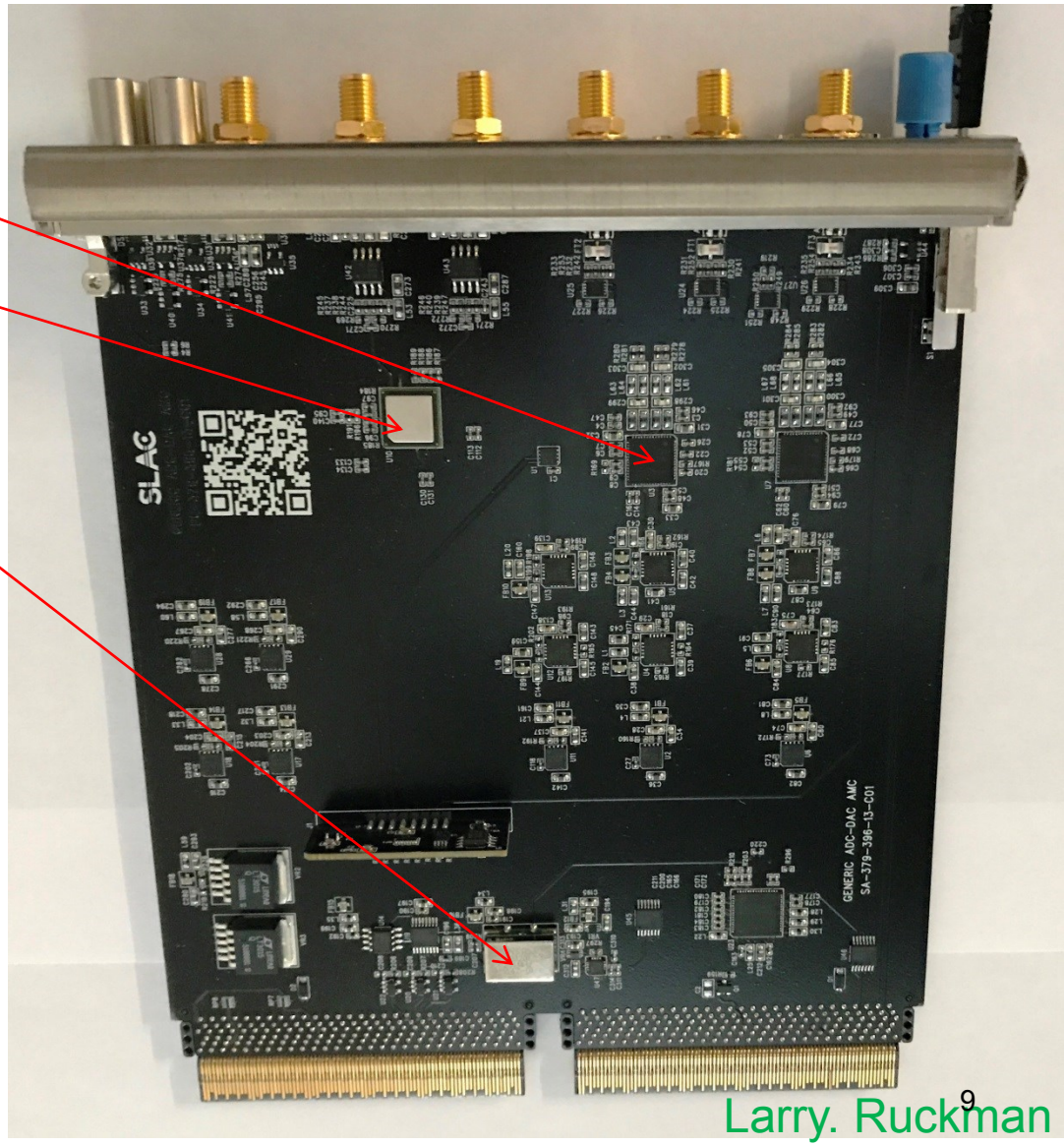
2X DIN, 2X DOUT

Fiber output for triggering

Status: In Production



Used for 300nm resolution cavity BPMs



Larry. Ruckman

Stripline e-Beam Position Monitor

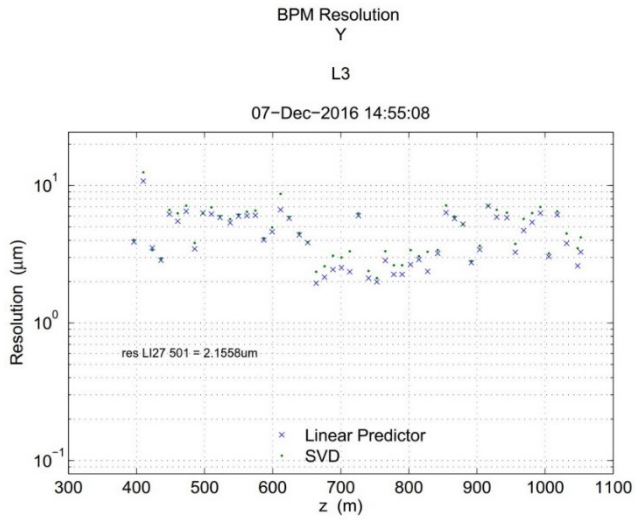
BPM signal processing

- 300MHz, 30MHz BW filters
- Distributed amplification /attenuation for high linearity
- 370Ms/s ADC

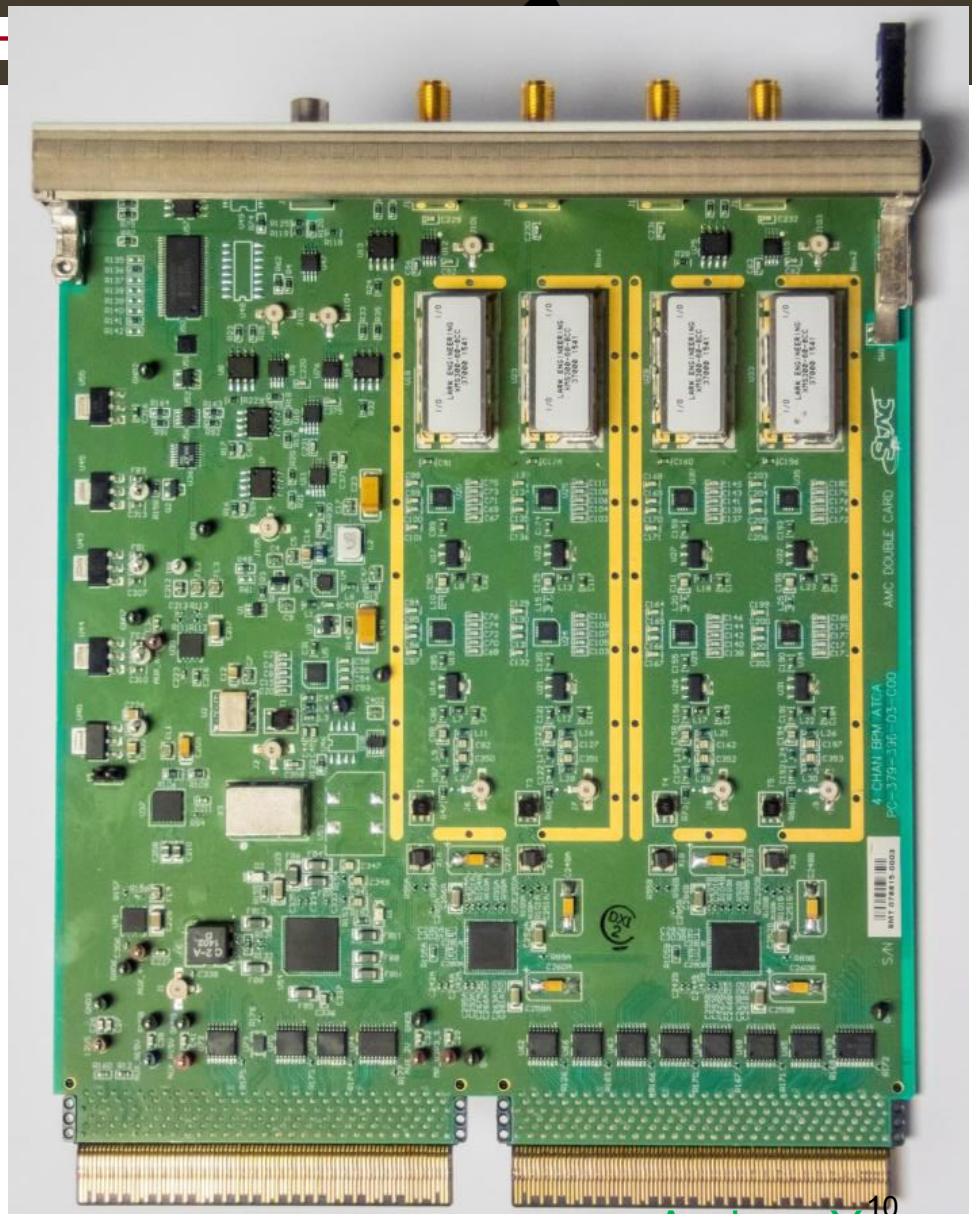
Calibration function

- Inject signals on BPM strips
- Measure induced signal in perpendicular strips
- Corrects for cable and electronics drifts

Status: In Production



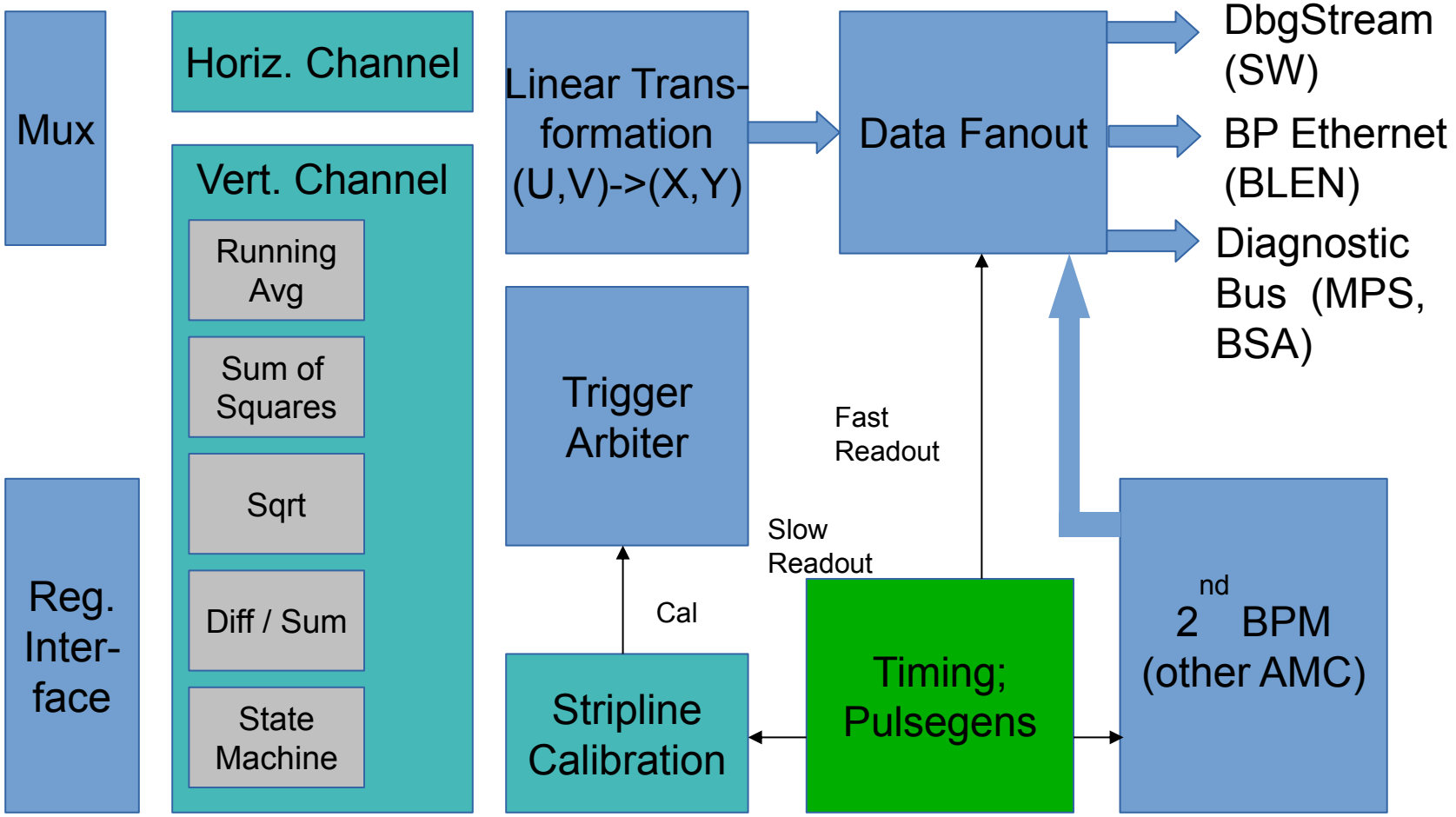
2 micron resolution at 180pC



RF shields removed for picture

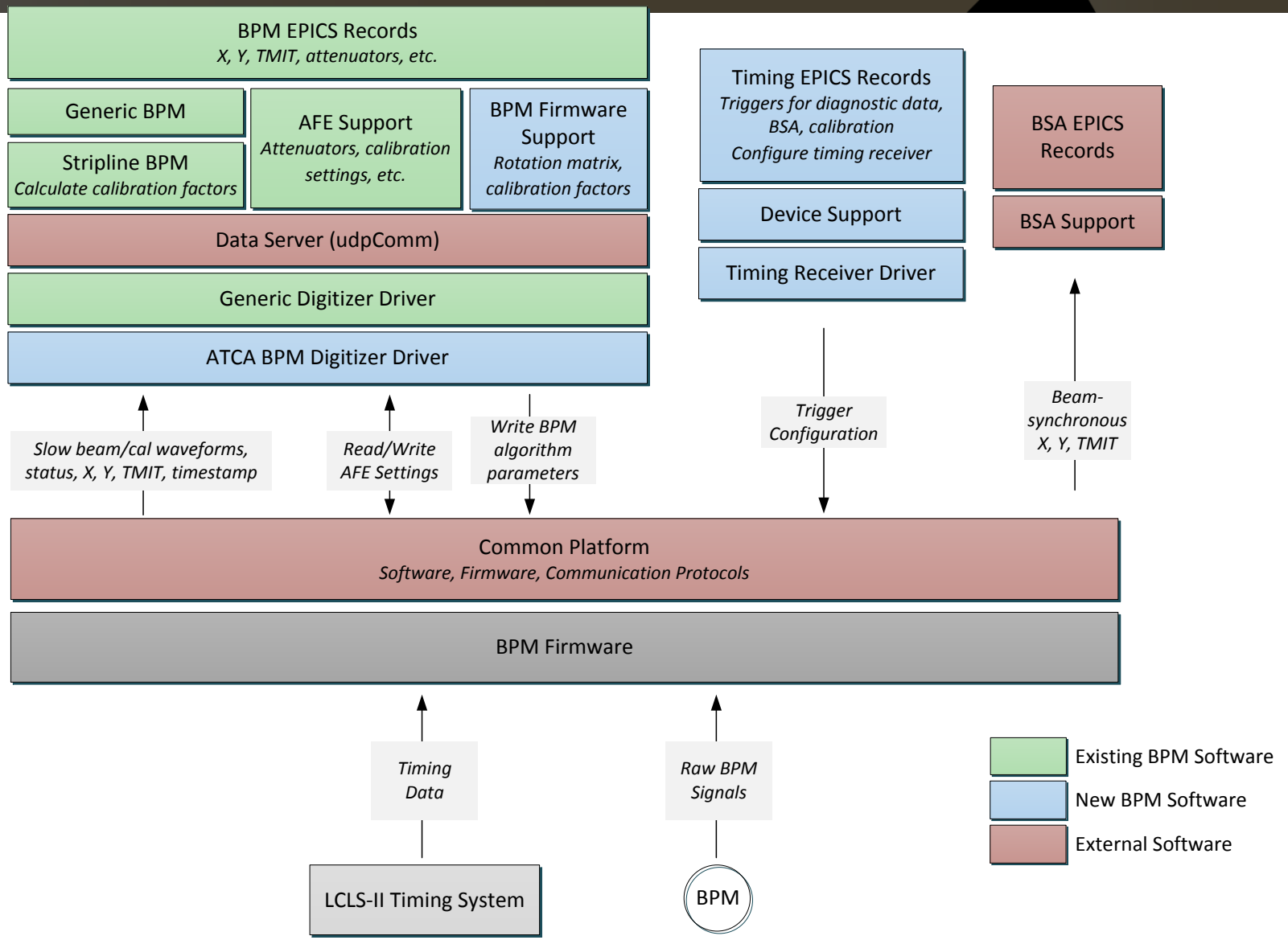
LCLS-II Injector Crate

LCLS-2 BPM Firmware Block Diagram

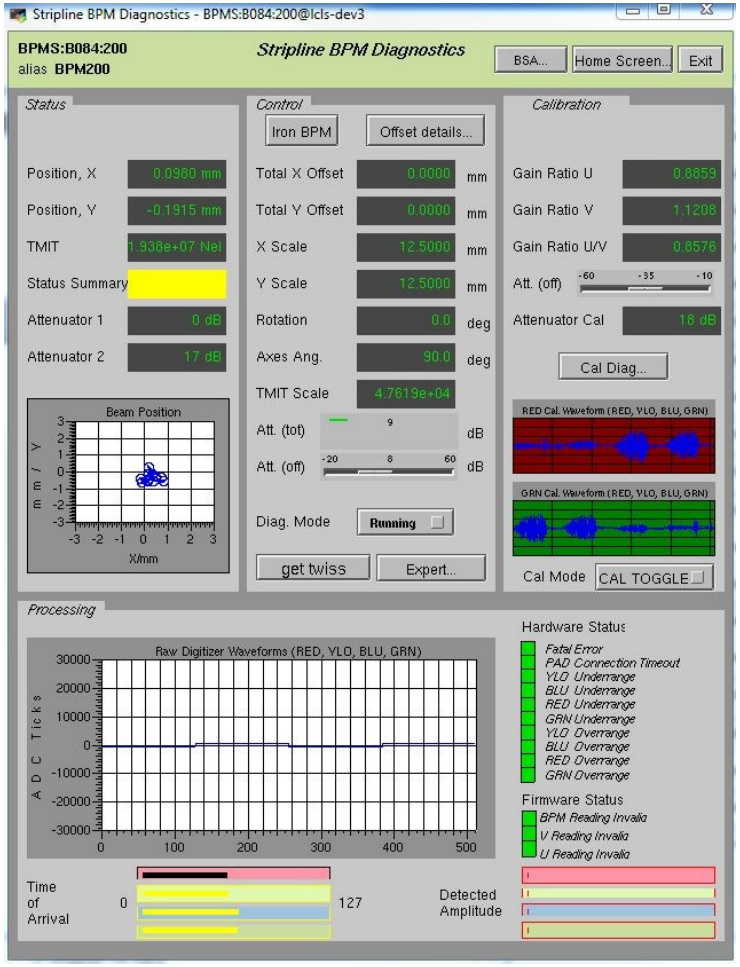


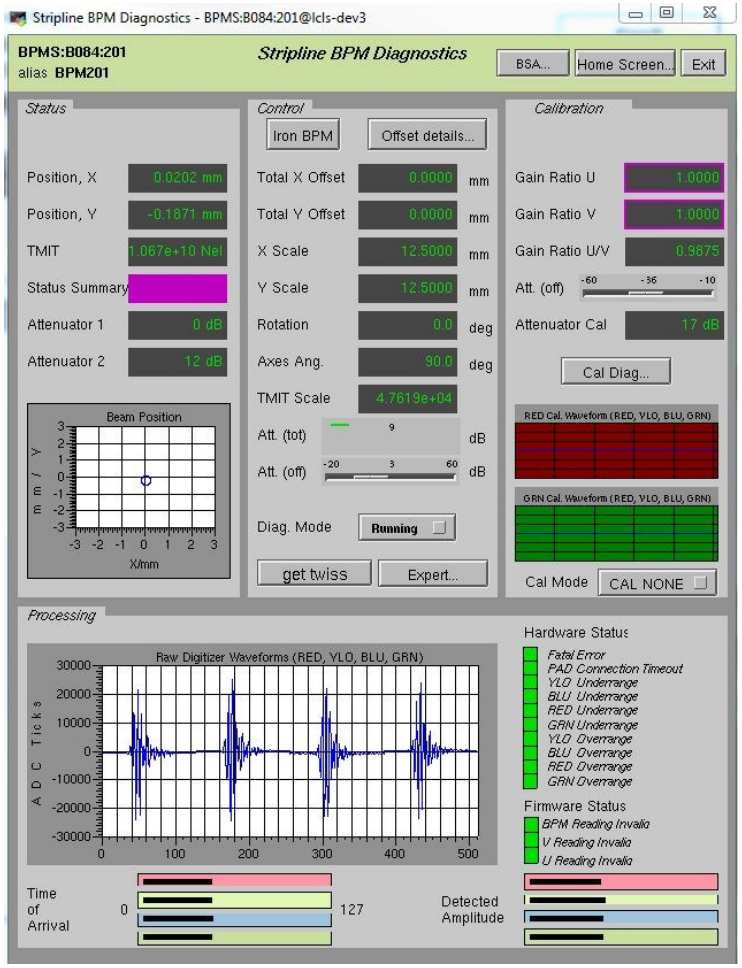
Stripline-specific; “pluggable” modules

BPM Software Architecture



EPICS Screens





Low Level RF Controller

2 AMC cards on a single carrier
- (receiver shown).

10X RF input channels

1X RF output channel

2X fast DC ADC (370Ms/s)

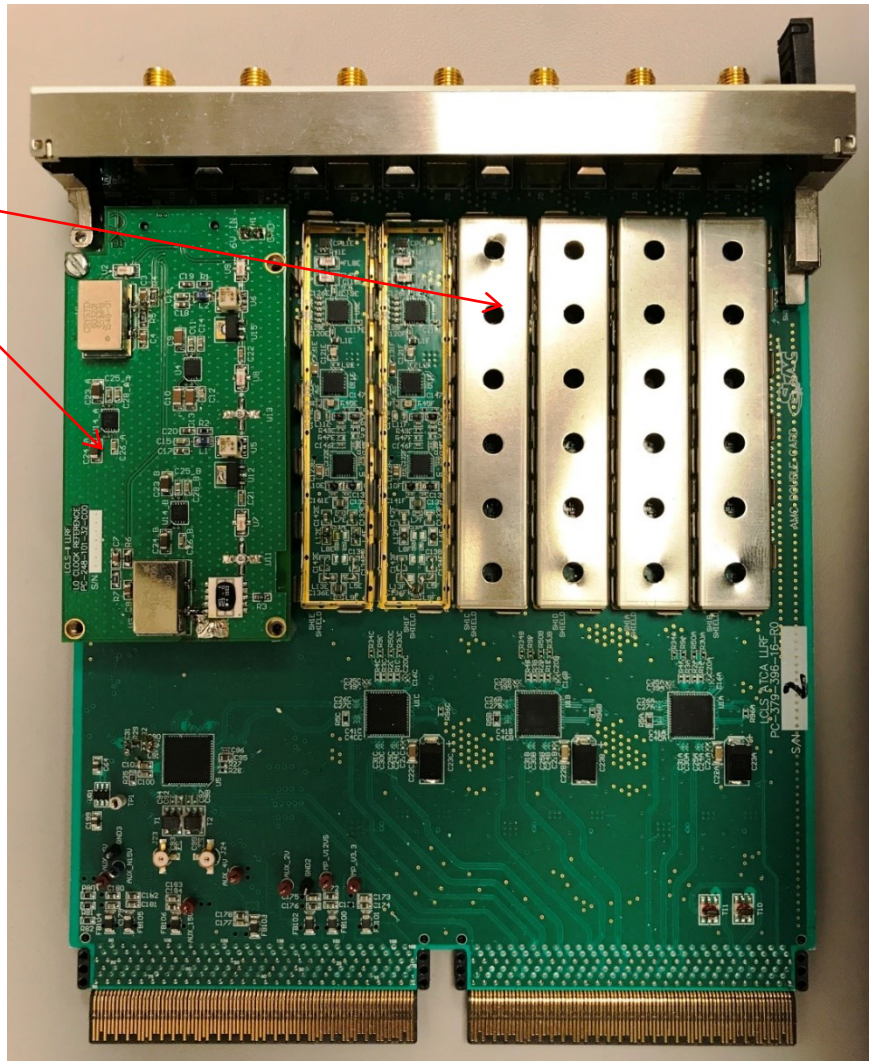
300MHz to 3GHz range with different oscillator daughter cards

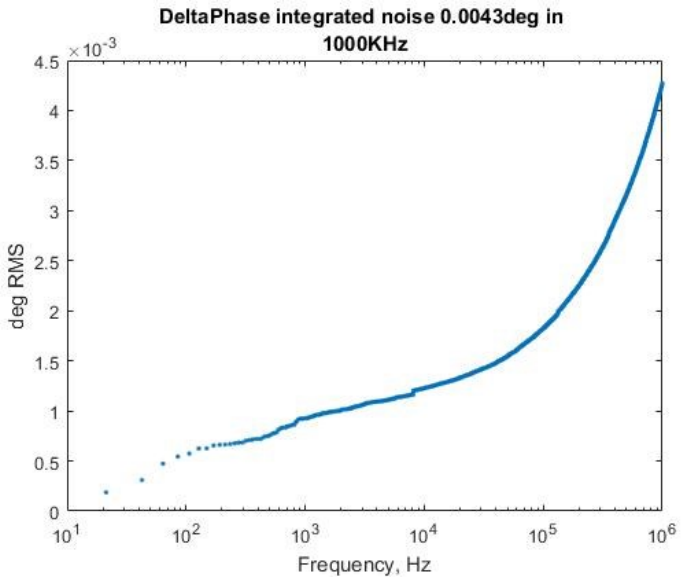
Clocks and LO phaselocked to timing reference system.

FPGA provides closed loop RF control.

Very low measurement noise
- 4.3 femtoseconds RMS in 1MHz bandwidth
- 1 femtosecond RMS in 1KHz bandwidth

Status: Operational





Dan Van Winkle

High Speed A-D / D-A

- 4X 2.5Gs/s 14 bit ADC, 4X 2.5Gs/s 16 bit DAC
- 200Gbit/s raw ADC / DAC bandwidth, reduced in ADCs / DACS to 100Gbit/s to the FPGA

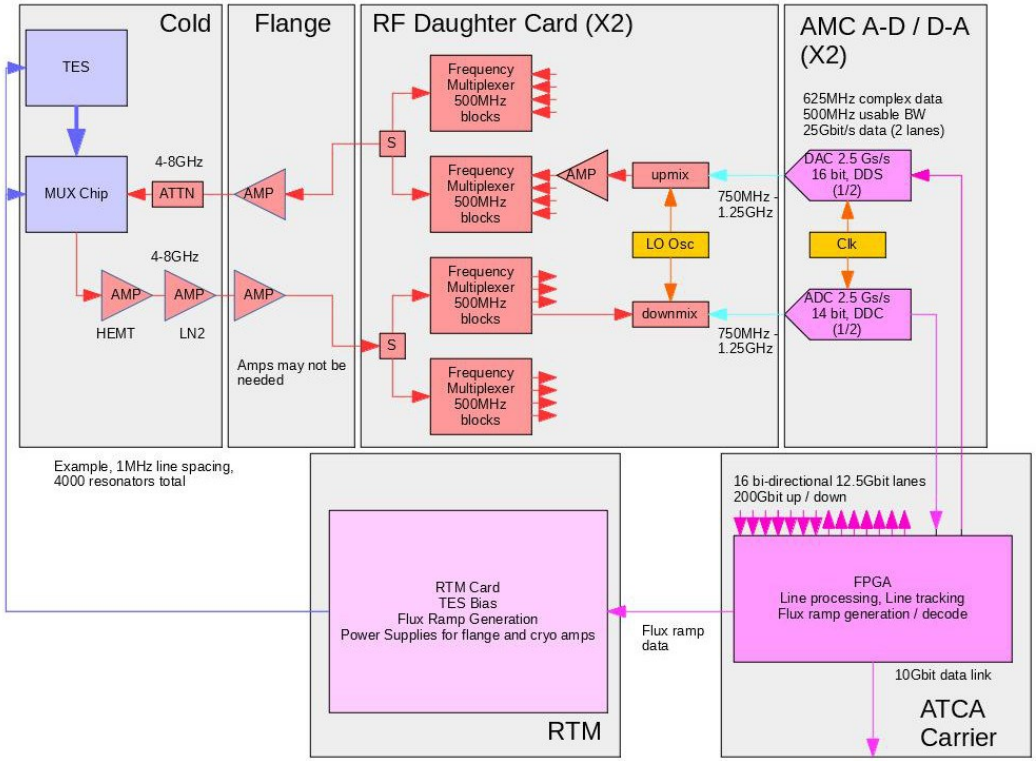
Designed for cryogenic sensor arrays (RF MUX SQUID / TES detectors) [Kent Irwin et. al.]

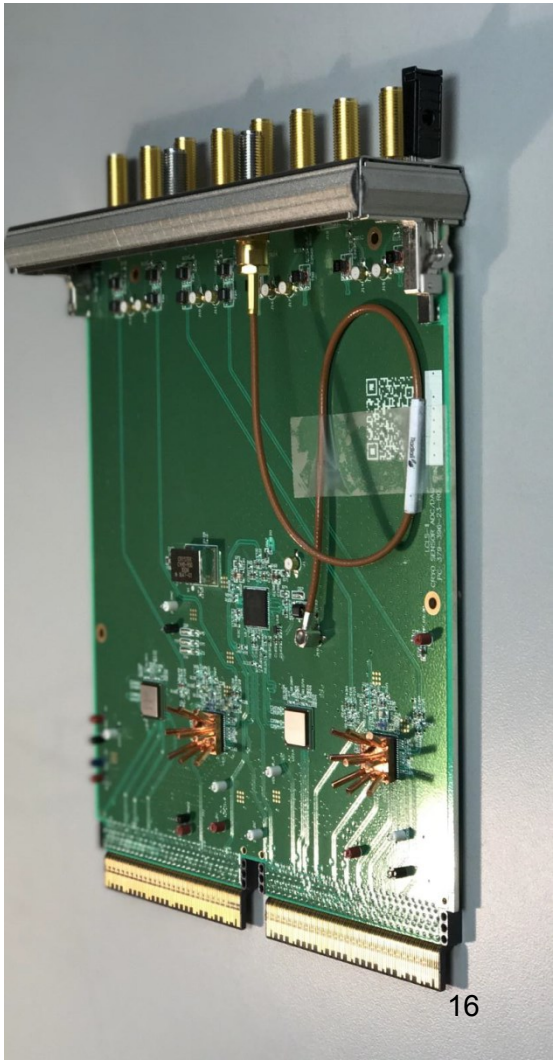
- Cosmic microwave background
- High energy resolution X-ray detectors

Designed to interface to RF daughter card

- RF multiplexing filters
- Synthesizers and mixers

Status: Testing 1st prototype





Rear Transition Modules

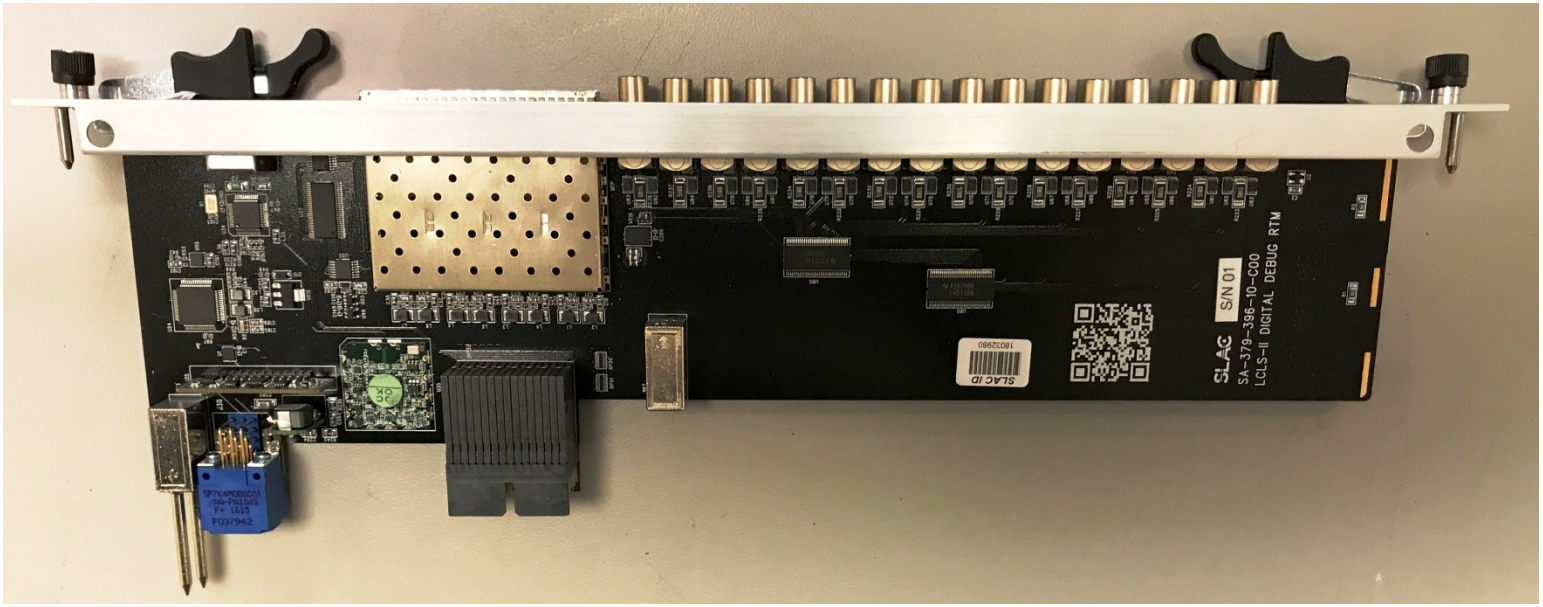
Direct connection to carrier card FPGA and to AMC cards

- 3X high speed serial lanes. 2X for network and timing data stream, 1 for on-board use
- Parallel digital IO to FPGA
- Digital IO to AMC modules – can be used for clocks or interlocking

Often contain simple programmable logic (CPLD) for interlocks that need to be independent of the main FPGA code for high reliability operation.

Several variants for different applications.

- Digital IO, laser locker, low level RF, interlocks, trigger output etc.



ATCA Common Platform Projects

SLAC / LCLS Low Level RF upgrade

- 83 ATCA cards for SLAC LCLS operations
- Additional for SPEAR ring and FACET2 accelerator

SLAC LCLS-II, Instrumentation

- Cavity BPMs, stripline BPMs, bunch length monitor, bunch charge monitor, machine protection, beam loss monitors
- Approximately 500 ATCA cards

Cosmic microwave background telescope projects

- Approximately 100K sensor channels, 25 ATCA cards.

LCLS-II cryogenic X-ray sensor

- Approximately 10K high bandwidth sensor channels, 10 ATCA cards.

SLAC RF femtosecond timing system

- Laser locker, RF-over-fiber timing
- Approximately 30 ATCA cards