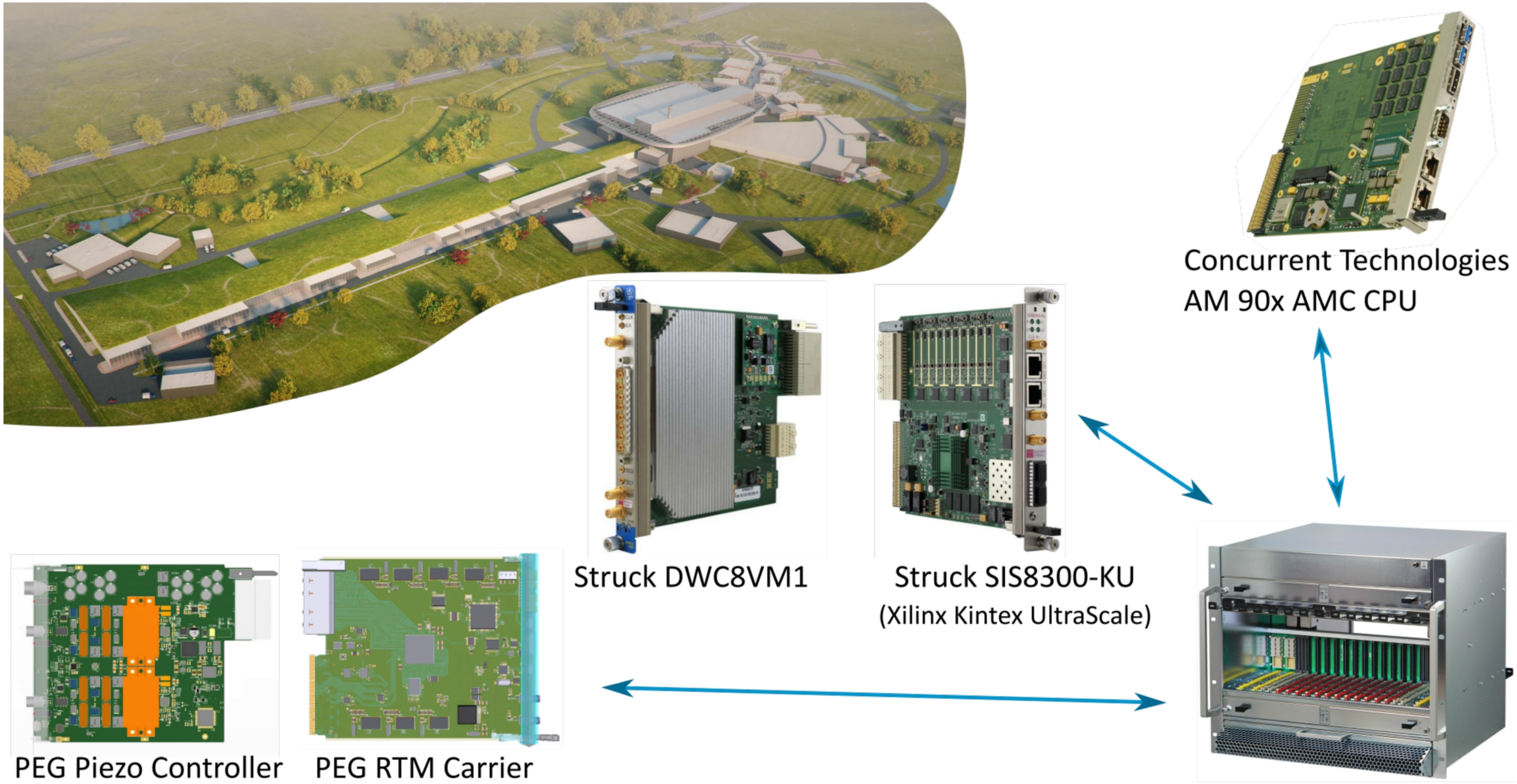
AXI4-based FPGA Framework for MicroTCA Boards

Christian Amstutz, Mehdi Mohammednezhad,
Maurizio Donna, Anders Johansson

www.europeanspallationsource.se

Example LLRF System at the ESS Linear Accelerator



Concurrent Technologies
AM 90x AMC CPU

Struck DWC8VM1

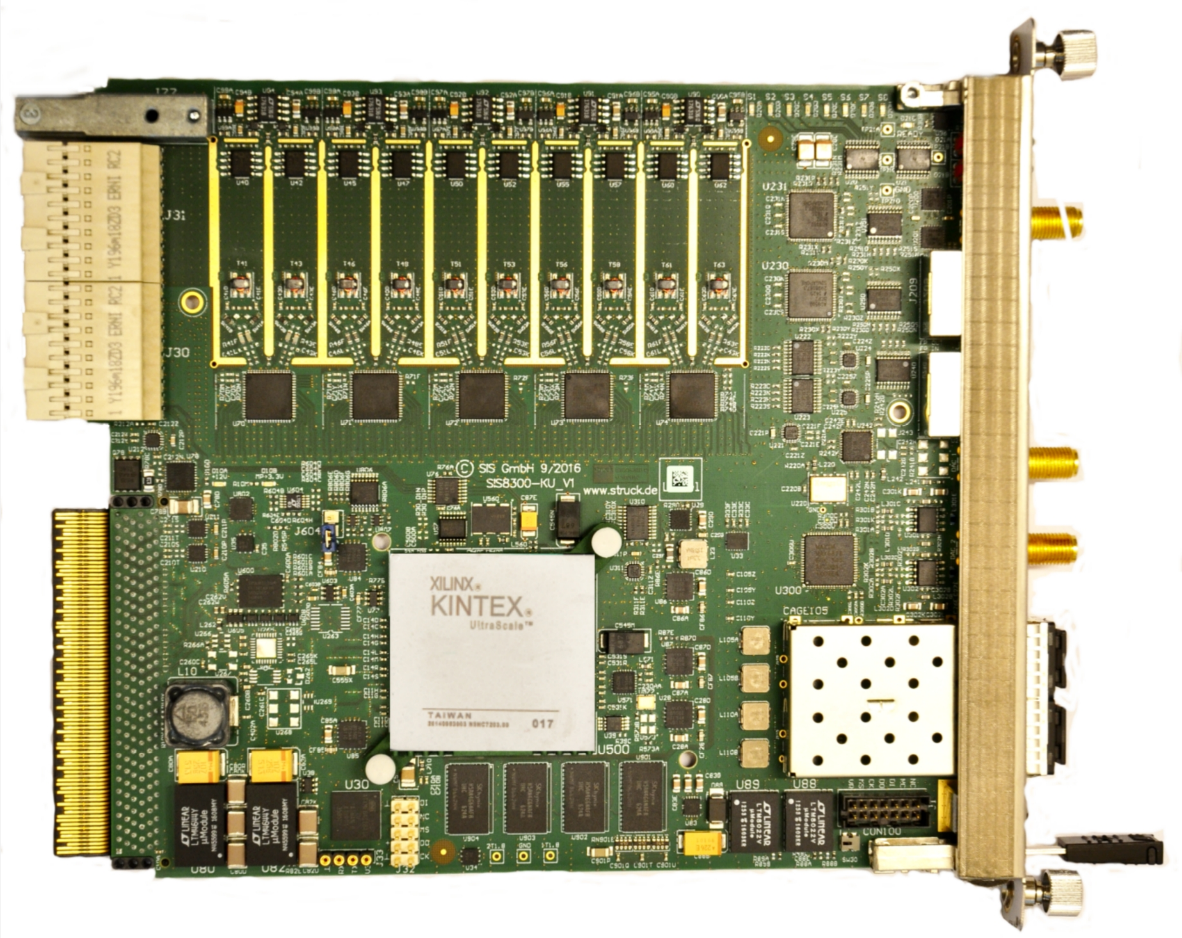
Struck SIS8300-KU
(Xilinx Kintex UltraScale)

PEG Piezo Controller

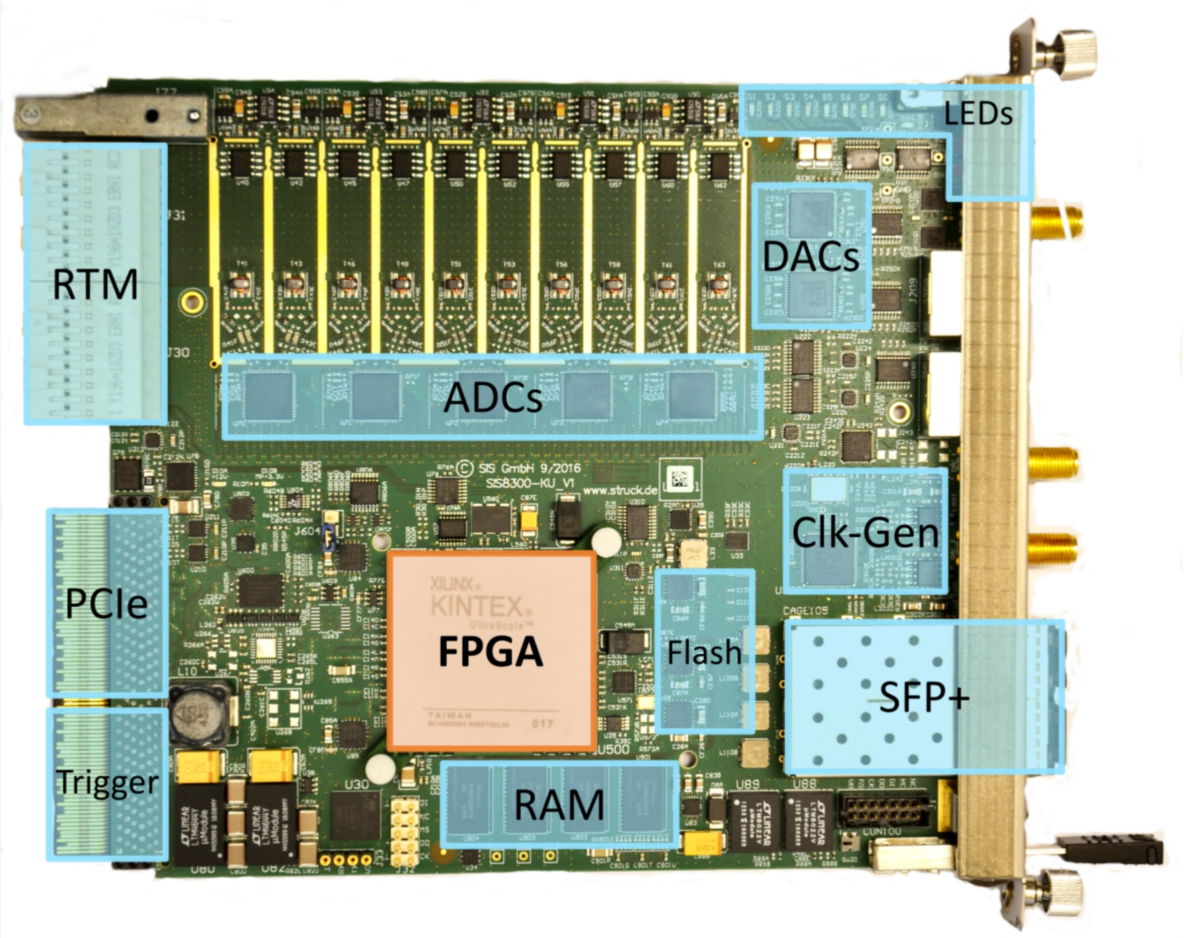
PEG RTM Carrier
(Xilinx Artix-7)

Schroff 12 slot MTCA crate

What does an FPGA Framework offer?



What does an FPGA Framework offer?



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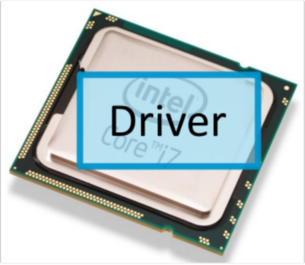
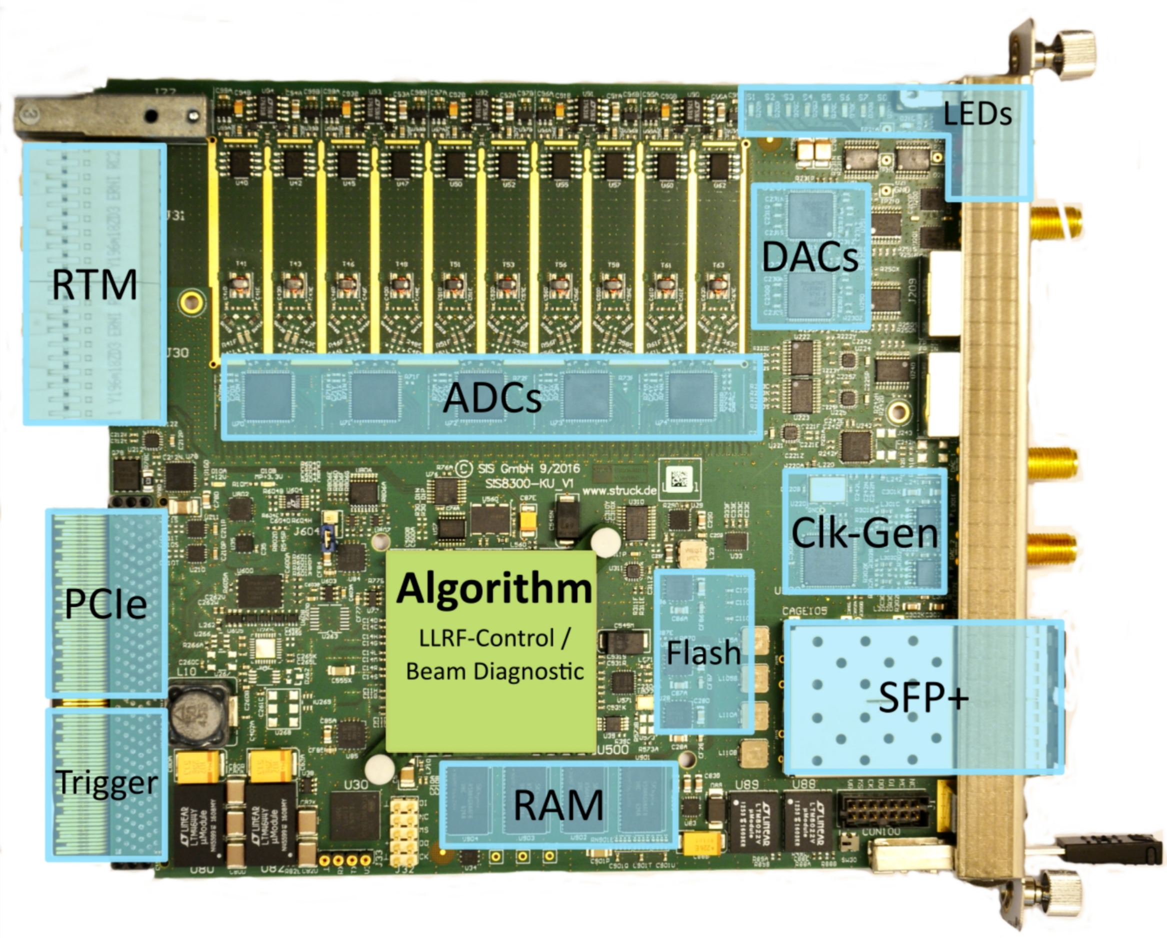
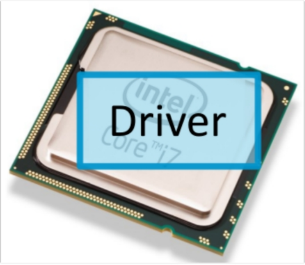
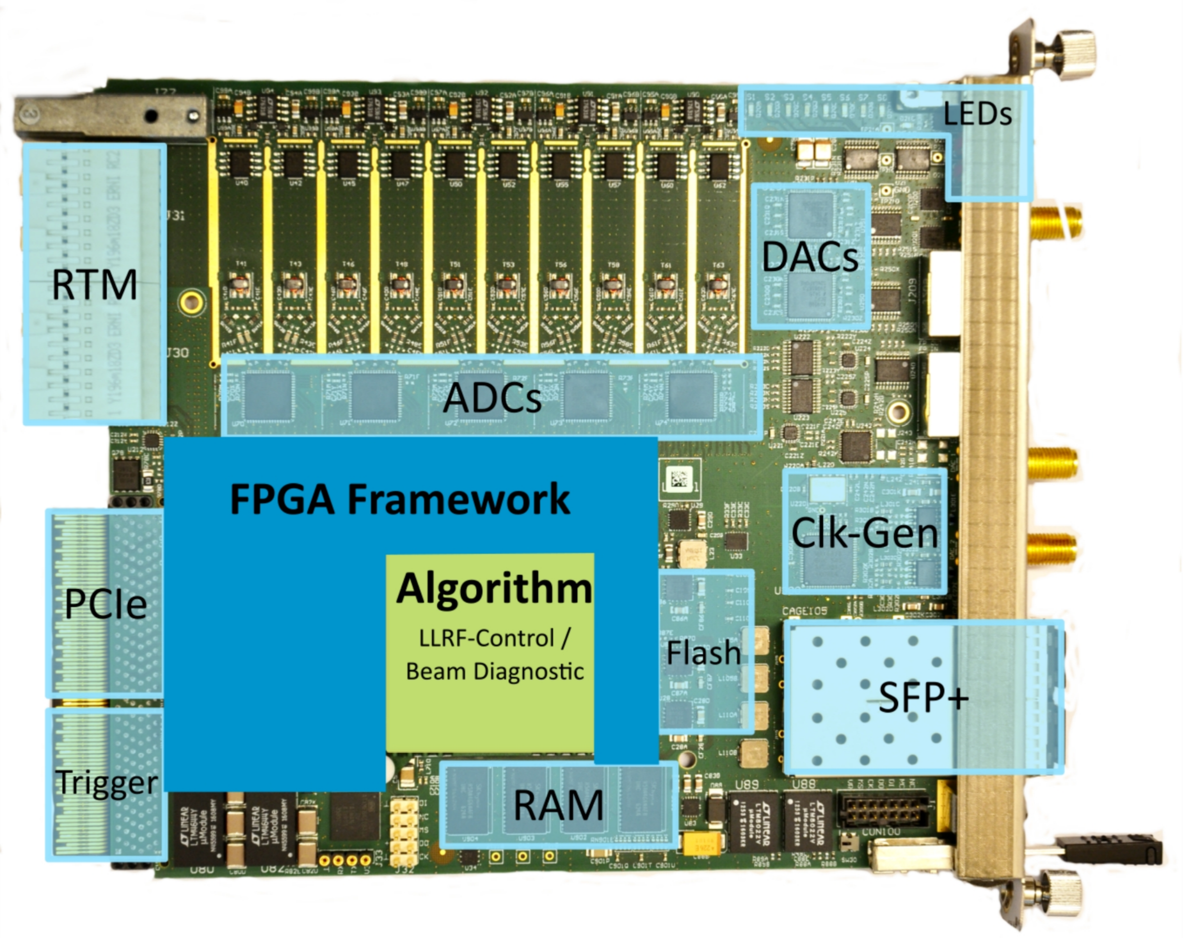




What does an FPGA Framework offer?





Concepts of the AXI4-based Framework

Flexibility

Different Boards / Different Applications

Long-term support

Reduction of dependencies of third-party code

Re-use of existing IP

Development of all code is expensive

Follow Standards

AXI4: Open standard from ARM for on-chip interconnects

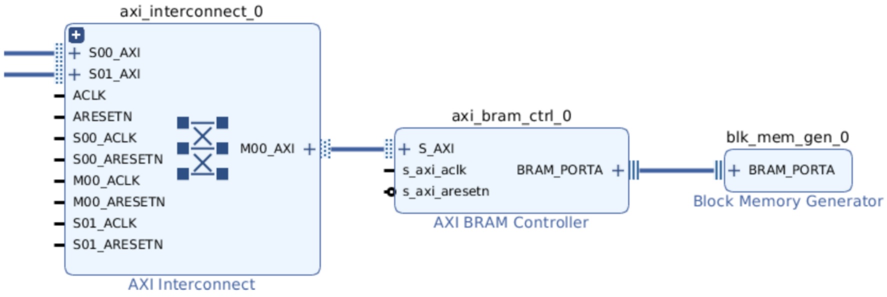
Integration into workflow at ESS

Replicate software workflow at ESS to firmware development

XILINX
VIVADO™

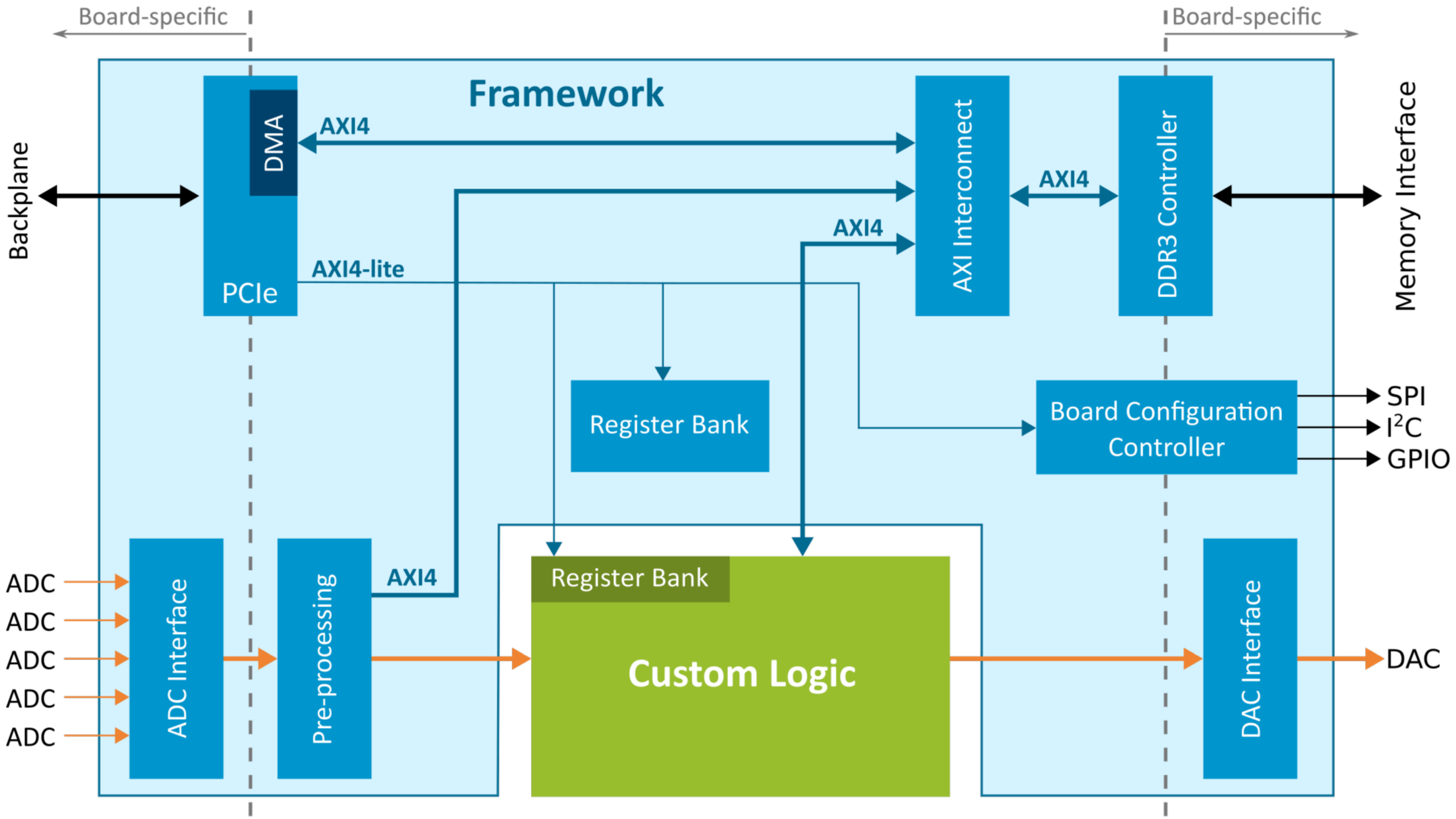
AXI4 Bus

- Part of the open-standard AMBA bus family from ARM
- On-chip interconnect: High bandwidth / low latency
- Highly configurable:
  - Read-only / read-write
  - Width of data lane
- 3 types:
  - AXI4
  - AXI4-Lite
  - AXI4-Stream



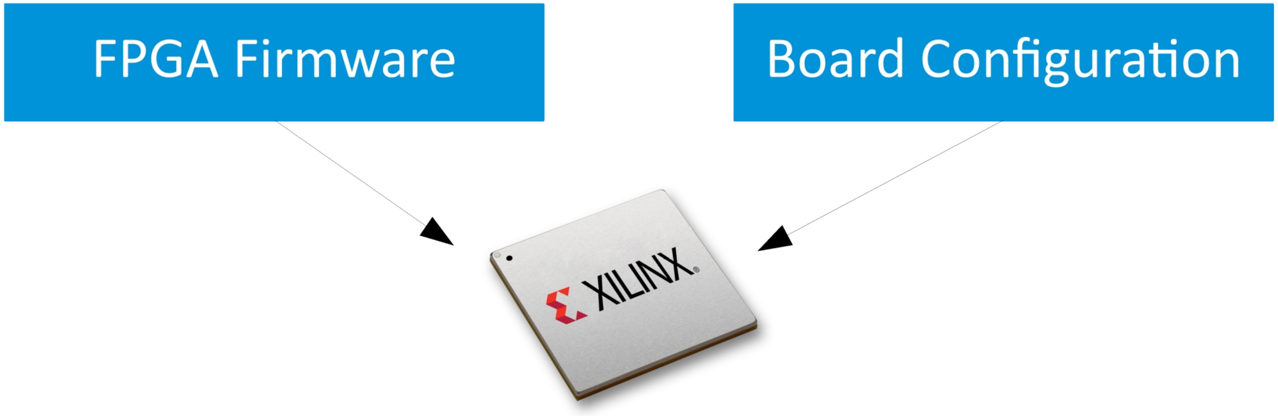
- Official bus in Vivado IP Integrator

Structure of the Framework



Configuration Controller – Concepts

→ Board Configuration is rather static for one application



FPGA Firmware

Board Configuration

Configuration Controller – Concepts

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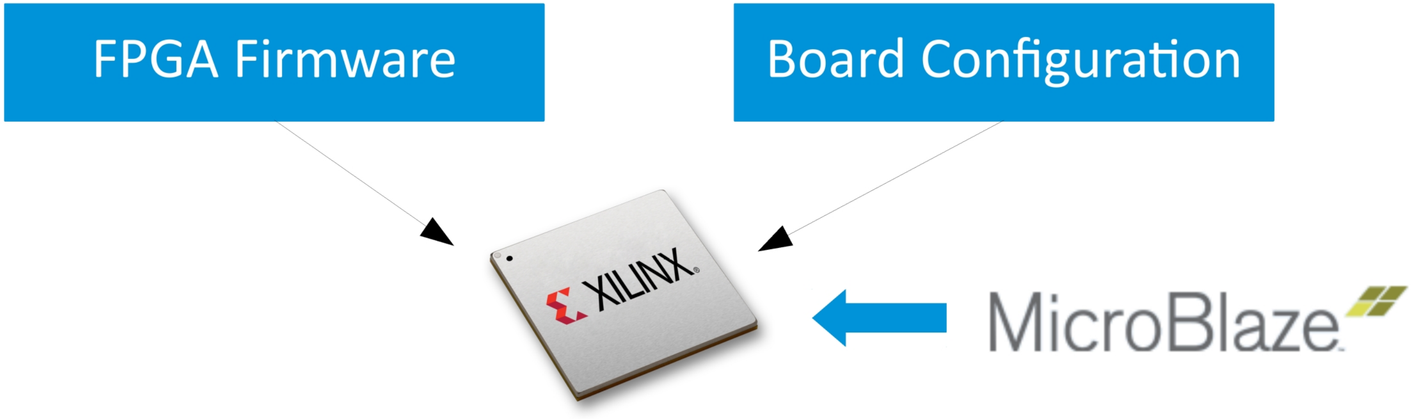
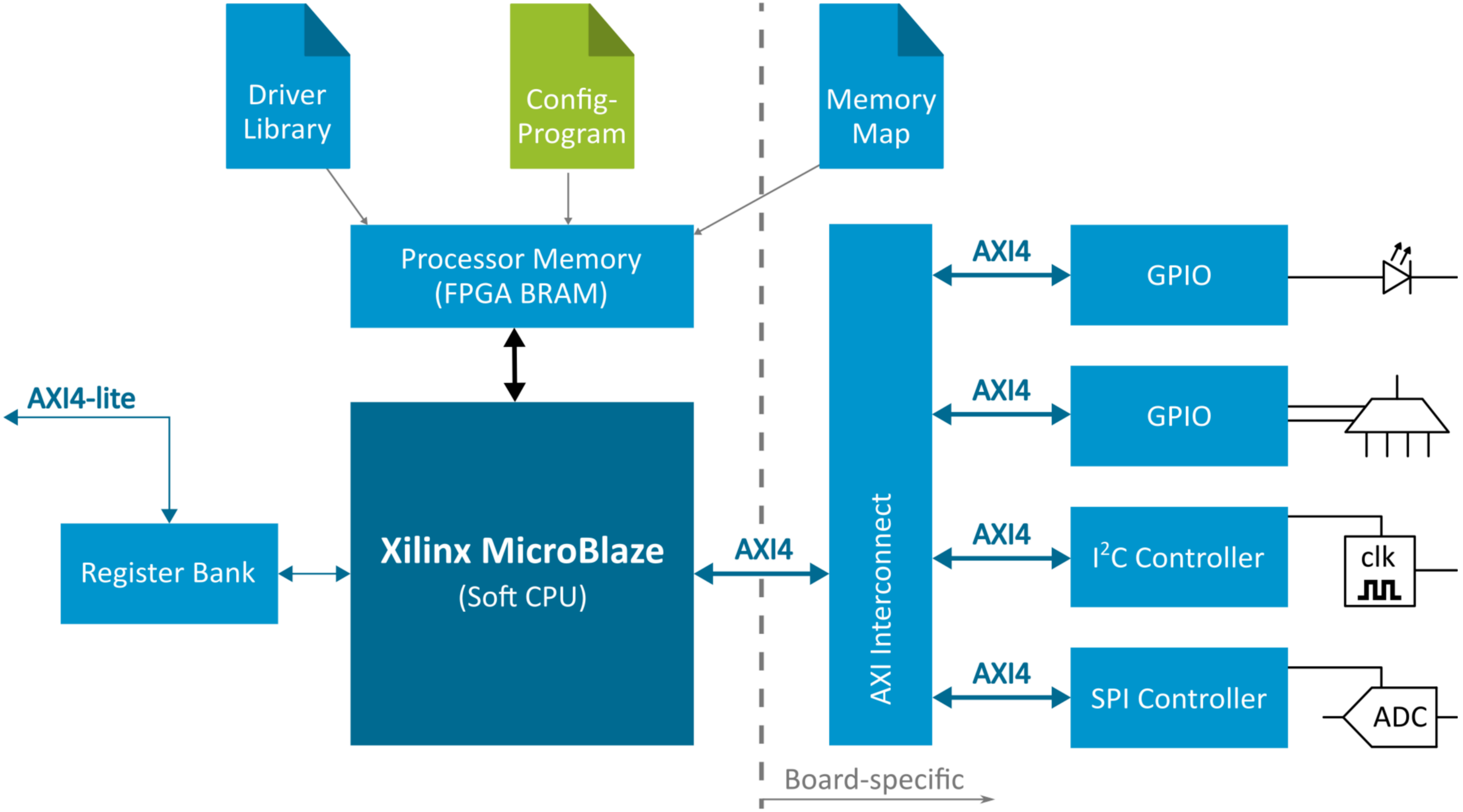


FPGA Firmware

Board Configuration

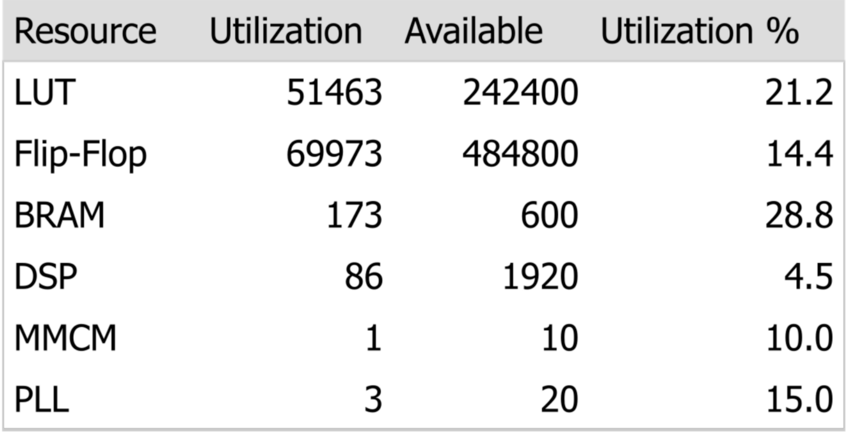
- Usage of Xilinx IP blocks for SPI, I2C, GPIO
- Adaptations to the serial protocols (SPI, I2C) made in software
- Separate board configuration from driver

Configuration Controller – Overview



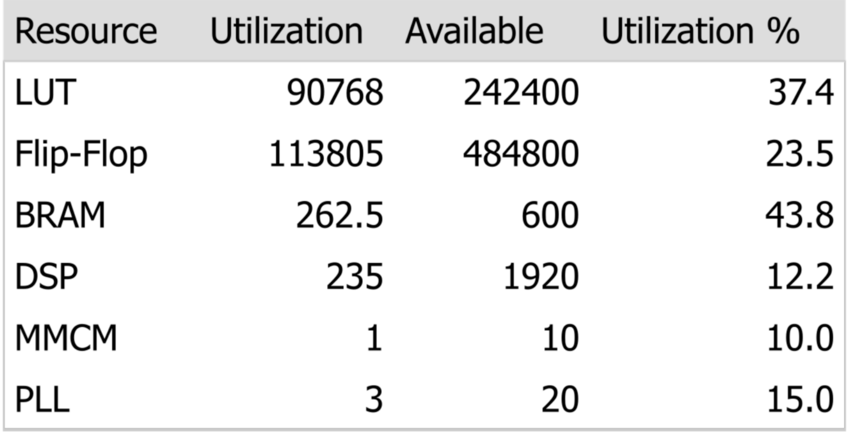
Resources

→ FPGA resources occupied by framework: ca. 20%



Resource	Utilization	Available	Utilization %
LUT	51463	242400	21.2
Flip-Flop	69973	484800	14.4
BRAM	173	600	28.8
DSP	86	1920	4.5
MMCM	1	10	10.0
PLL	3	20	15.0

Framework only



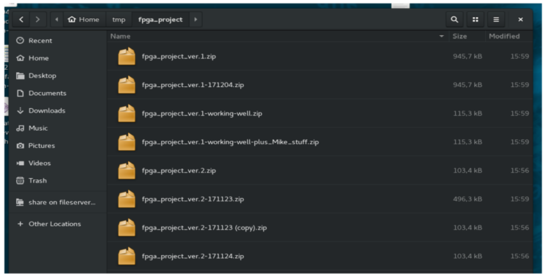
Resource	Utilization	Available	Utilization %
LUT	90768	242400	37.4
Flip-Flop	113805	484800	23.5
BRAM	262.5	600	43.8
DSP	235	1920	12.2
MMCM	1	10	10.0
PLL	3	20	15.0

Framework with LLRF application

(Device: Xilinx Kintex Ultrascale xcku040-ffa156-1-c, AXI4 bus: 512 bit @ 200 MHz, Tools: Xilinx Vivado 2017.1)

One repository contains everything

Code



Name	Size	Modified
fpga_project_ver.1.zip	945,7 kB	15:59
fpga_project_ver.1-171204.zip	945,7 kB	15:59
fpga_project_ver.1-working-well.zip	115,3 kB	15:59
fpga_project_ver.1-working-well-plus_Mike_stuff.zip	115,3 kB	15:59
fpga_project_ver.2.zip	103,4 kB	15:56
fpga_project_ver.2-171123.zip	496,3 kB	15:59
fpga_project_ver.2-171123 (copy).zip	103,4 kB	15:56
fpga_project_ver.2-171124.zip	103,4 kB	15:56

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git

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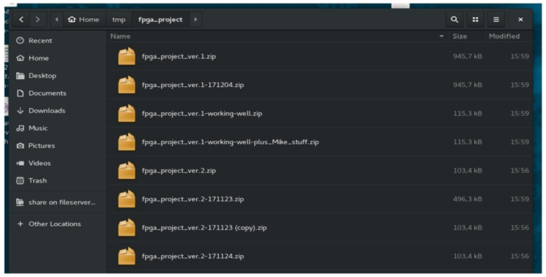
Code



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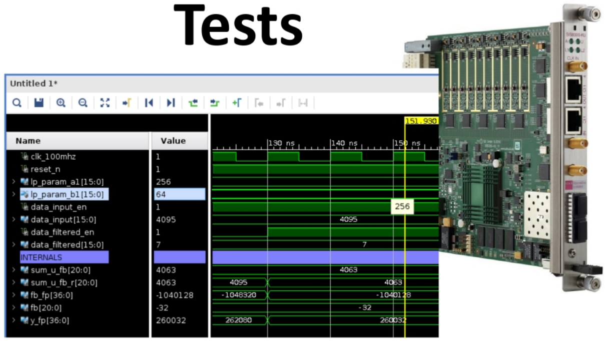
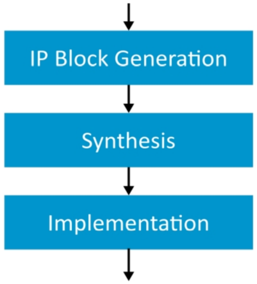
fpga_project_ver.2-171124.zip	103,4 kB	15:56

Tests



Name	Value
clk_100mhz	1
reset_n	1
lp_param_a1[15:0]	256
lp_param_b1[15:0]	64
data_input_en	1
data_input[15:0]	4095
data_filtered_en	1
data_filtered[15:0]	7
INTERNALS	
sum_u_fb[20:0]	4063
sum_u_fb_r[20:0]	4063
fb_fp[36:0]	-1040128
fb[20:0]	-32
y_fp[36:0]	260032

Build Process



IP Block Generation

Synthesis

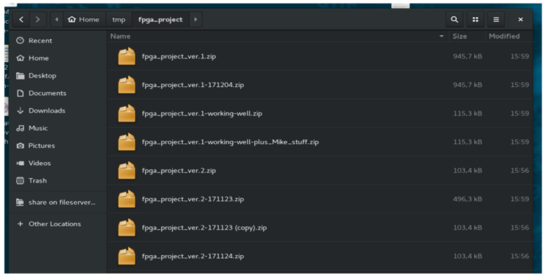
Implementation

Atlassian Bitbucket

git

One repository contains everything

Code



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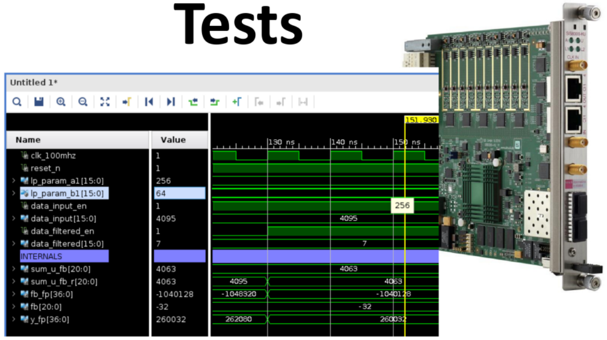

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fb[20:0]	-32
y_fp[36:0]	260032

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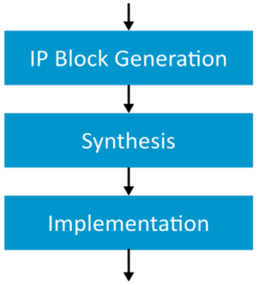
Build Process



Build Environment

CentOS

ubuntu

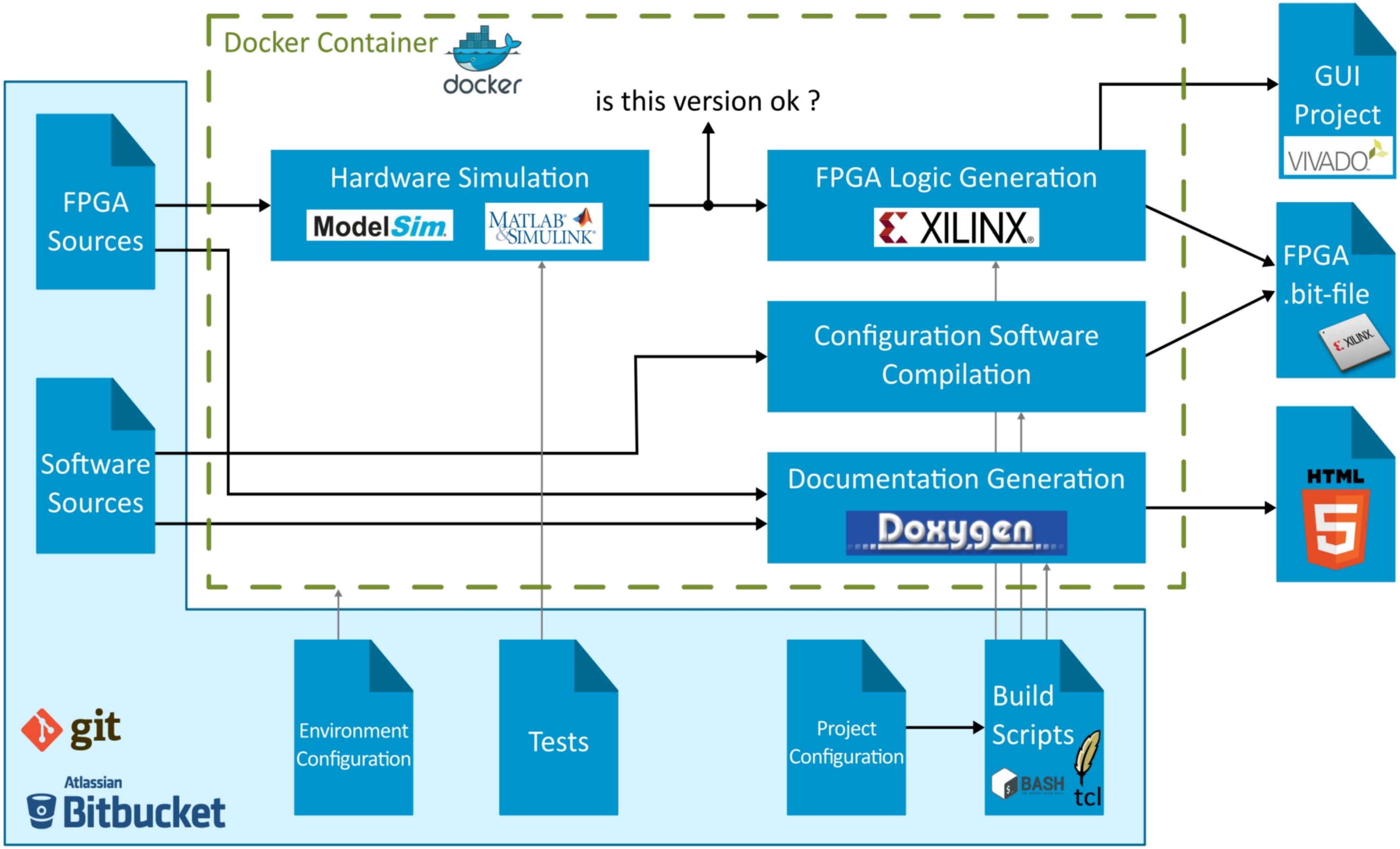
VIVADO

2016.4

2017.2

Goal: Usage of the continuous integration system Jenkins.

Automated Design Process



Conclusions

- LLRF project integrated / Other projects currently ported
- Usage of AXI4 and Xilinx IP blocks reduced development time
- Development the automated design process worth the time

Contact: christian.amstutz@esss.se

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Thank you