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The ESS FPGA Framework: An AXI4-based Framework for MicroTCA boards

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Most FPGA designs need similar functionality in order to interact with the on-board peripherals and the applications running, for instance, on a CPU in the crate. FPGA frameworks are employed to reuse the code of these functions among different projects. The ESS FPGA Framework provides these functionalities within an AXI4-based environment with the goal of supporting different MicroTCA boards and different firmware applications.
The ESS FPGA framework includes the functionality that is generally required on MicroTCA FPGA boards: (1) communication interfaces to peripherals, i.e. the analog-to-digital converter (ADC); the digital-to-analog converter (DAC) and the DDR memory; (2) upstream communication with the control system over the backplane via PCIe and definition of the interface to access the board by drivers; and (3) configuration of the on-board peripherals over SPI and I²C. Within this framework, the configuration of the on-board peripherals is handled by a microcontroller sub-system, i.e. the configuration software becomes part of the FPGA firmware. The usage of the widely used AXI4 bus family as the communication interconnect makes the framework easily extensible by IP blocks and facilitates the seamless integration of the framework with the Xilinx Vivado tool flow. Along with the framework development, an automated tool flow has been established that covers the verification of firmware components, the building of the FPGA firmware and software components, and the generation of part of the documentation.
A first version of the ESS FPGA Framework has been developed that supports the SIS8300-KU MicroTCA digitizer from Struck. The low-level radio frequency (LLRF) control system for the linear accelerator of the European Spallation Source (ESS) has been successfully integrated into the framework and several beam instrumentation applications are currently ported.

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