EUROPEAN SPALLATION SOURCE

MTCA.4 Components Designed by Polish Electronic Group for ESS LLRF Control System

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on behalf of the Polish Electronic Group (PEG)

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PEG - Polish Electronic Group

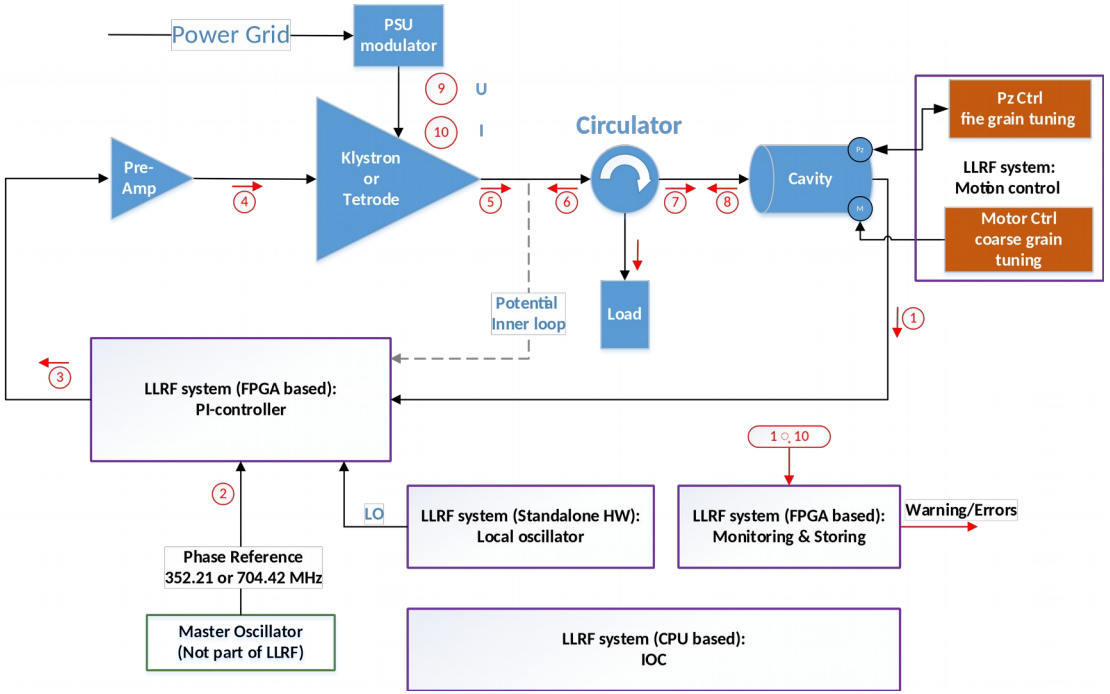
Consortium of following research units:

- National Centrer for Nuclear Research (NCBJ)
- Lodz University of Technology (LUT)
- Warsaw University of Technology (WUT)

Established for the participation in the ESS Project.

ESS LLRF System

Digital feedback system implemented in the MTCA.4 chassis



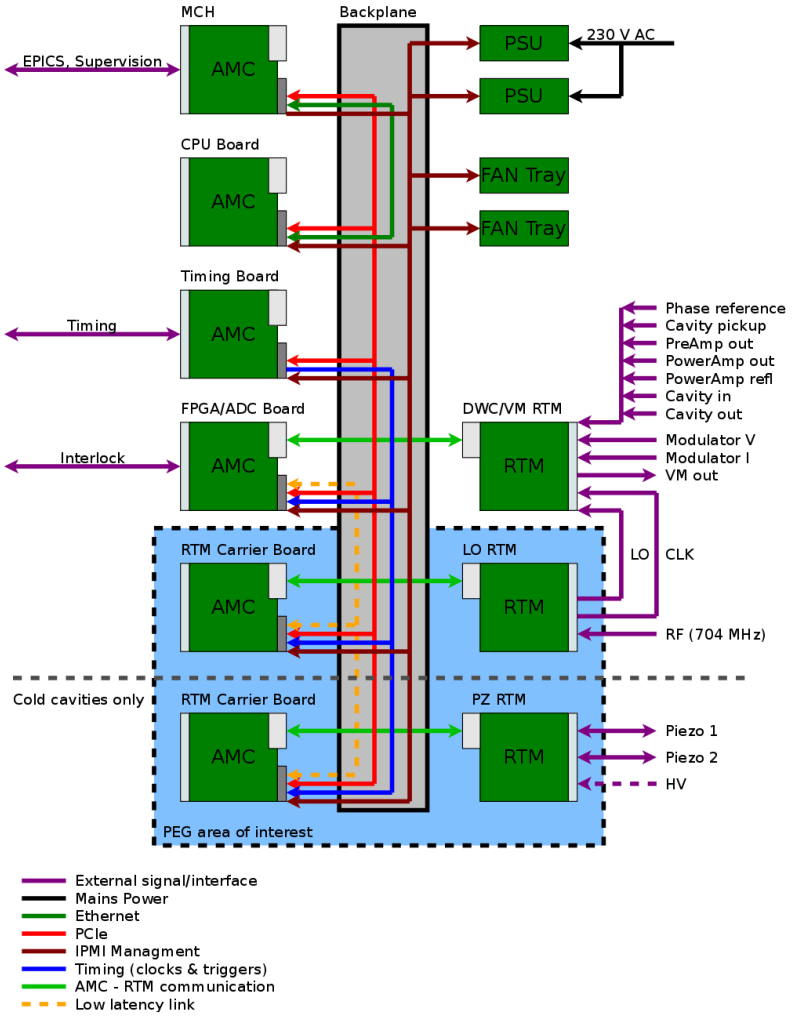
LLRF for ESS: Requirements and System design, Courtesy: Anders J Johansson

ESS LLRF System

Each ESS LLRF System unit (one MTCA.4 chassis) will be made of commercial and custom designed devices.

PEG will design, manufacture and deliver following MTCA.4 devices:

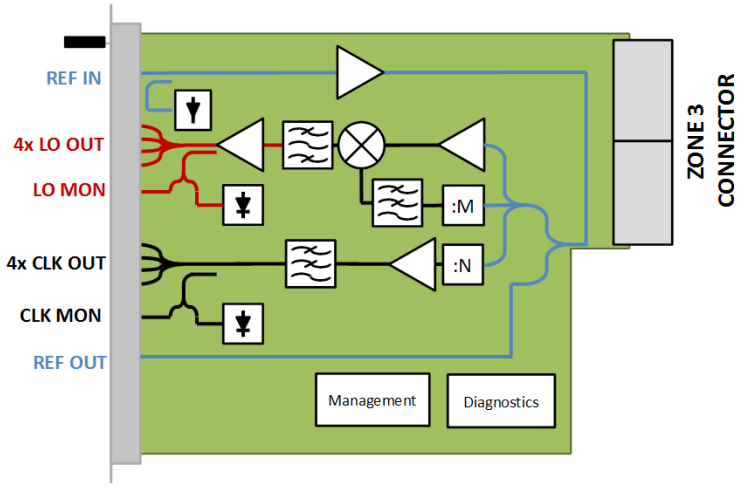
- **LO RTM** - clock generation RTM (40 units)
- **PIEZO RTM** - Cavity resonance frequency control and monitoring (120 units)
- **RTM Carrier** - minimal AMC board required for handling LO and PIEZO RTMs (160 units)

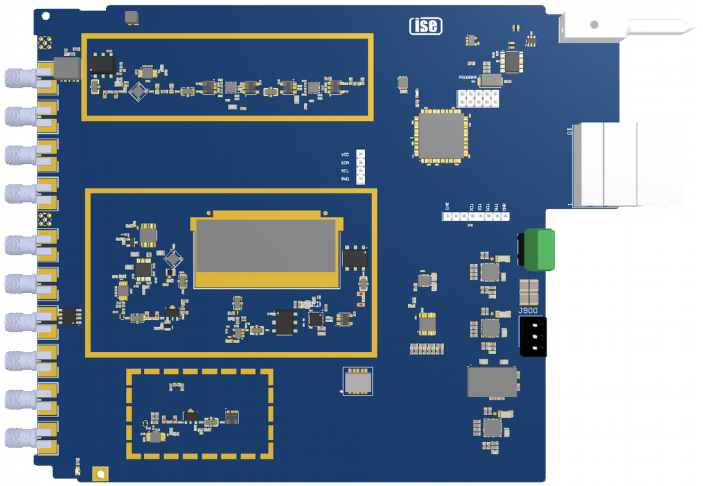


LO RTM

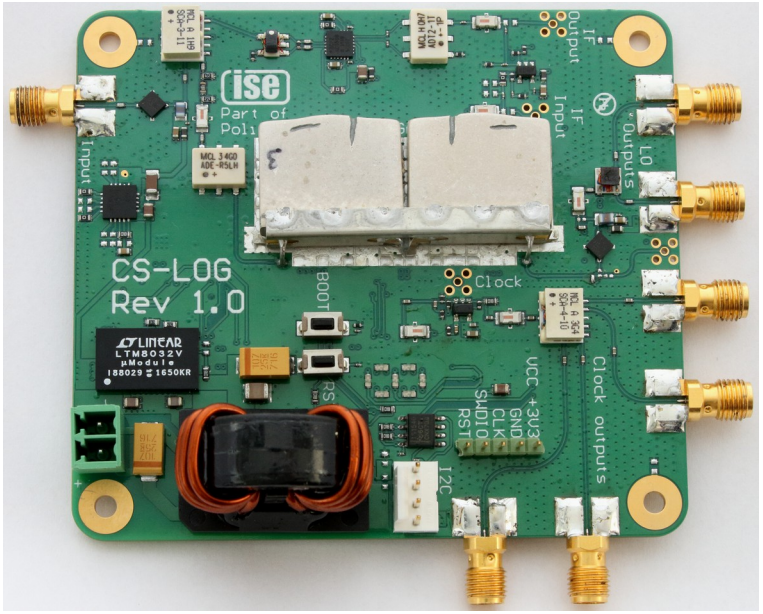
Functionality:

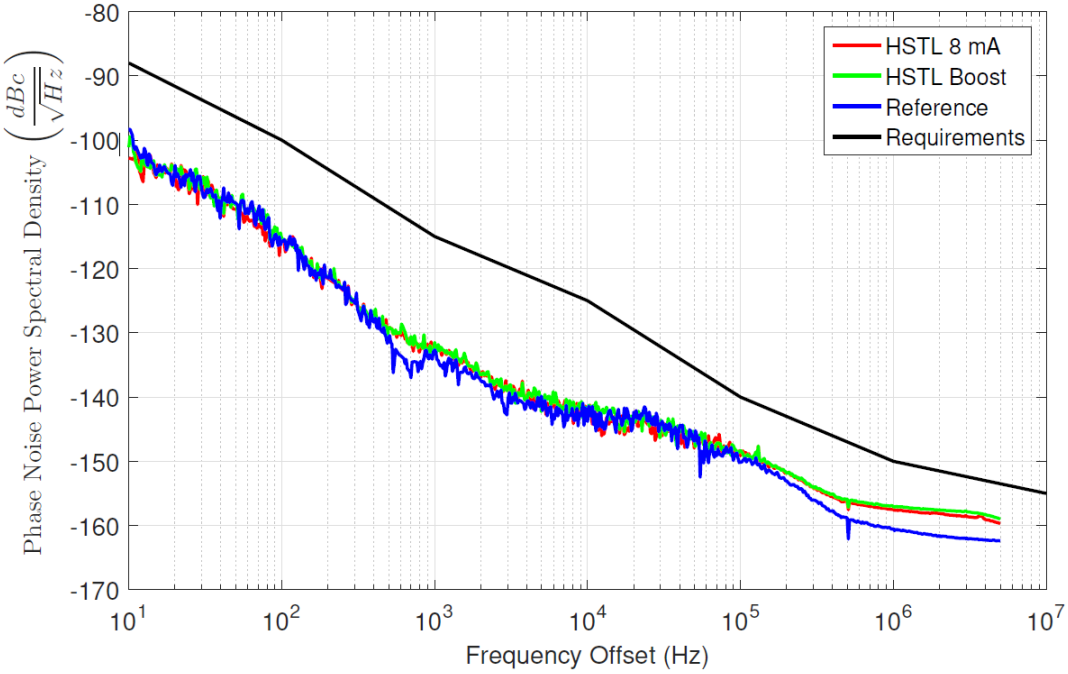
- Generation of LO and clock frequencies for the 704.42 MHz LLRF system
- IF: 25.158 or 32.019 MHz
- 4 LO signal outputs
- Monitoring output for the LO signal
- Clock frequency: 117.403(3) MHz
- 4 clock signal outputs
- Monitoring output for the clock signal
- Remote configuration by the AMC module
- D1.0 compliant
- Monitoring of output and input signals' power levels
- Diagnostics
- Monitoring of power supply voltages
- Temperature sensor





LO RTM Prototype





Current Status:

- Prototype (non-RTM) build and proven to deliver the expected performance
- Schematics and PCB design of the RTM are under review
- Boards expected in Jan 2018

Phase noise spectra of the LO signal for two signaling standards and an ideally converted reference signal. IF: 32.019 MHz

Piezo RTM

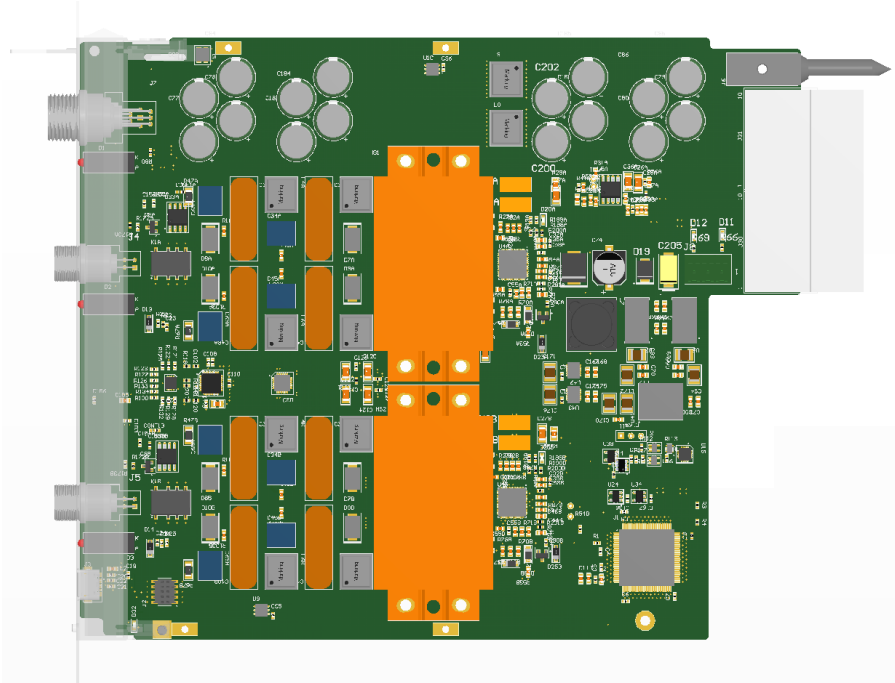
Requirements:

- Provide a control signal for piezo actuators of medium-, high-beta and spoke ESS accelerator cavities operating in cryogenic temperatures
- Measure cavity deformation using piezo device as sensor element
- Support two independent channels with configurable mode of operation: piezo actuator or sensor
- Compatible with MicroTCA.4 standard
- Provide health monitoring and diagnostics
- Assure safe operation of piezo actuator

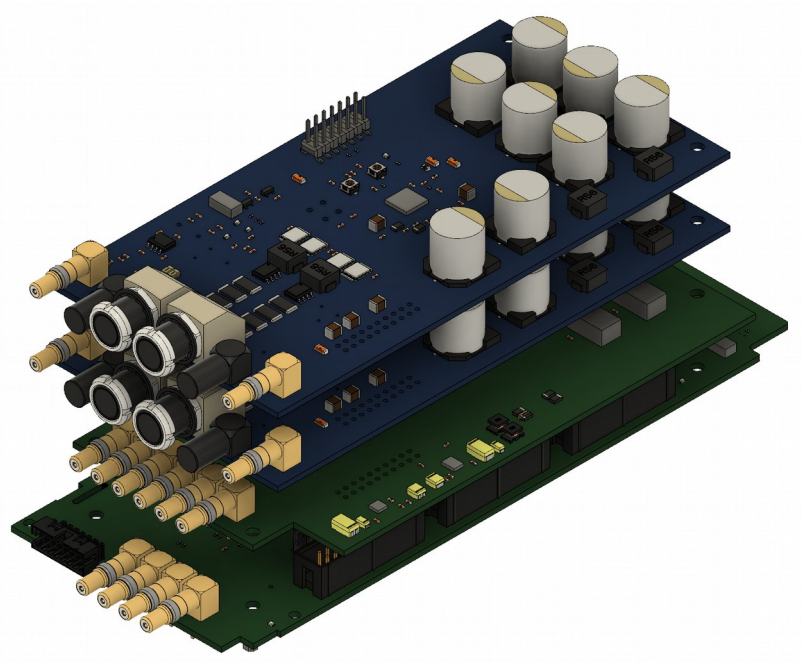
Piezo RTM

Specification:

- 2 channels of high power piezo driver
  - 2x 35 Watts (MTCA.4 power supply)
  - 2x 100 Watts (external power supply)
- Piezo driver and piezo sensor mode
- Advanced build-in diagnostics (advanced RMC with IPMI protocol)
- Various protection mechanisms for both Piezo channels to protect driver itself and piezo actuator

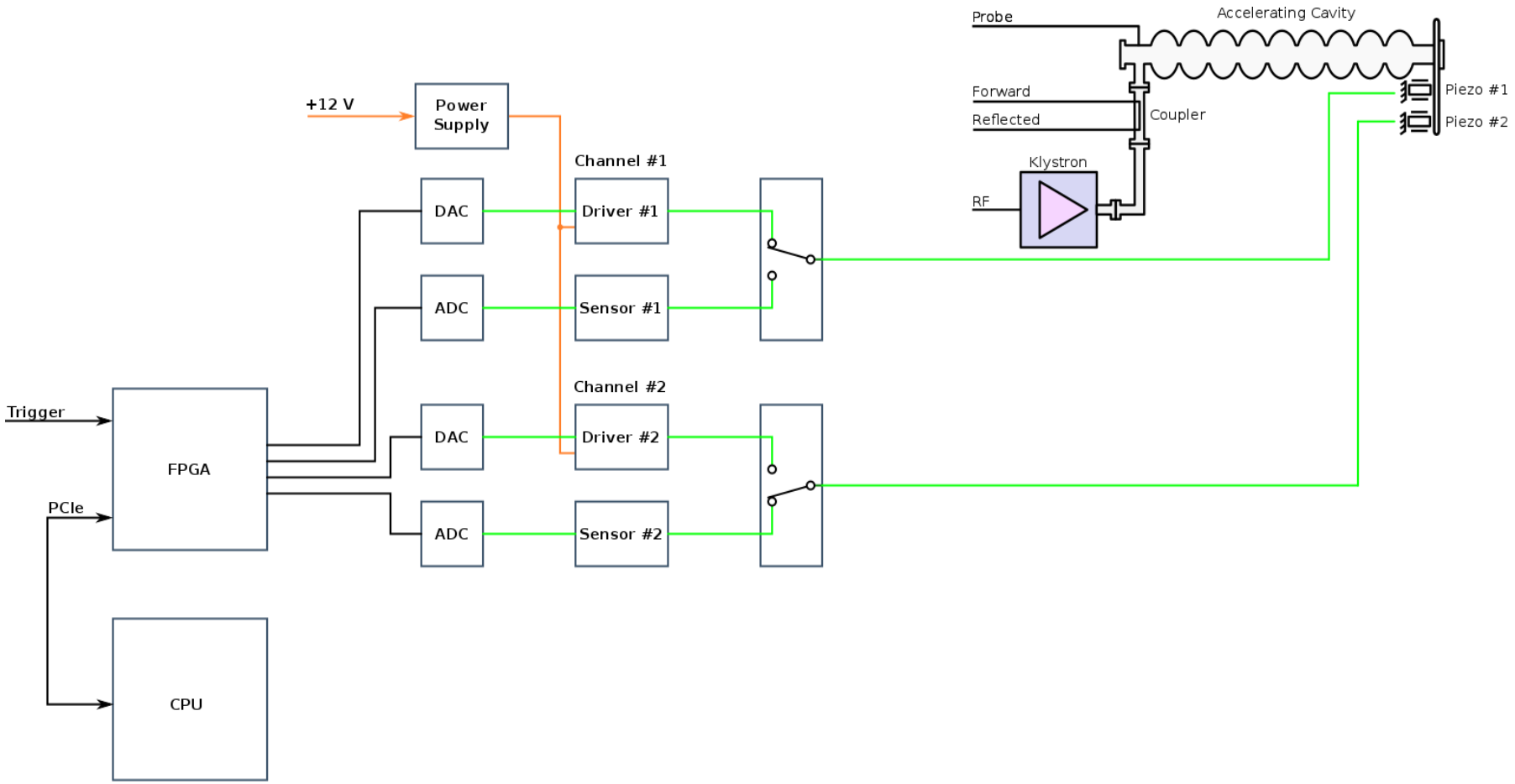


Piezo MTCA.4 Prototype Device

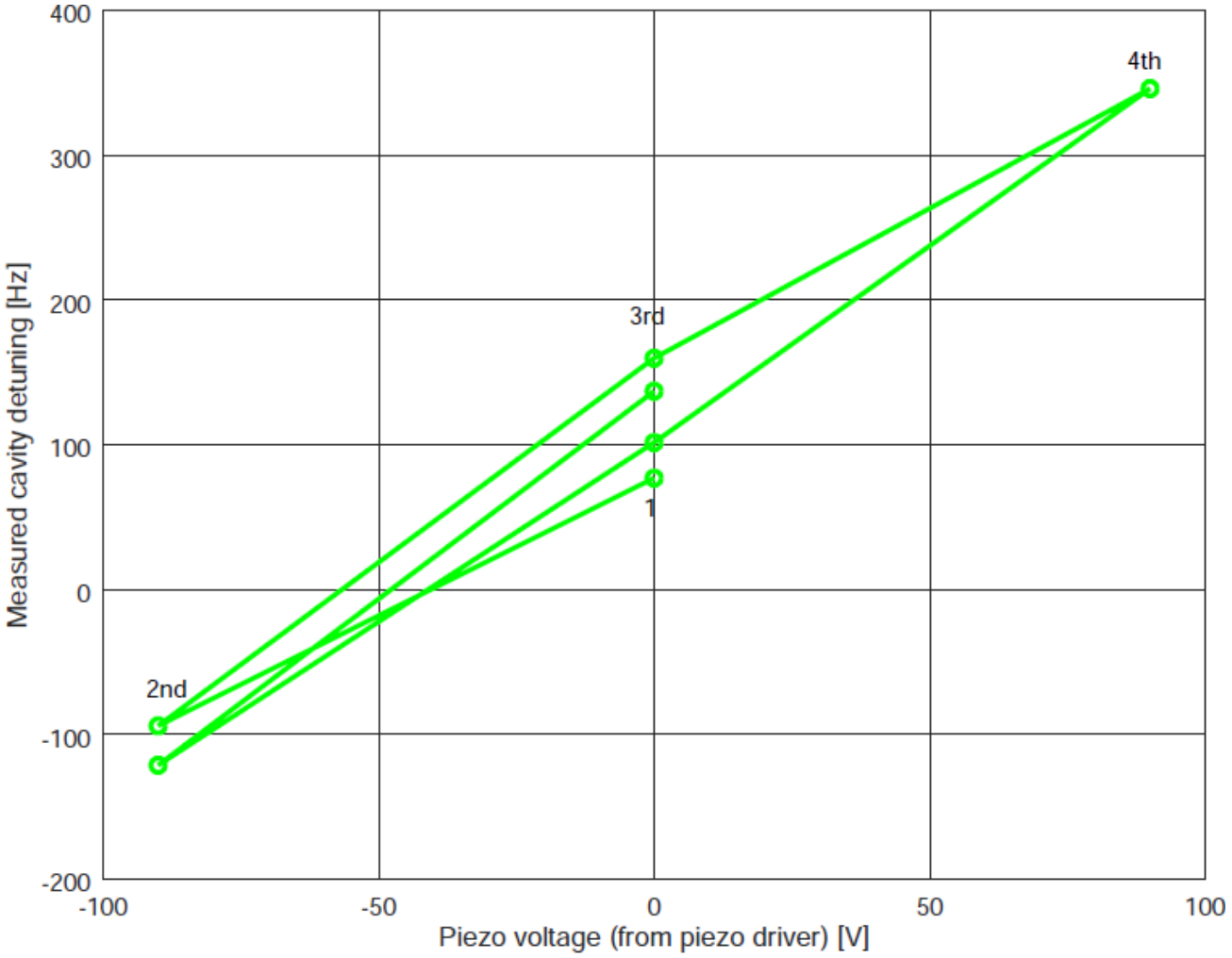


Dedicated MTCA.4 (AMC) prototype device has been created

Piezo Prototype Tests at FREIA



Piezo Prototype Tests at FREIA



RTM Carrier - AMC for LO and PIEZO RTM

Top-level requirements:

- Simple FPGA AMC board for supporting RTMs
- Minimize cost, optimally below 1000 Euro

RTM Carrier - Specification

MTCA.4 support:

Zone 3 (RTM) support compatible with DESY D1.0 recommendation (96 LVDS lines, no gigabit transceivers)

MMC (IPMI) support (mandatory LEDs, Hot-Swap handle, sensors)

PCI Express support on AMC ports 4-7

MLVDS clock and trigger lines on AMC ports 17-20

Low latency links on AMC ports 12-15 (optional, if PCI Express is x1 or x2)

FPGA

Artix-7 device (Latest family, Low cost)

Package: FFG484/FBG484 (All Artix devices can be used in this package)

Available user pins: 250/285

Available gigabit transceivers: 4

Communication:

PCI Express (x1, x2 or x4)

I2C (MMC, IPMI, debug)

USB-Serial (debug)

Low latency links on AMC ports 12-15 (optional, if PCI Express is x1 or x2)

RTM Carrier - Specification

Clocking:

- Local oscillator for FPGA
- Local oscillator for FPGA for GTP
- Programmable clock manager / clock cross-switch, which connects:
  - External Clock input on front panel
  - On-board programmable generator (Si570 or similar)
  - AMC TCLKA and TCLKB clocks
  - RTM clock in
  - RTM clock out
  - Clock output for FPGA

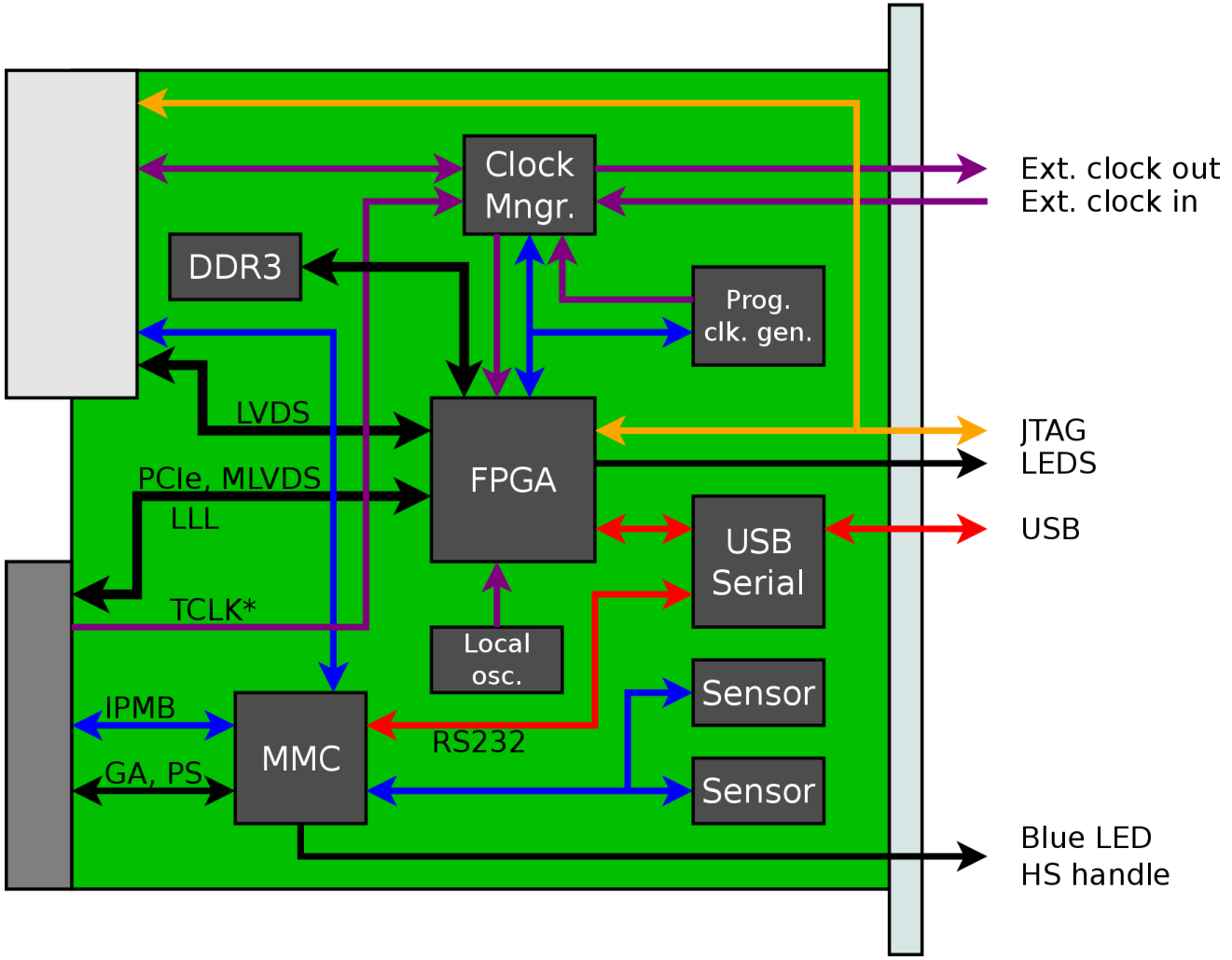
Memory:

- FPGA configuration memory
- Secondary failsafe FPGA configuration memory & watchdog (optional)
- DDR3 memory

Debugging

- USB-Serial (FTDI dual channel chip for MMC and FPGA)
- MMC IPMI support
- JTAG connector for FPGA programming
- JTAG switch to include RTM in the chain
- FPGA remote firmware upgrade (optional, via PCIe or via MMC)

RTM Carrier block diagram



FPGA

Xilinx **Artix-7** in footprint **FGG484/FBG484** footprint for the FPGA has been chosen.

This footprint allows assembly of the following devices:

Part Number	Logic Cells	Slices	CLB Flip-Flops	Total Block RAM (Kb)	DSP Slices	Max. single ended IOs (6.6 Gb/s GTPs)
XC7A15T	16,640	2,600	20,800	900	45	250 (4)
XC7A35T	33,280	5,200	41,600	1800	90	250 (4)
XC7A50T	52,160	8,150	65,200	2700	120	250 (4)
XC7A75T	75,520	11,800	94,400	3780	180	285 (4)
XC7A100T	101,440	15,850	126,800	4860	240	285 (4)
XC7A200T	215,360	33,650	269,200	13140	740	285 (4)

FPGA Configuration

FPGA configuration process will be controlled by the Module Managment Controller (MMC).

The following configuration modes are foreseen to be used:

- Master SPI – FPGA loads firmware from SPI flash by itself
- Slave Serial – MMC can disable SPI Flash ans push bitstream to FPGA
- JTAG – fail-safe configuration mode using external programming cable

FPGA Configuration – JTAG

For development and in case of FPGA troubleshooting, JTAG configuration mode is provided. Described design has two JTAG slave devices:

- FPGA device
- RTM Interface

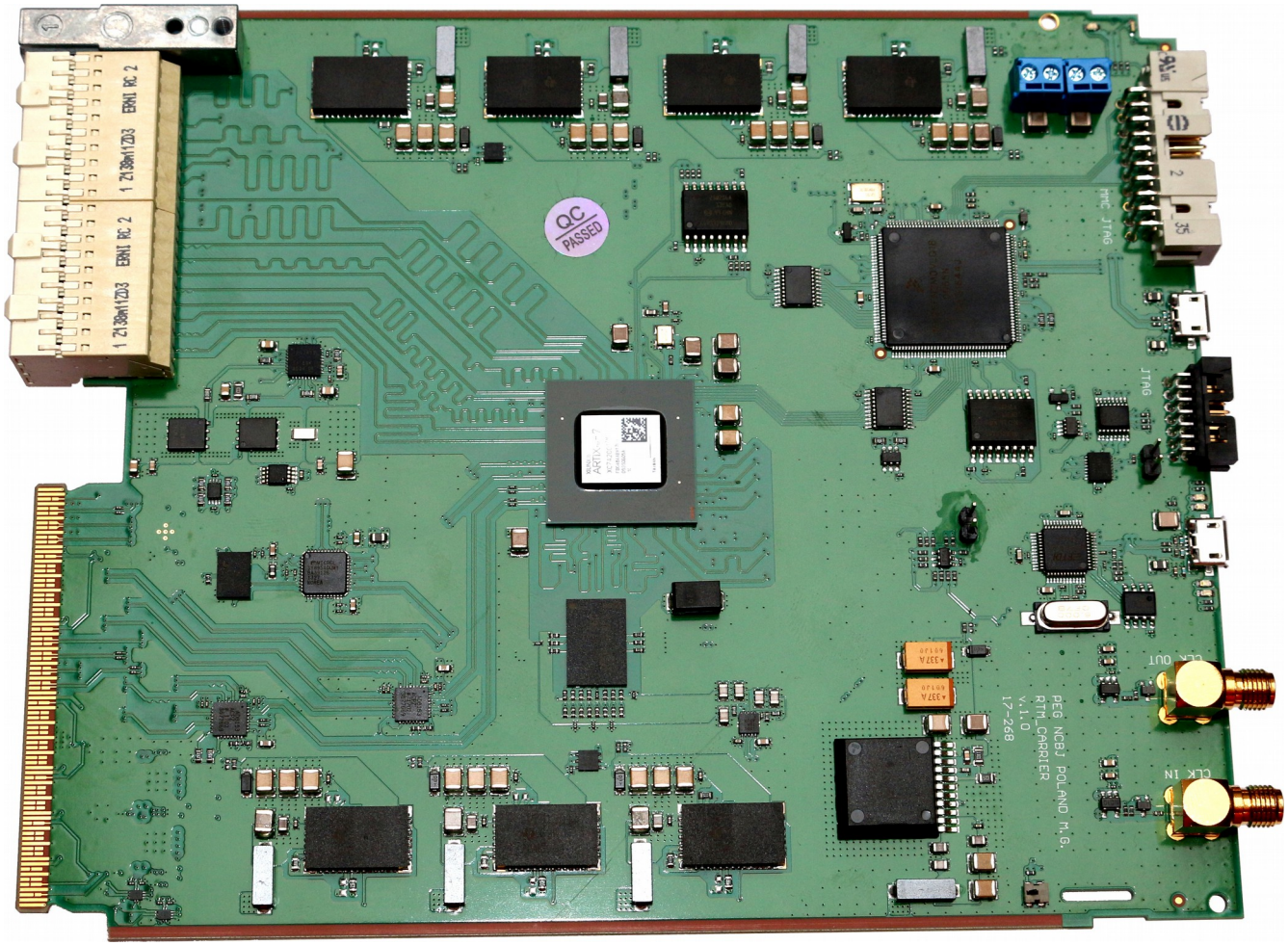
and two JTAG master interfaces:

- Xilinx JTAG Connector
- AMC JTAG interface

Board has smart active JTAG distribution, which allows plug and play operation - **no jumper configuration is required for JTAG**

MMC device is not included in the chain and will have own JTAG connector

RTM Carrier First Prototype



Lodz University of Technology Stand

The End

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Thank You for Your Attention !