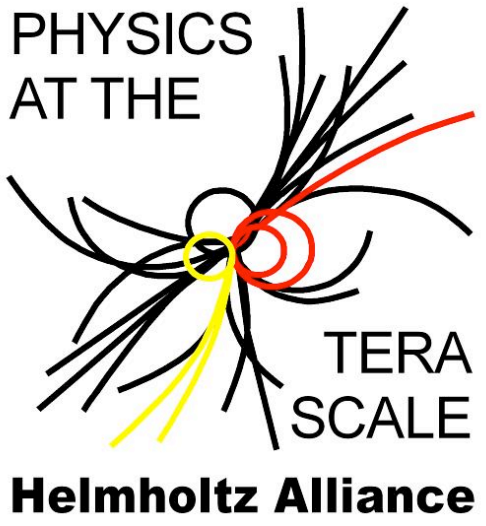
Status of VLDT Nodes Heidelberg Report

Karlheinz Meier, DESY 03/2009

- Goals
- Infrastructure (update from 03/2008)
- Current Projects



WP 1 The Virtual Laboratory for Detector Technologies

A central part of the Alliance is the formation of a Virtual Laboratory for Detector Technologies, called VLDT in the following.

This laboratory will form the backbone of a network of the alliance partners formed to ensure a visible, efficient and long-lasting contribution of German groups to the future projects ILC and sLHC. The VLDT will develop, provide and maintain infrastructures and make them available to the Alliance. It will have three branches, electronics system development, sensor development and general detector test facilities. The central nodes of the VLDT will be DESY, the University of Bonn and the University of Heidelberg. Additional infrastructure will be made available to the Alliance by Aachen, Hamburg and Karlsruhe. As the project develops other institute might contribute infrastructure as well. All Alliance partners involved in detector design and construction will profit from the VLDT.

WP 1.1 The Electronics System Development Laboratory

HD Contribution :

KIRCHHOFF-
INSTITUT
FÜR PHYSIK

Within the Helmholtz Alliance Initiative the Heidelberg group plans to upgrade its research and development facilities in order to extend training and support to the German particle physics community. For that purpose it is planned to acquire laboratory (clean-room) workbenches including measurement equipment for five guest users, and to set up ten additional chip design and simulation workstations.

Basis : ASIC Laboratory for Microlectronics Heidelberg

- Established 1994
- Hosted by Kirchhoff-Institut für Physik
- Support Lab for Particle / Nuclear / Cosmic and Biophysics
- Contributions to HERA-B, HERMES, H1, ZEUS, ATLAS, LHC-b, ALICE, HEGRA, HESS, GERDA
- Current full staff : SW Engineer, Lab Engineer
- Related activities : Technical Informatics (KIP), Technical Informatics (ZITI, former Mannheim Group), International Graduate School on Intelligent Detetctors
- TASKS : ASIC / FPGA Design, Test of Chips / Wafers / Boards / Systems, System Design, Simulation

Support offered to (external) Users

- Access to Lab Equipment and S/W Tools
- Instrumentation Tutorials (Testing, Bonding, Packaging)
- Software Support (Layout, Simulation)
- Submission Support (MPW, Engineering Runs, Full Runs)
- Submission Readiness Reviews
- ASIC Designer Style Guides
- Online Tutorials

Computer Hardware and Access Policies

Remote access for ASIC lab members and registered HGF Alliance users via KIP Portal Server :

portal.kip.uni-heidelberg.de

Running local NXClient, SGD (Sun Secure Desktop) or SSH

Selected project partners with increased access needs : VPN Access

DIFFEENT ACCESS RIGHTS DEFINED BY SOFTWARE VENDORS

PLEASE CONTACT ASIC LAB TO USE THIS INFRASTRUCTURE

NEW : MOSIS Membership – Access for HGF Members

AMIS Fabrication Processes
include 0.7µm high voltage CMOS, 0.5µm CMOS
and 0.35µm high voltage CMOS

AMS Fabrication Processes Processes
include 0.35µm CMOS, high voltage CMOS
and SiGe BiCMOS

IBM Fabrication Processes
from 65nm to 0.25µm in CMOS
and from 0.13µm to 0.50µm in SiGe BiCMOS

TSMC Fabrication Processes
include 0.35µm, 0.25Mm, 0.18 µm CMOS

Design Kits installed at KIP, contact the ASIC lab if you want to use them !

Clean Box operational since February, semi-automatic prober and bonder installed

Laboratory Acquisitions

Alliance Acquisition of Laboratory Equipment finished

State-of-the-Art Equipment for

- High speed (serial) link developmenz and test
- Low noise high bandwidth analogue circuit testing
- BGA placing and mounting
- Medium thoughput wafer and chip testing

Open issue (request to Alliance management board)

- Flip-chip placer (200 k€ Investment)
- No interest outside HD -> Not to be pursued further

Staff Support

2 Engineers available for HGF support

- Use of Lab Facilities
- Access to Design / Simulation / Technology Kits

Additional promising candidate to visit lab in june

REMEMBER THE PROPOSAL :
THIS IS NOT A PLACE „TO ORDER CHIPS“ !

Alliance related local projects (many more outside HGF)

ATLAS (Phase 1 and 2 to be approved) :

LVL-1 Calorimeter Trigger MCM Update (Phase 0)
Time frame 2009 / 2010

LVL-1 PPr input stage Upgrade (Phase 1)
Time frame 2012 / 2013

LVL-1 PPr optical transmission to JEM (Phase 1)
Time frame 2012 / 2013

Tile Calorimeter Frontend Upgrade, On-Detector PPr
Time frame 2017 / 2019

ILC-Calice :

SiPM and TDC Development