SiMPI - An avalanche diode array with bulk integrated quench resistors for single photon detection

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on behalf of

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TUM
LMU
Excellence Cluster
Universe

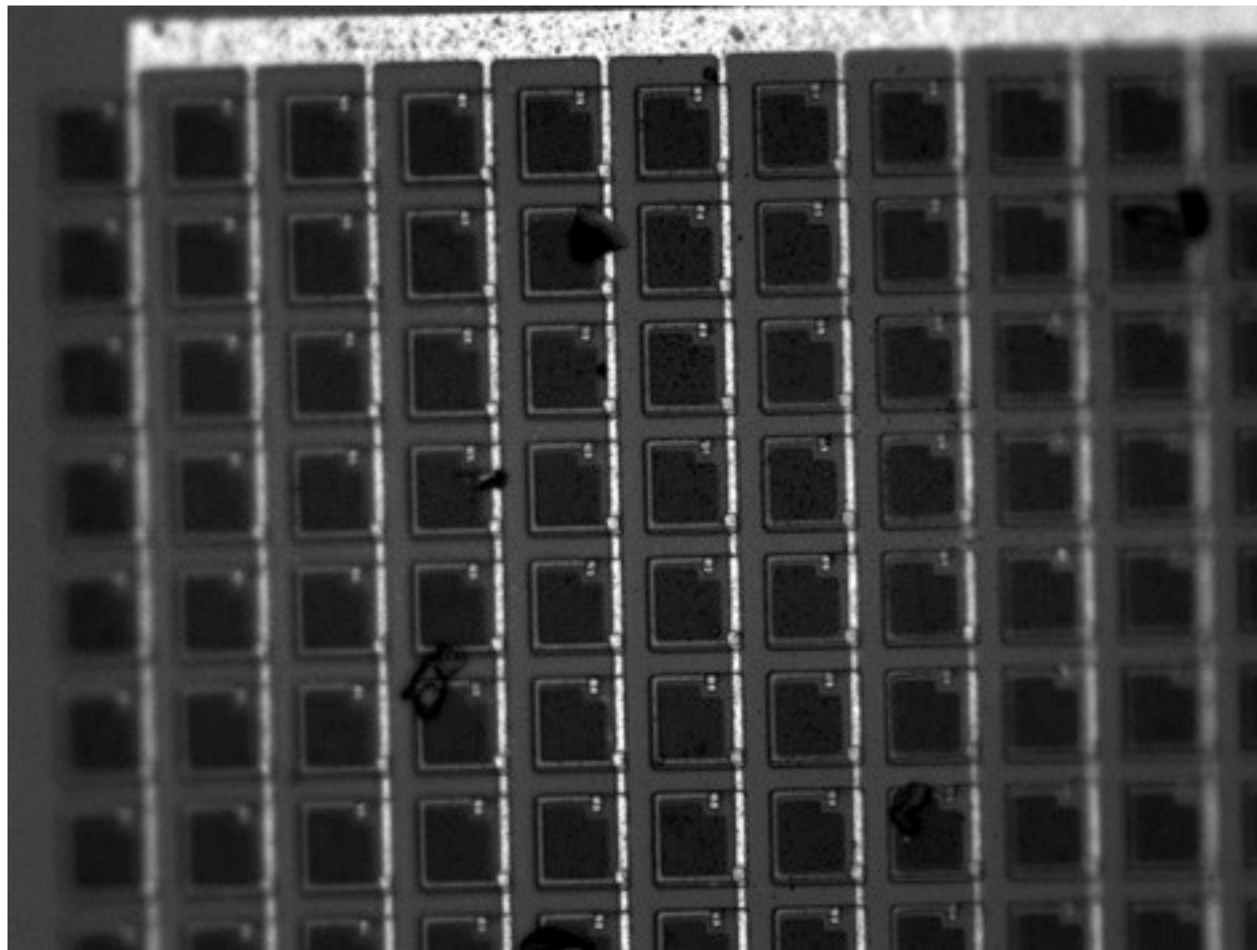
Overview

- Silicon Photomultipliers: SiPM
- The SiMPI Concept
- Device Simulations
- First Production: Proof of Principle
- Summary

What is a Silicon Photomultiplier – SiPM ?

An array of avalanche photodiodes

- operated in Geiger mode ➫ binary device
- passive quenching by integrated resistor
- read out in parallel ➫ signal is sum of all fired cells



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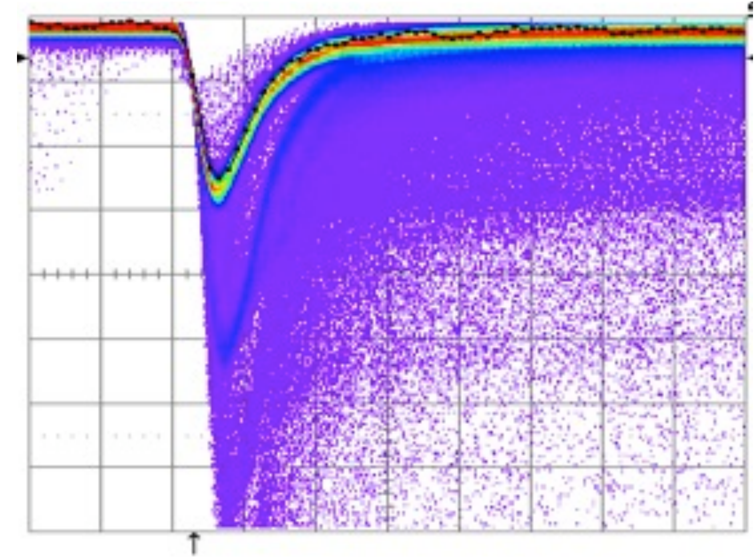

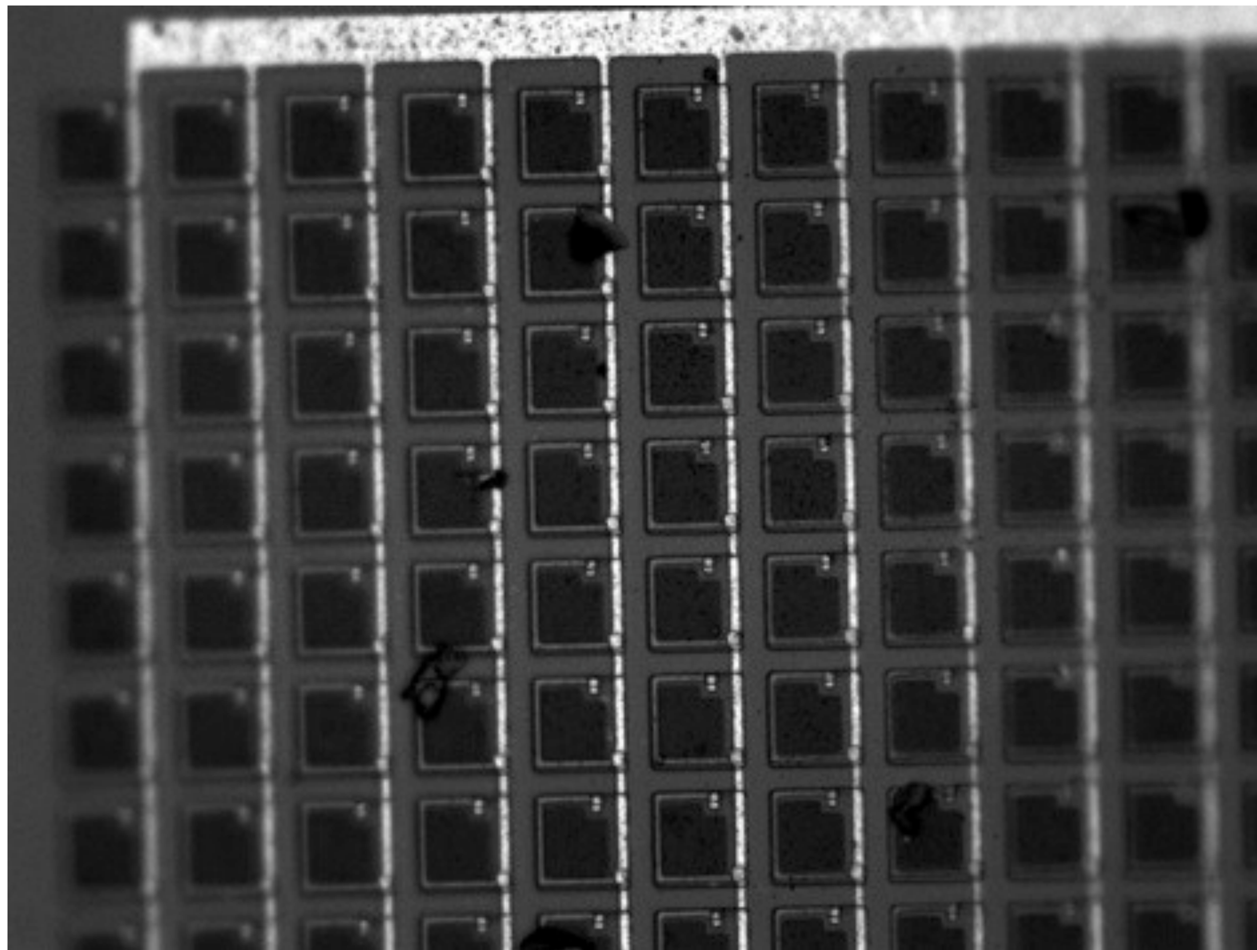

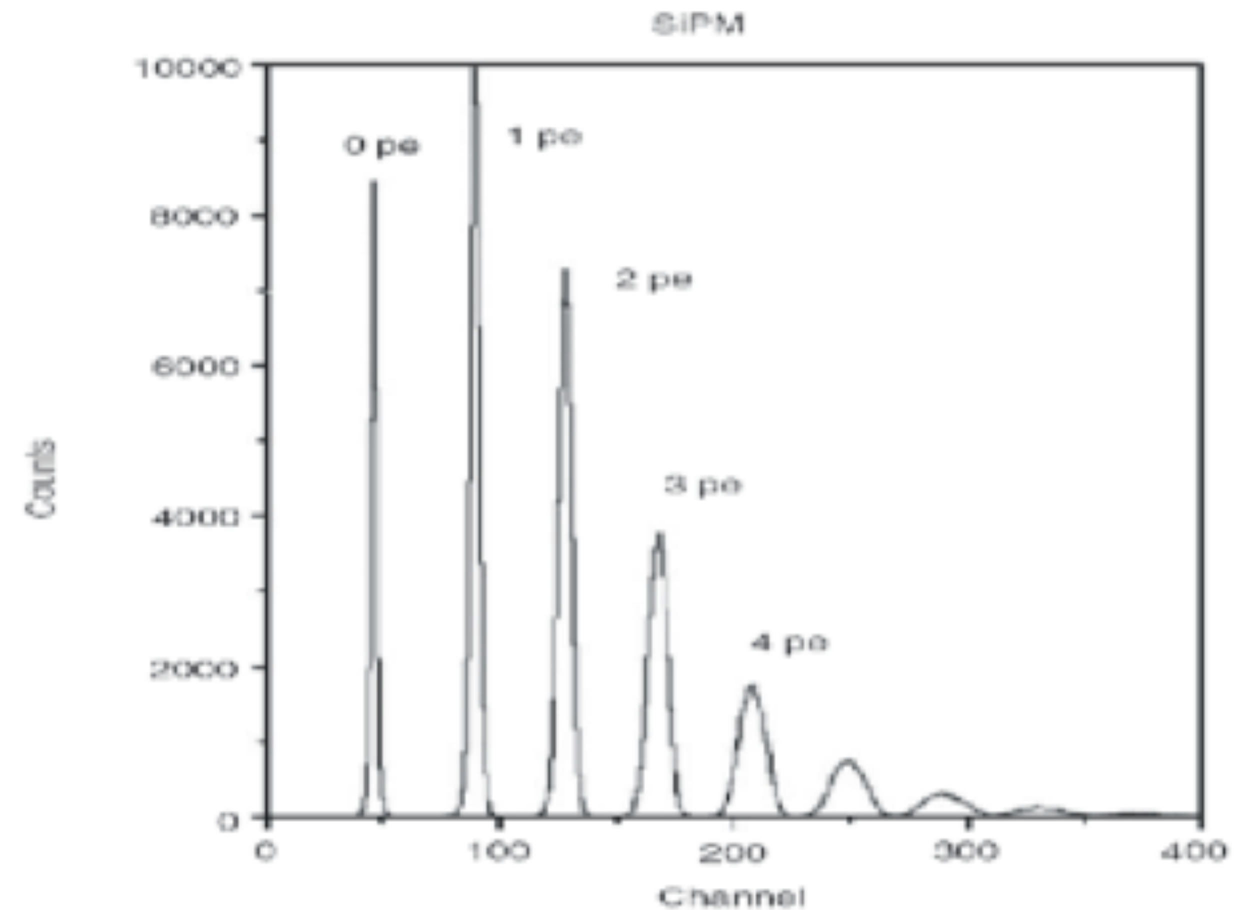

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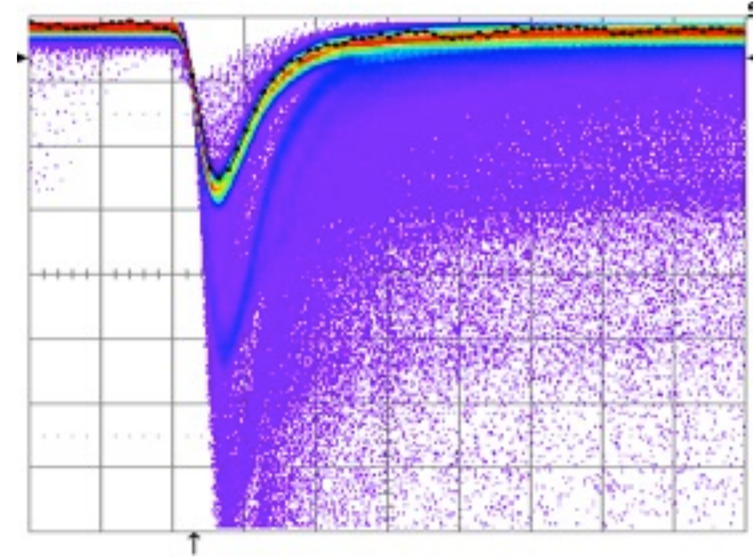
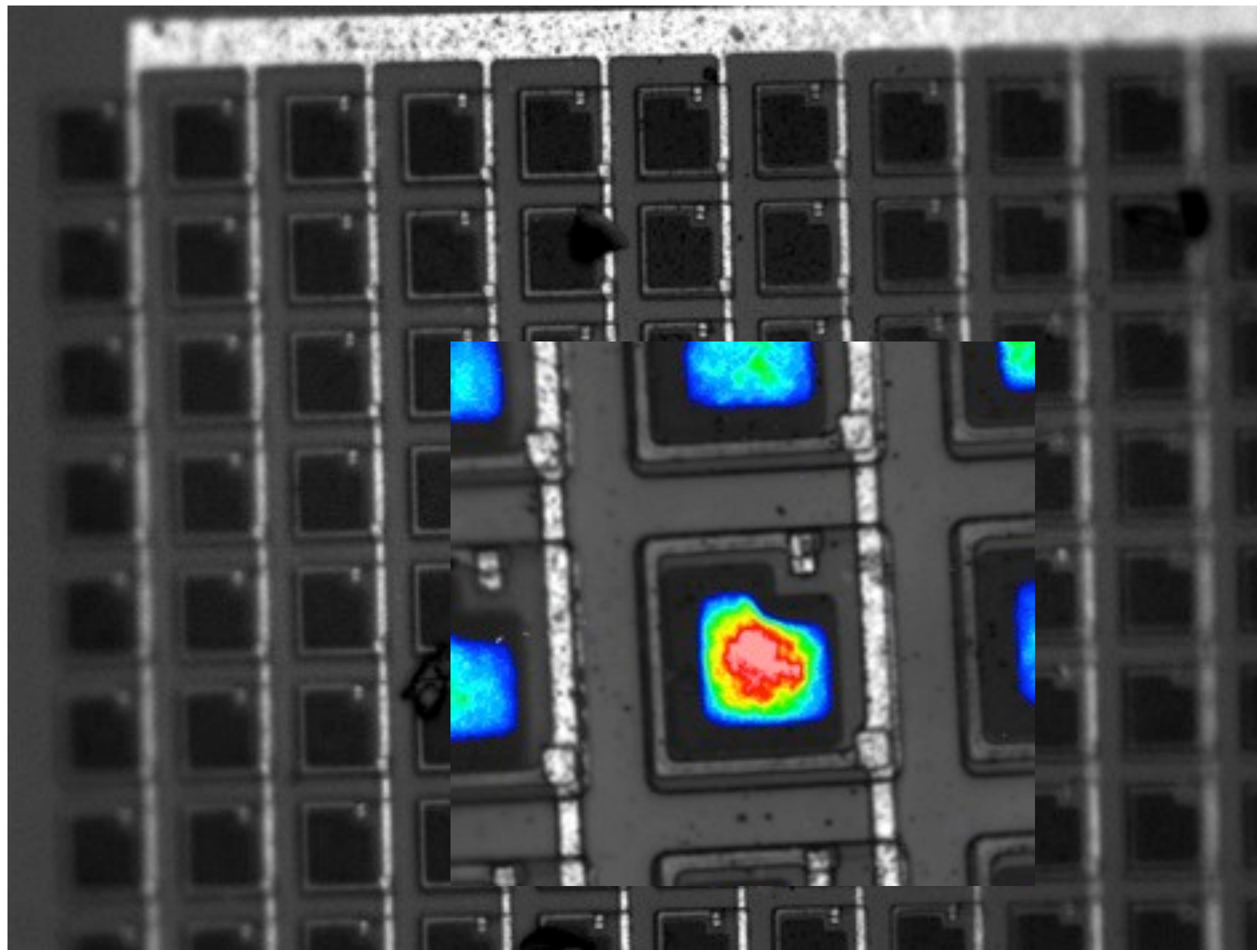
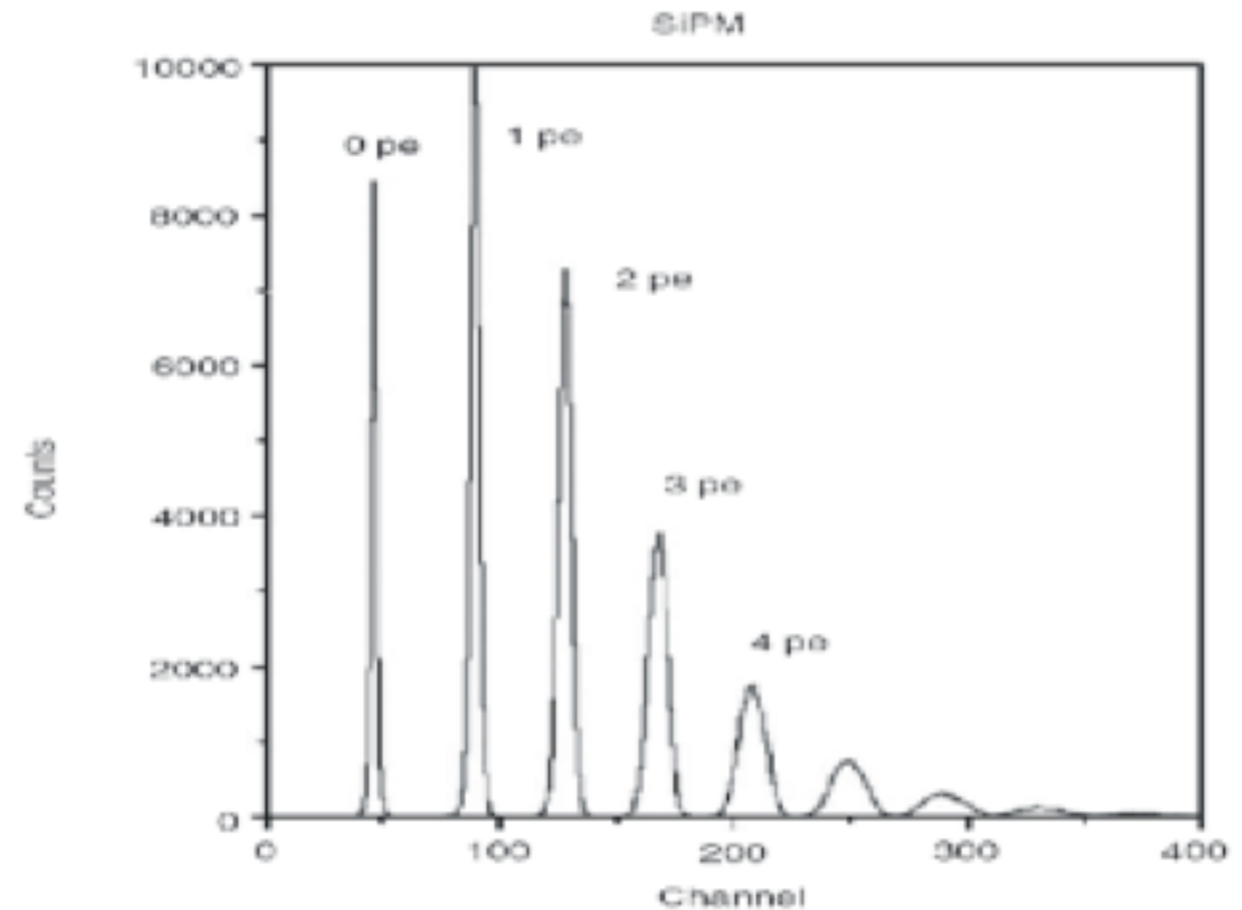
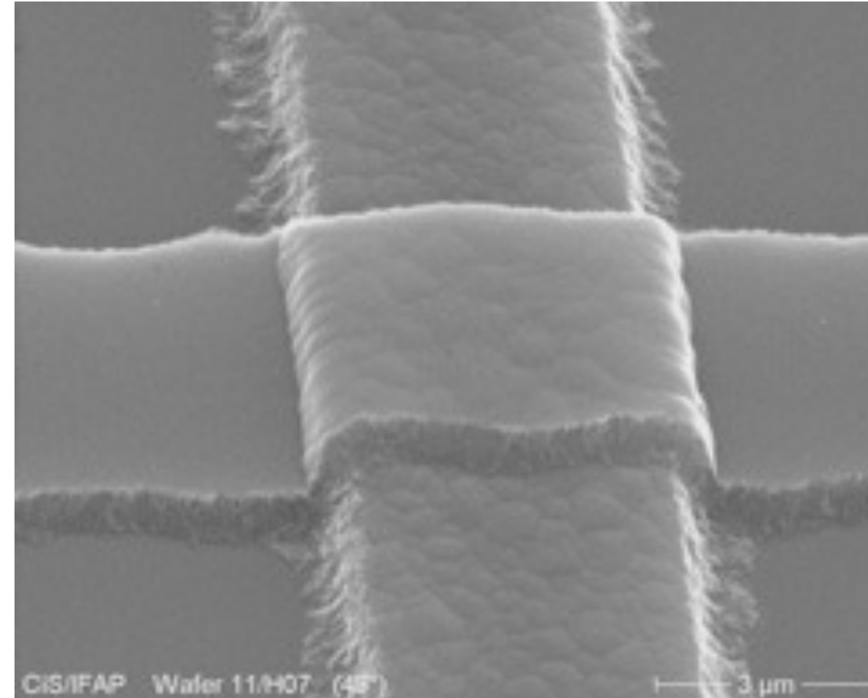




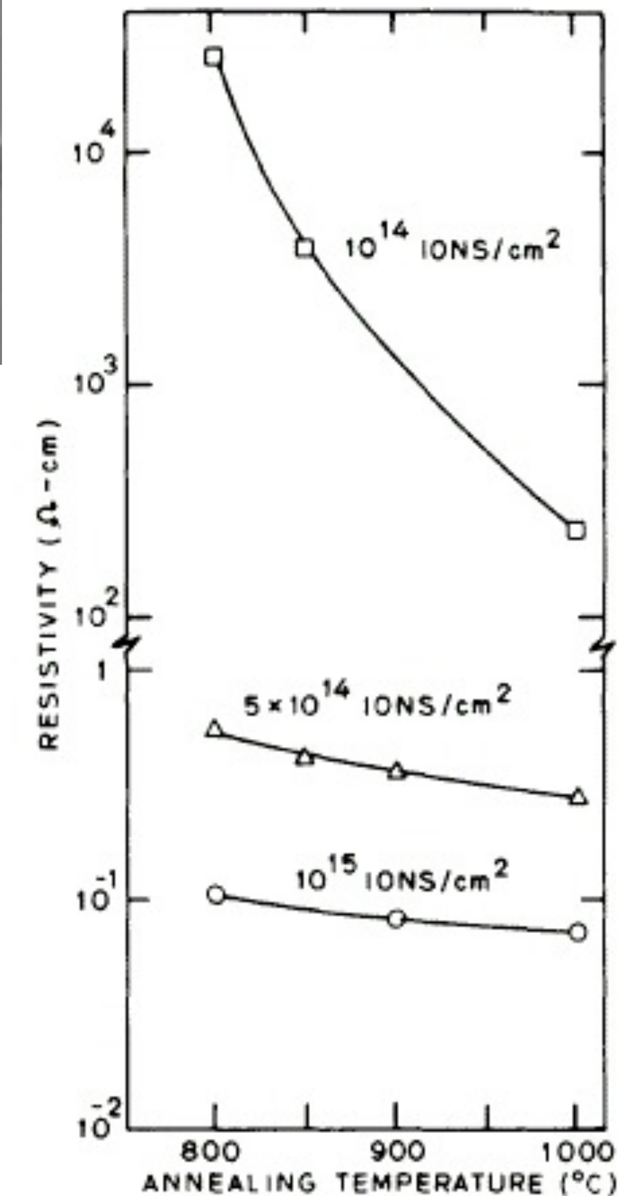


Polysilicon Quench Resistors

- Process complexity
  - CVD deposition
  - Photolithography, etching, insulation (over bias voltage drops across the insulator beneath the resistor)
- Critical resistance range
  - influenced by:
    - grain size, dopant segragation in grain boundaries, carrier trapping, barrier height
  - sheet resistance depends on:
    - Deposition conditions, implantation dose, layer thickness, annealing temperature, preconditioning (cleaning steps before deposition)



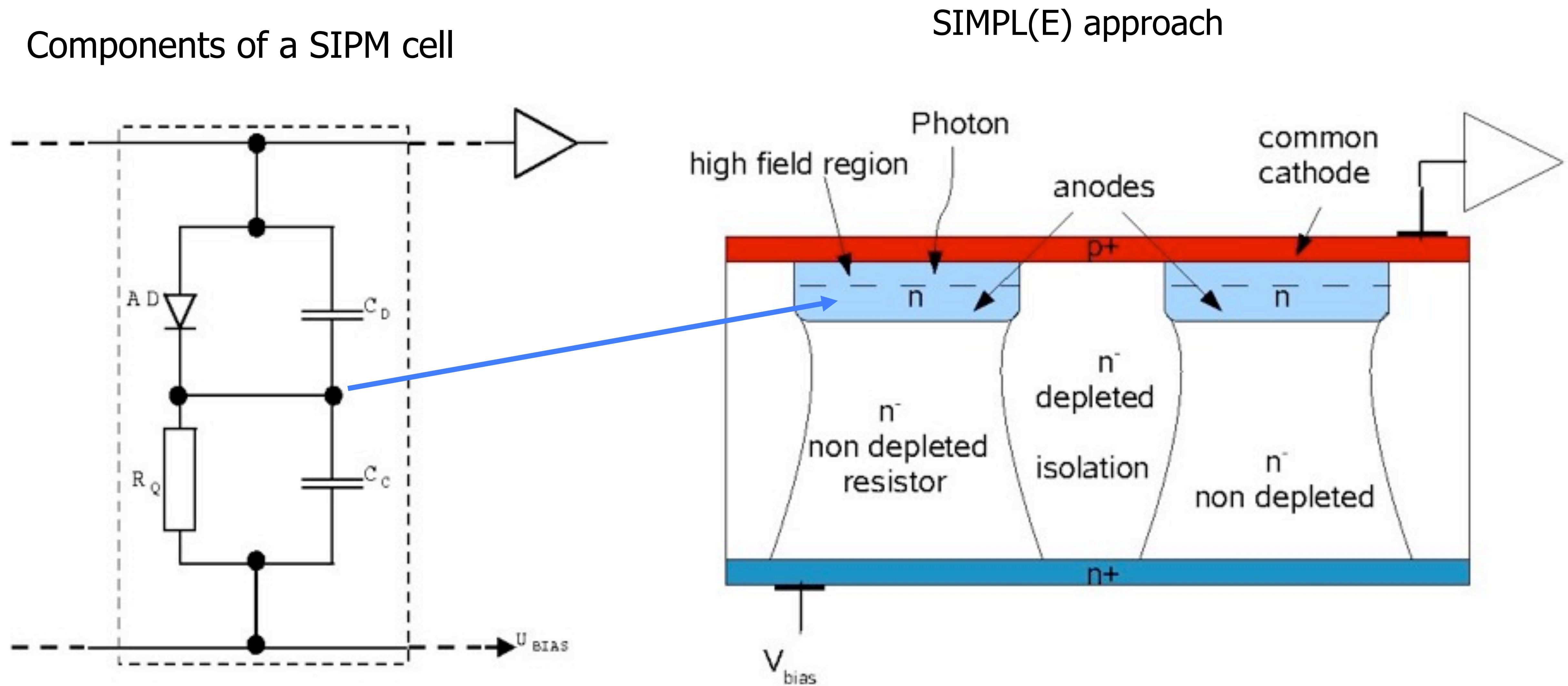
wet etching not trivial at all
not very homogeneous over the wafer



M. Mohammad et al.
'Dopant segragation in polycrystalline silicon',
J. Appl. Physics, Nov.,1980

▸ Rather unreliable process step and an obstacle for light!

Why not ?



Front side p^+ cathode and backside n^+ region are common for the entire array

Anode region becomes an internal node within silicon

Bulk region beneath the anode acts as vertical resistor shielded by the anode from depletion

Gap regions are depleted and isolate the individual resistors

But resistor matching does not work with a wafer of usual thickness ! ☹

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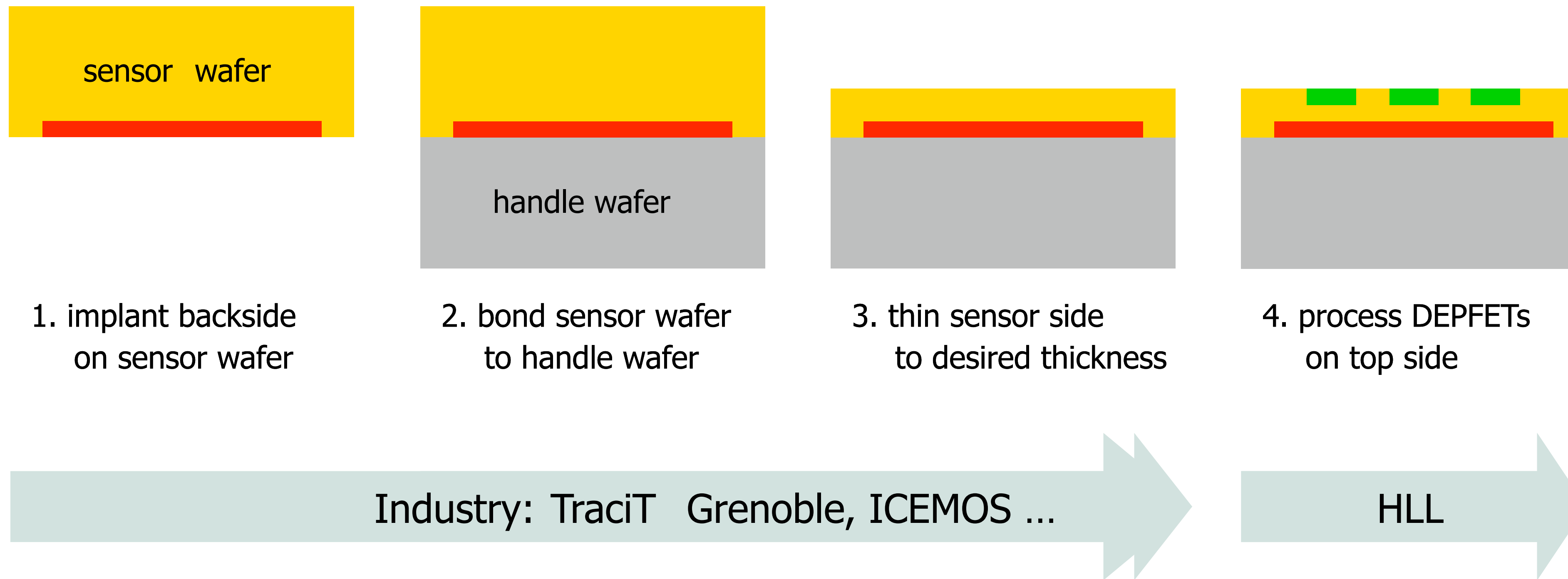
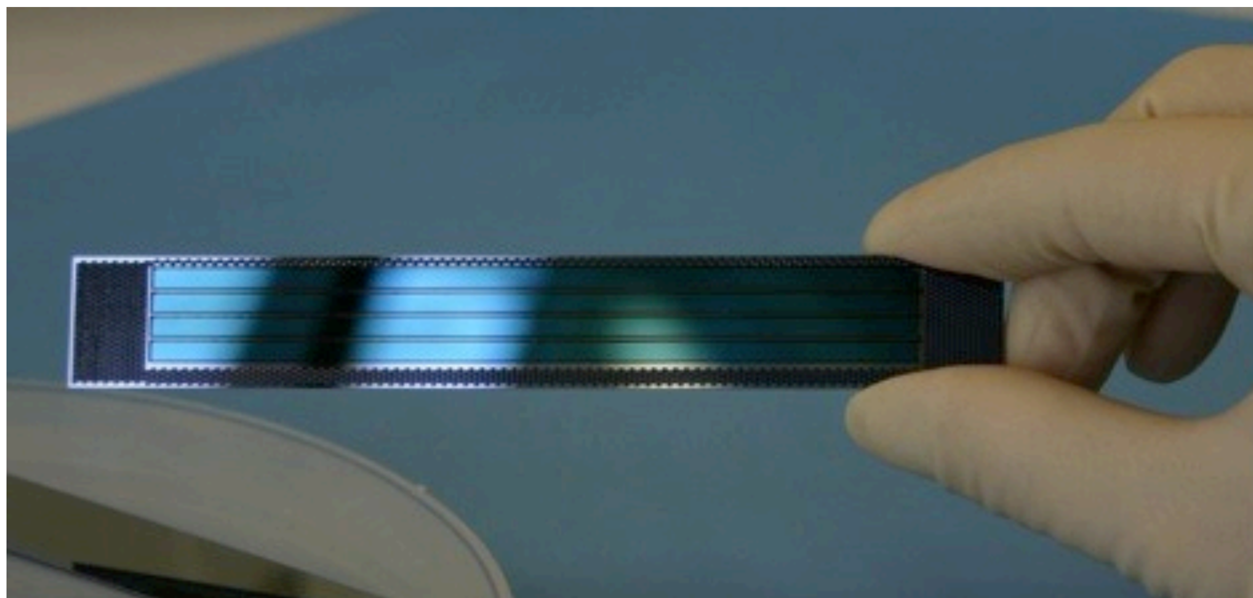
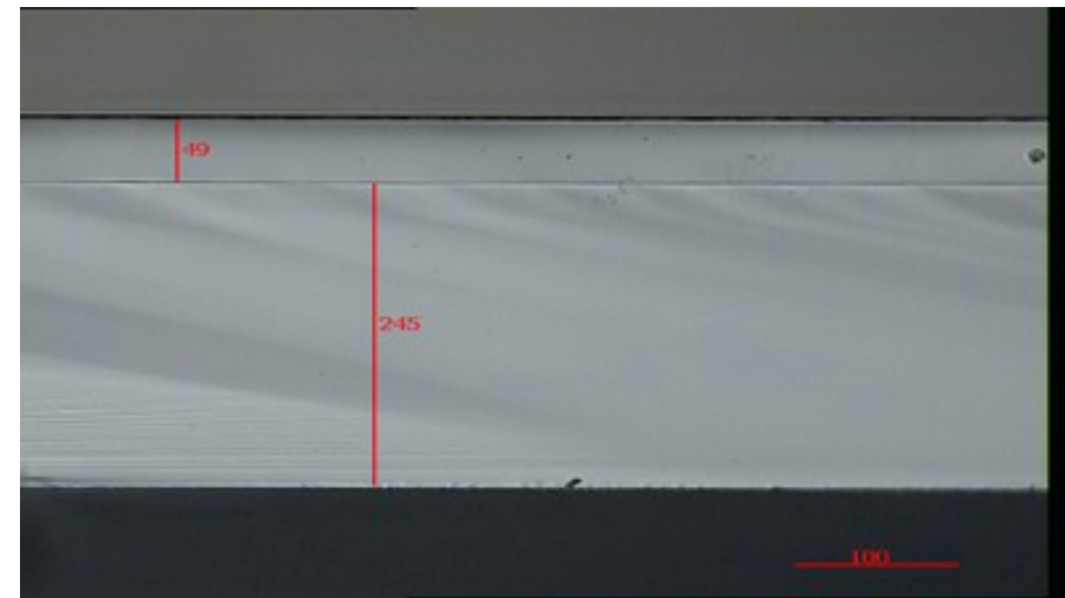
SOI wafers







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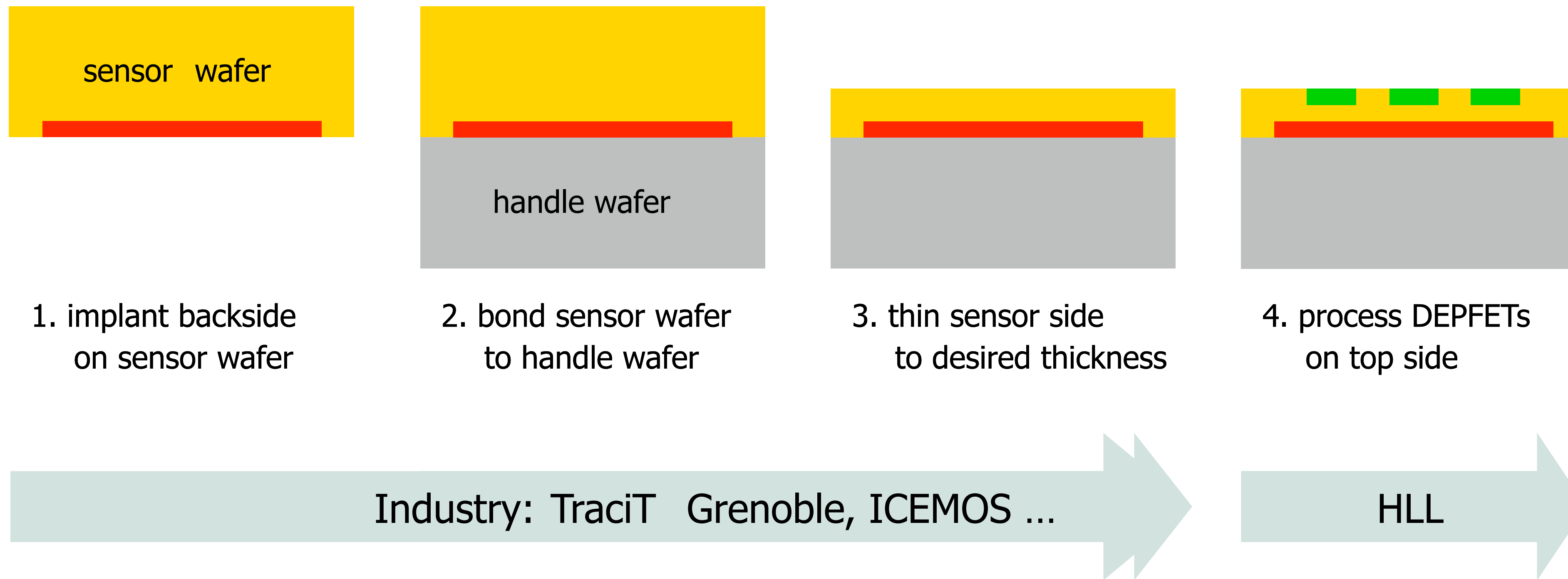
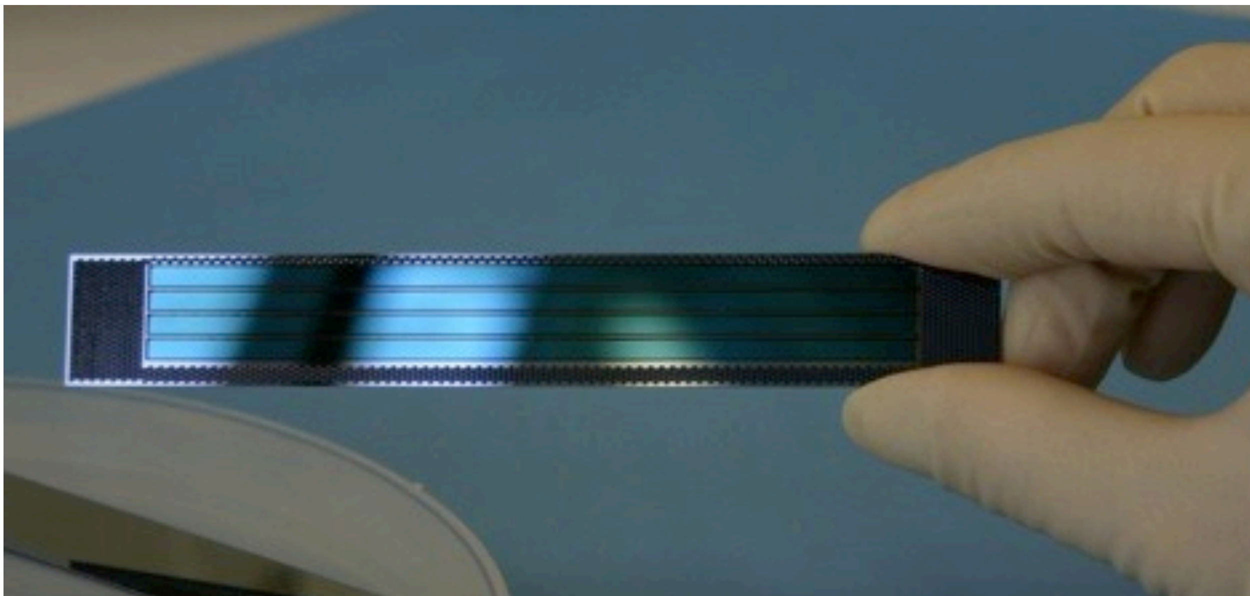
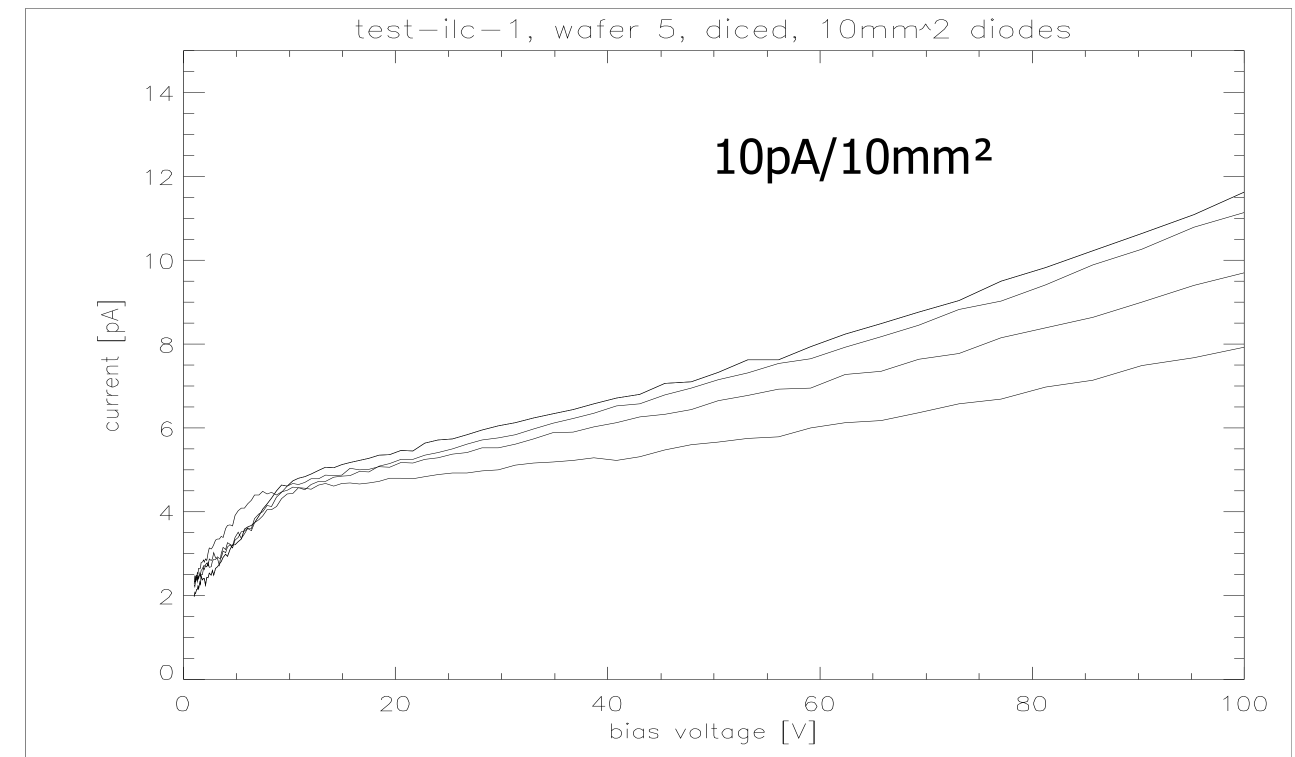




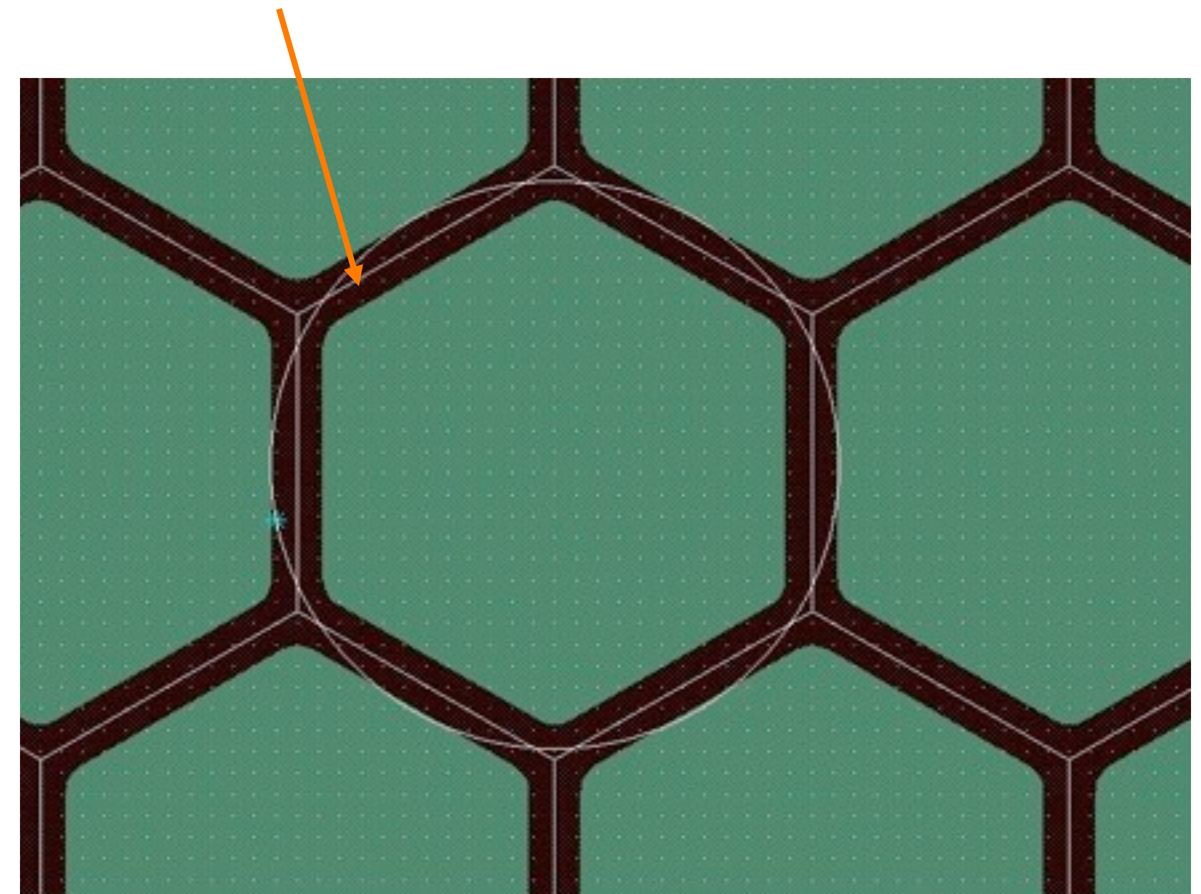


Matching of resistor requirements with bulk geometry

- A simple resistor problem (bulk resistivity and geometry)
- but ...
    - carrier diffusion from top and bottom layer into the resistor bulk
    - sideward depletion

➩ device simulations necessary !

cylindrical approximation of hexagons for quasi 3d simulation



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Simulation results

- Showed feasibility of the approach for both small pixel sizes and big pixel sizes.

Big pixel size (~100μm)

High PDE due to high fill factor
Small dynamical range

➔ in low light experiments astrophysics experiments like EUSO and CTA

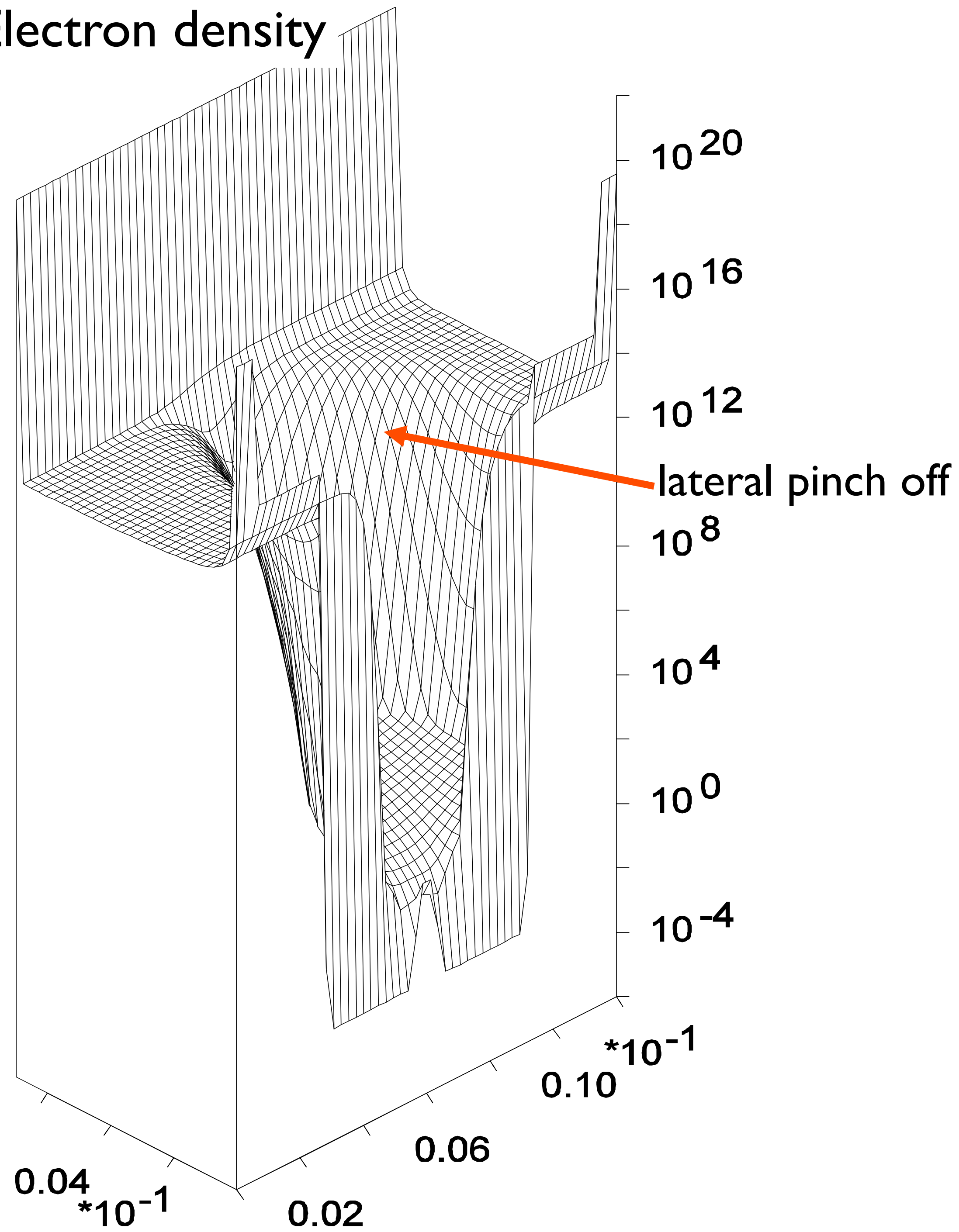
Small pixel size (~25μm)

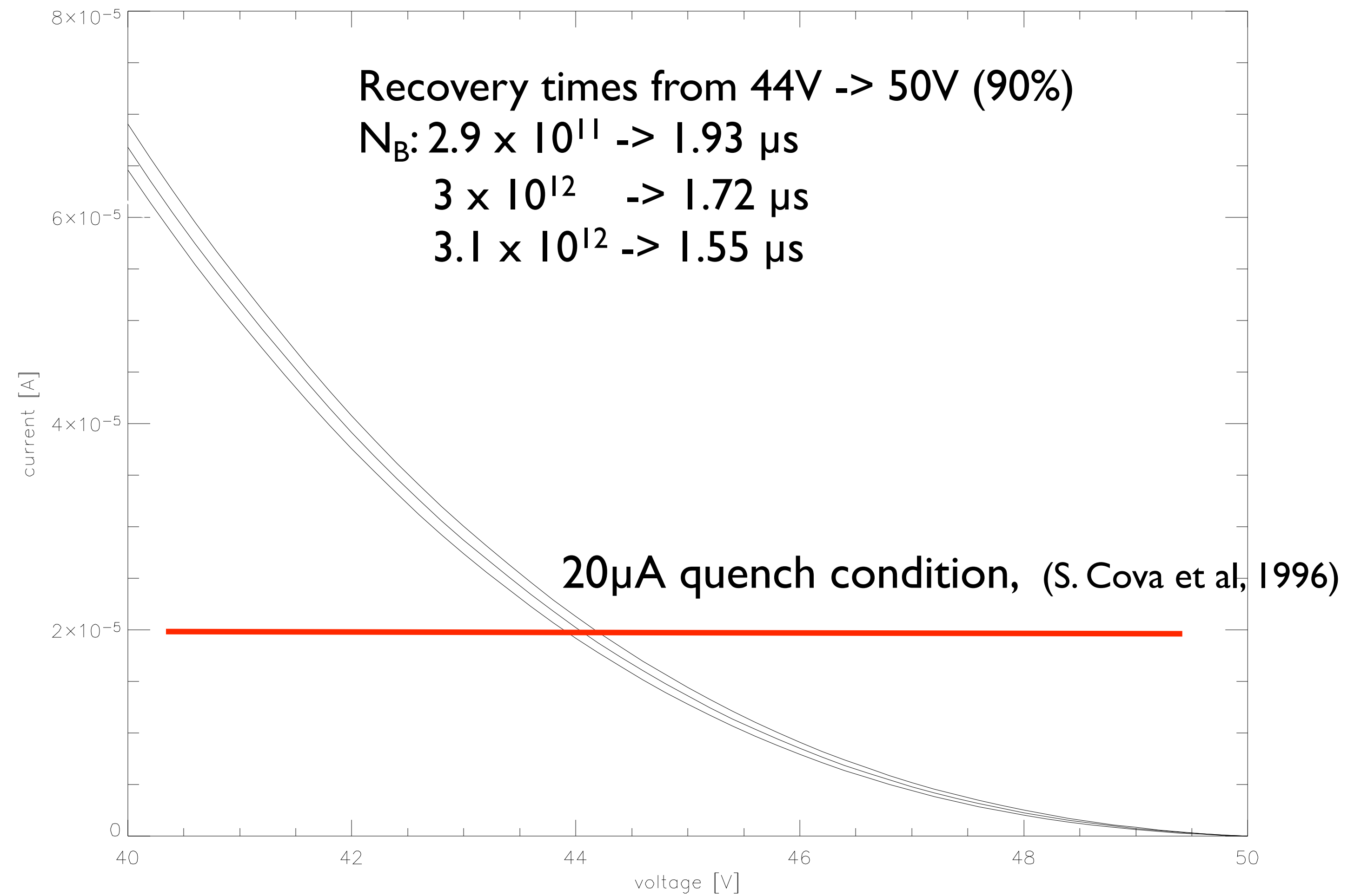
Smaller PDE
Big dynamical range

➔ in applications with scintillator coupling like calorimeters and PET scanners

Quench condition – parasitic JFET behavior

Electron density





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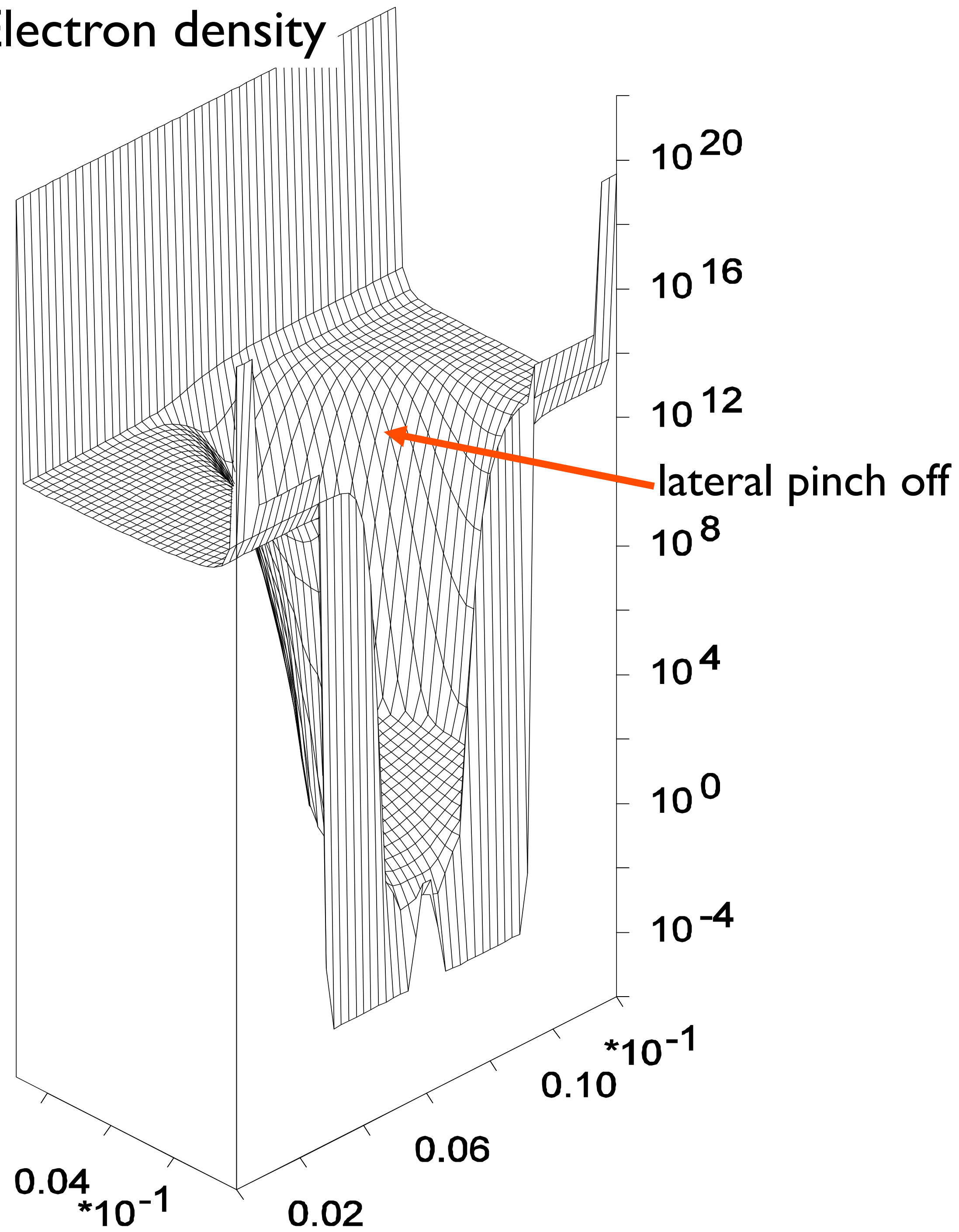
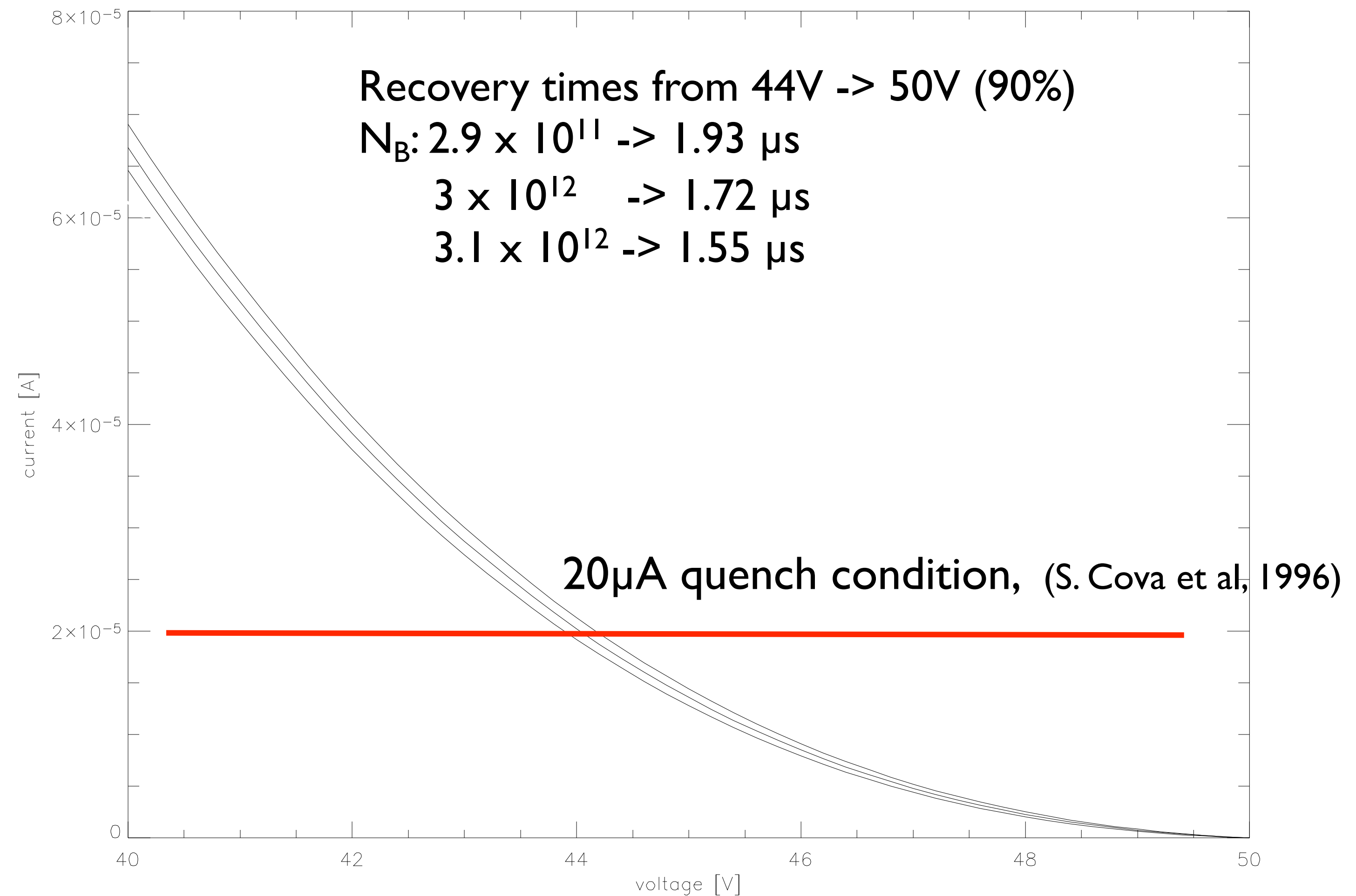
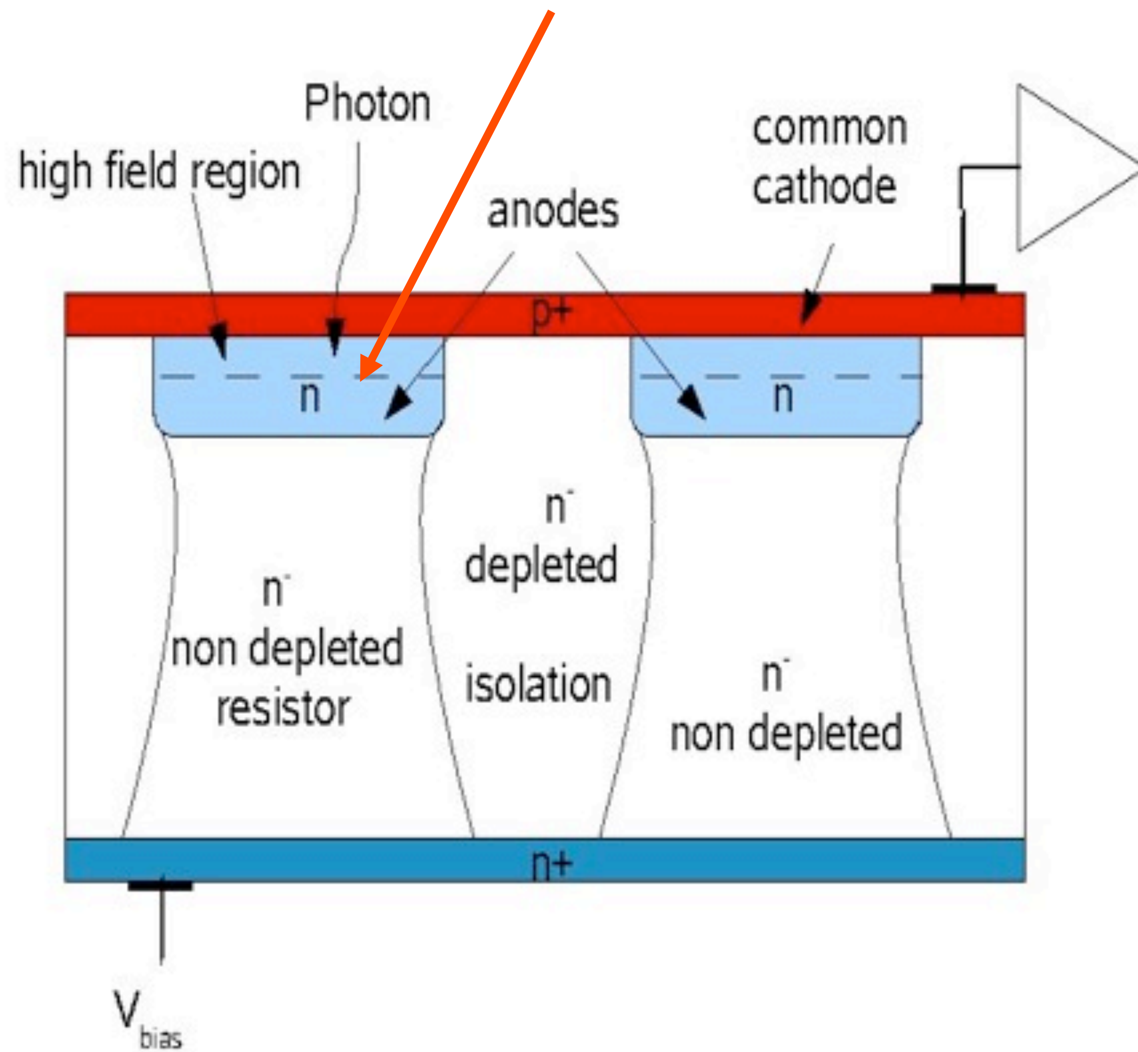




Recovery times by a factor 3 - 4 longer than with an optimally adjusted polysilicon resistor

Cross talk – bulk contribution

Highly doped high field region is a diffusion barrier for holes ($p\,n = n_i^2$)



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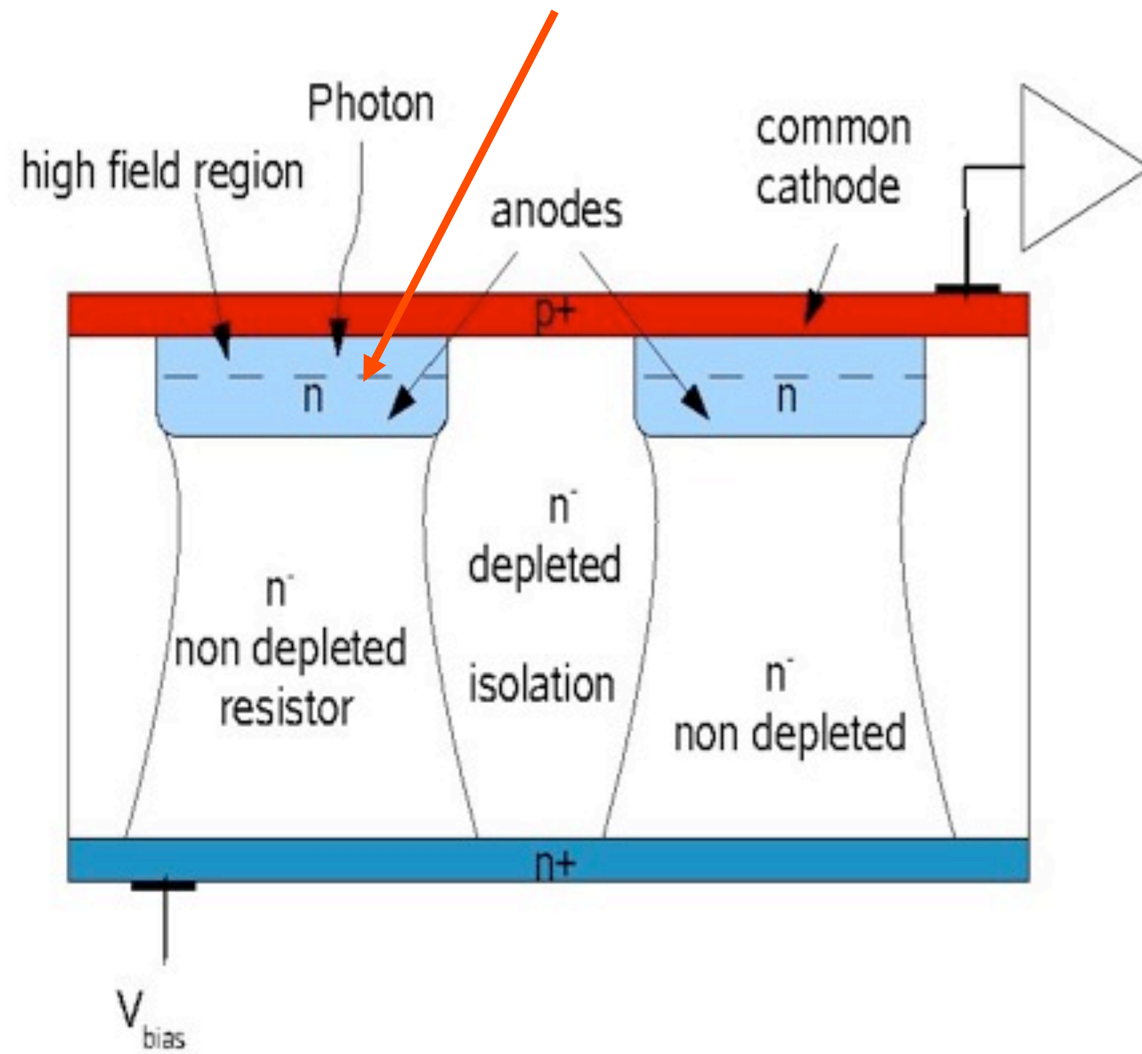
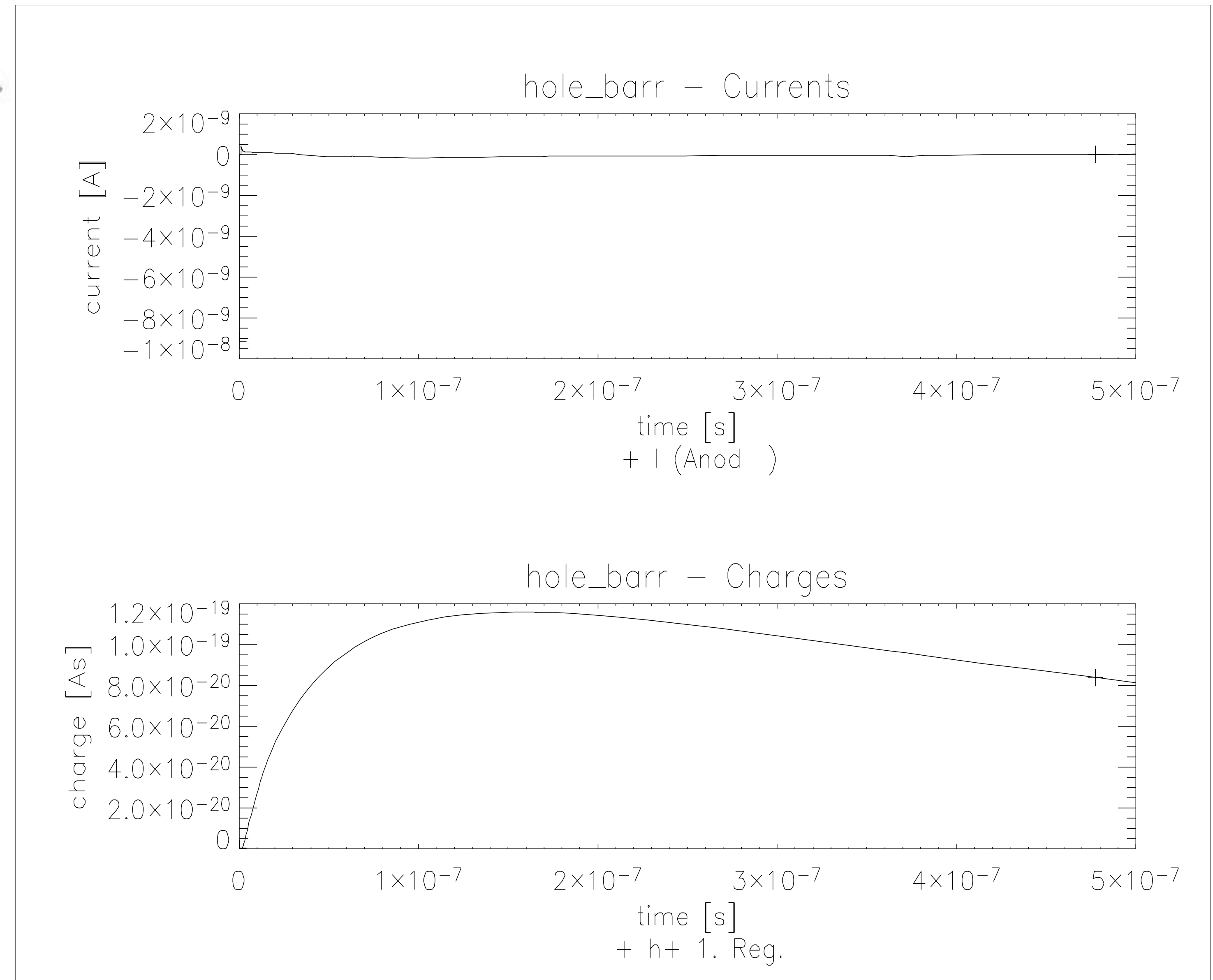


device simulation

generation of 1000e/h pairs in the bulk



Less than 1 hole in the high field region

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PDE estimation

- Hexagonal design pitch 150μm, isolation gap 20μm
  ➫ geomatrical fill factor 75%
- Optical entrance window: 90% @ 400nm
- Geiger efficiency : 90%

➫ PDE: 61% (depends strongly on gap size)

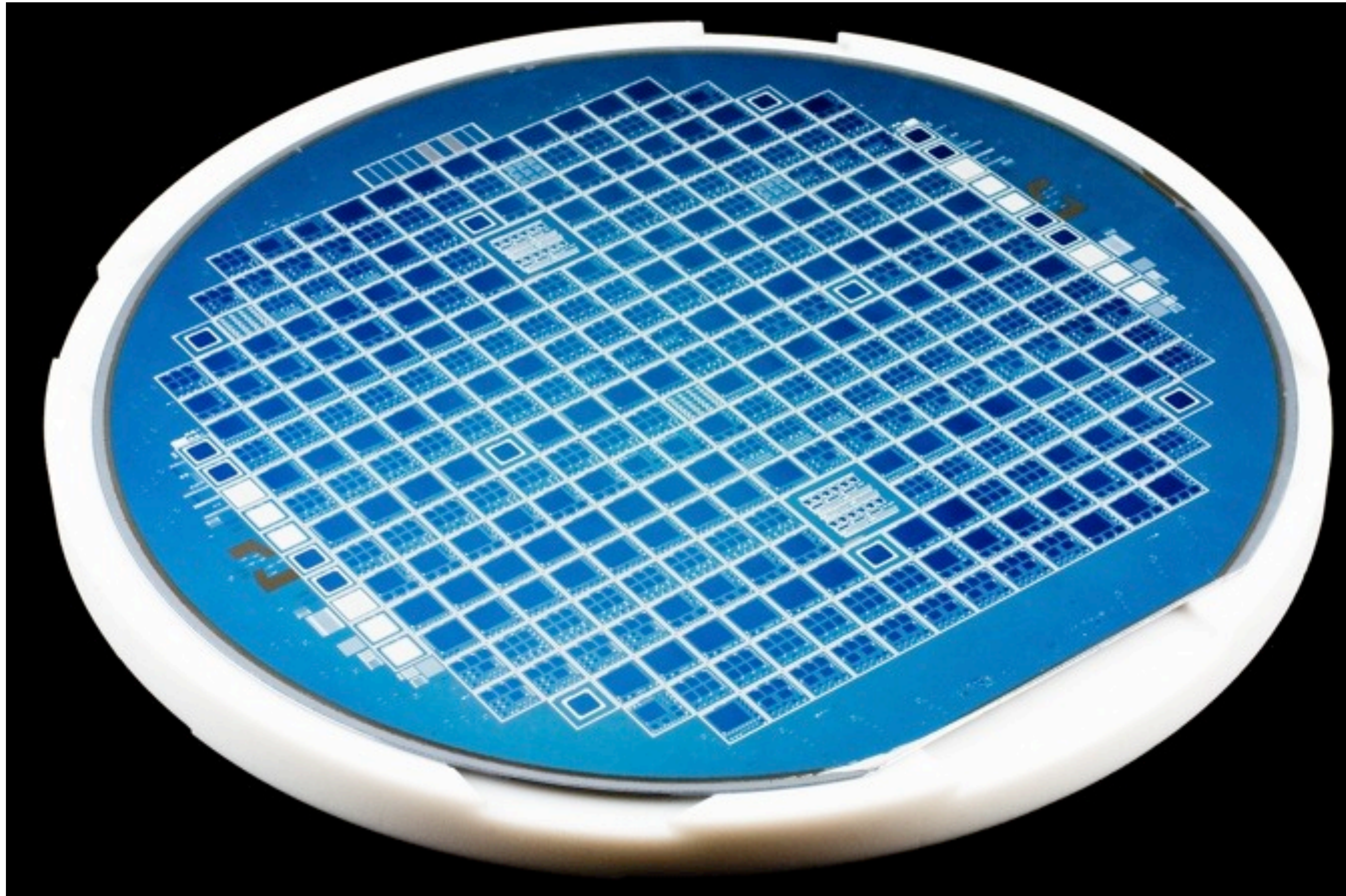
Pros and Cons

- **Advantages:**
  - no need of polysilicon
  - free entrance window for light, no metal necessary within the array
  - coarse lithographic level
  - simple technology
  - inherent diffusion barrier against minorities in the bulk -> less optical cross talk
  - hopefully better radiation hardness

- **Drawbacks:**
  - required depth for vertical resistors does not match wafer thickness
  - wafer bonding is necessary for big pixel sizes
  - significant changes of subpixel size requires change of material
  - vertical ‘resistor‘ is a JFET -> parabolic IV -> longer recovery times

Production

- 2.5 months total production time

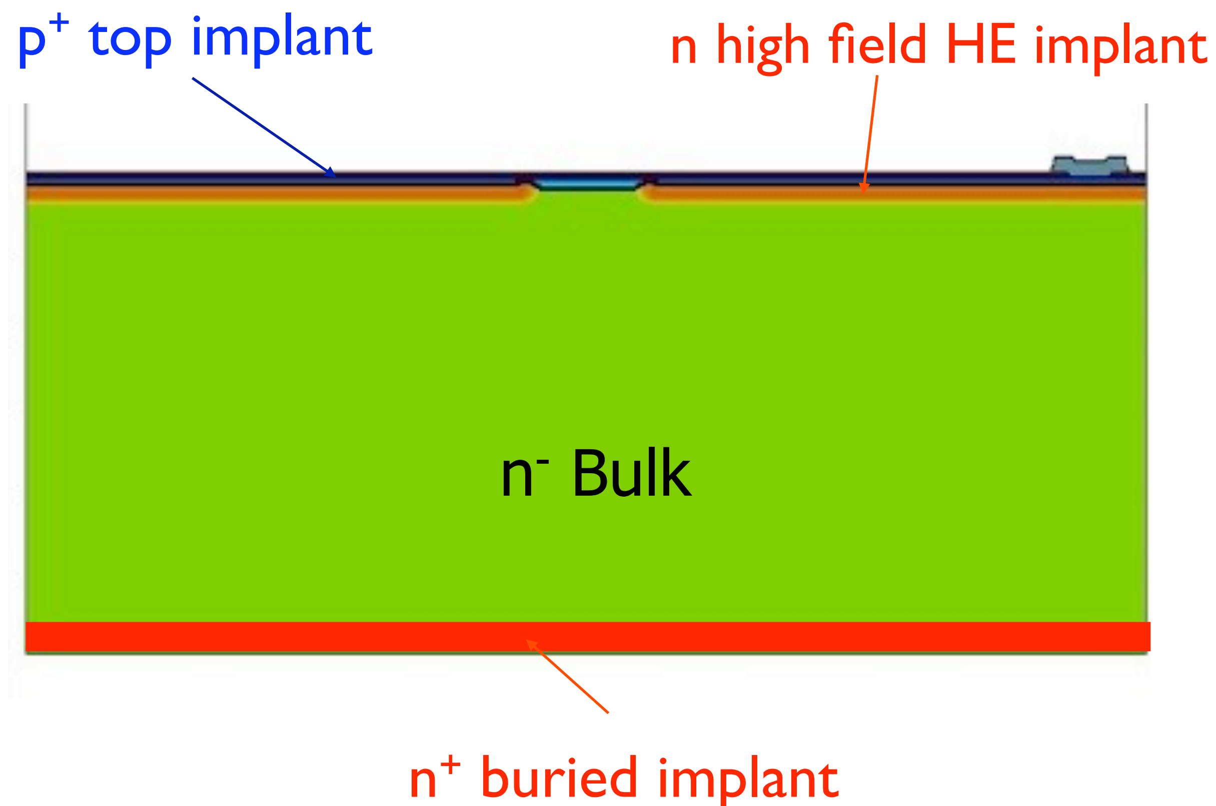


Proof of principle production

Simple technology

SOI material – 70µm
(wafer from TOPSIL, bonding at ICEMOS)

4 mask steps
- 2 implantations
- contacts
- metal



Hexagonal subpixel

Free entrance window for light without obstacles

Bulk doping variation of the top wafers

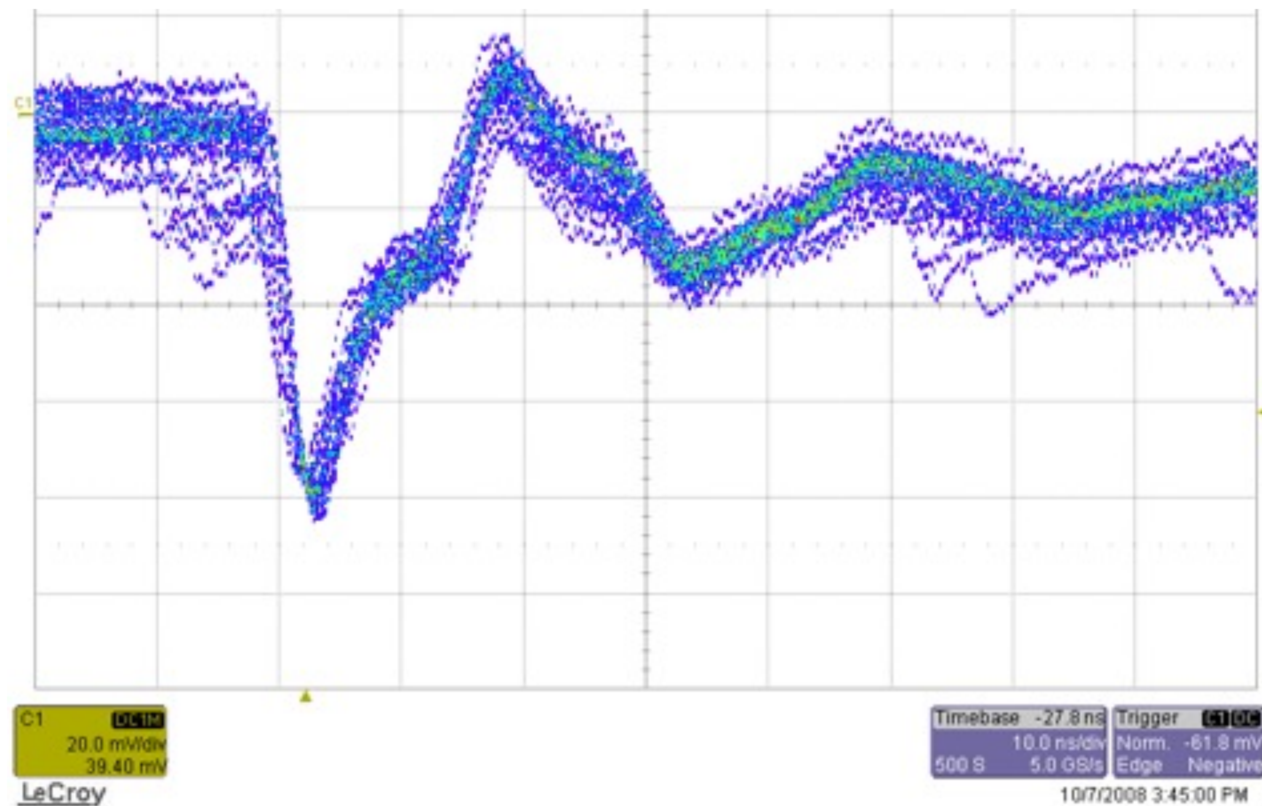
measured on 10 diodes (w/o high field implant) per wafer
(capacitance - voltage measurement)

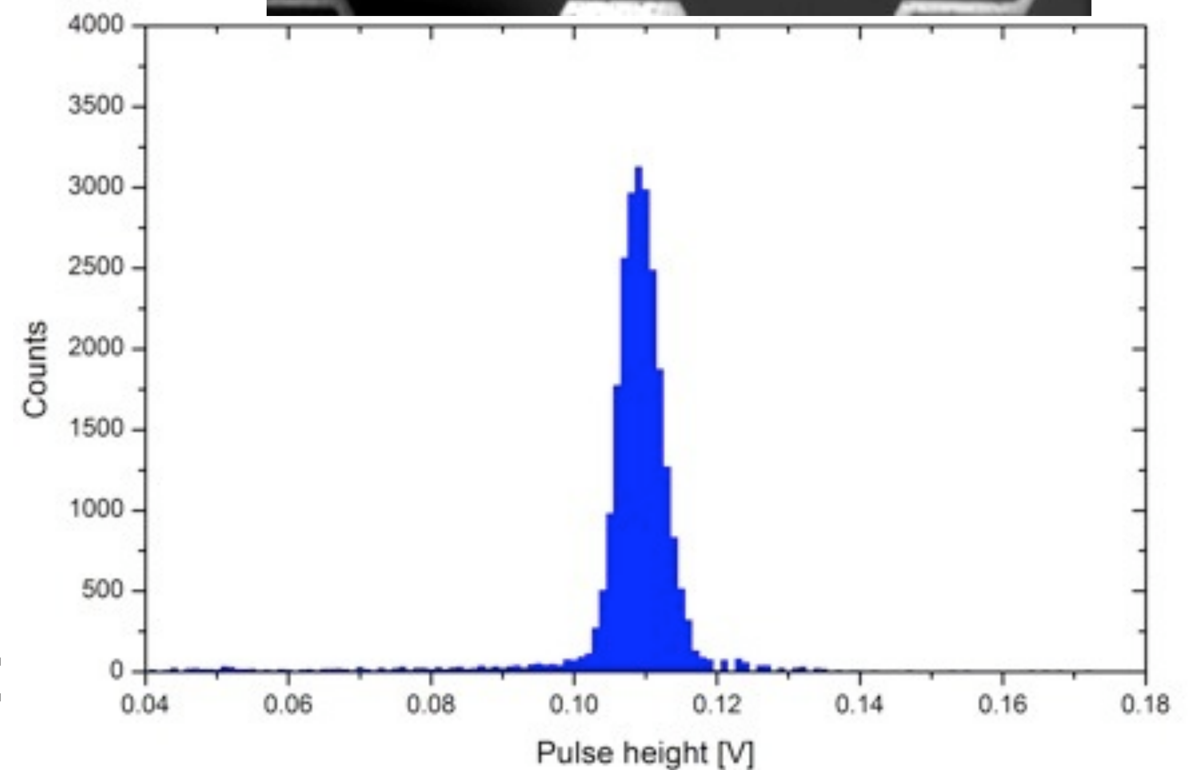
Wafer	Mean (cm^{-3})	Stdev (cm^{-3})
#737	2.87E+12	3.80E+10
#749	2.87E+12	3.40E+10
#739	2.64E+12	5.70E+10
#752	2.64E+12	3.10E+10

Proof of principle

Signals → Quenching works!

- 19cells , 3V overbias, RT, pitch 130μm, gap 14μm



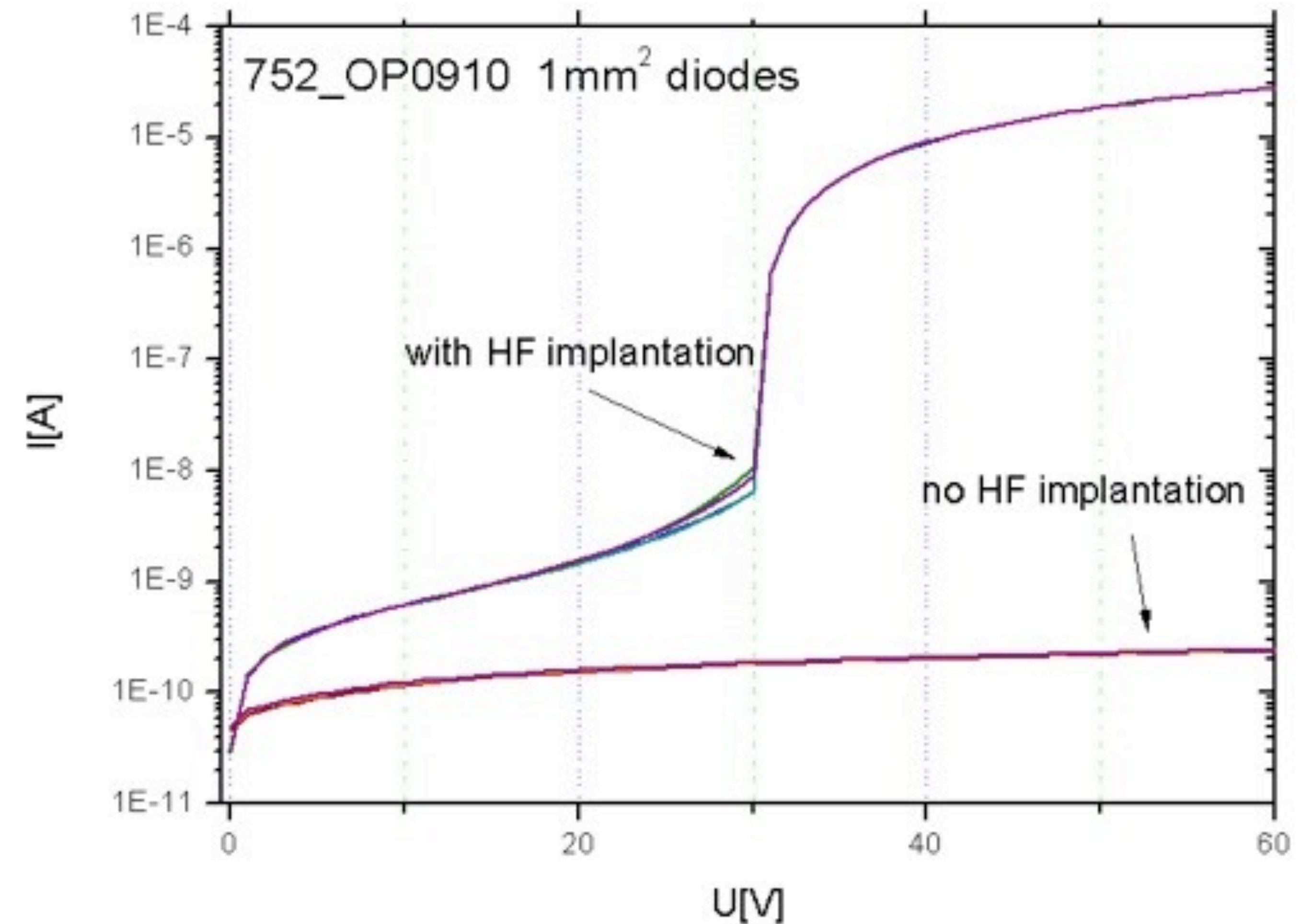


T = -46°C

Still some problems

- High leakage current (dark rate) – not sufficient annealing of the high field implant

- Edge breakdown
  due to a wrong tilt angle of the high field implant



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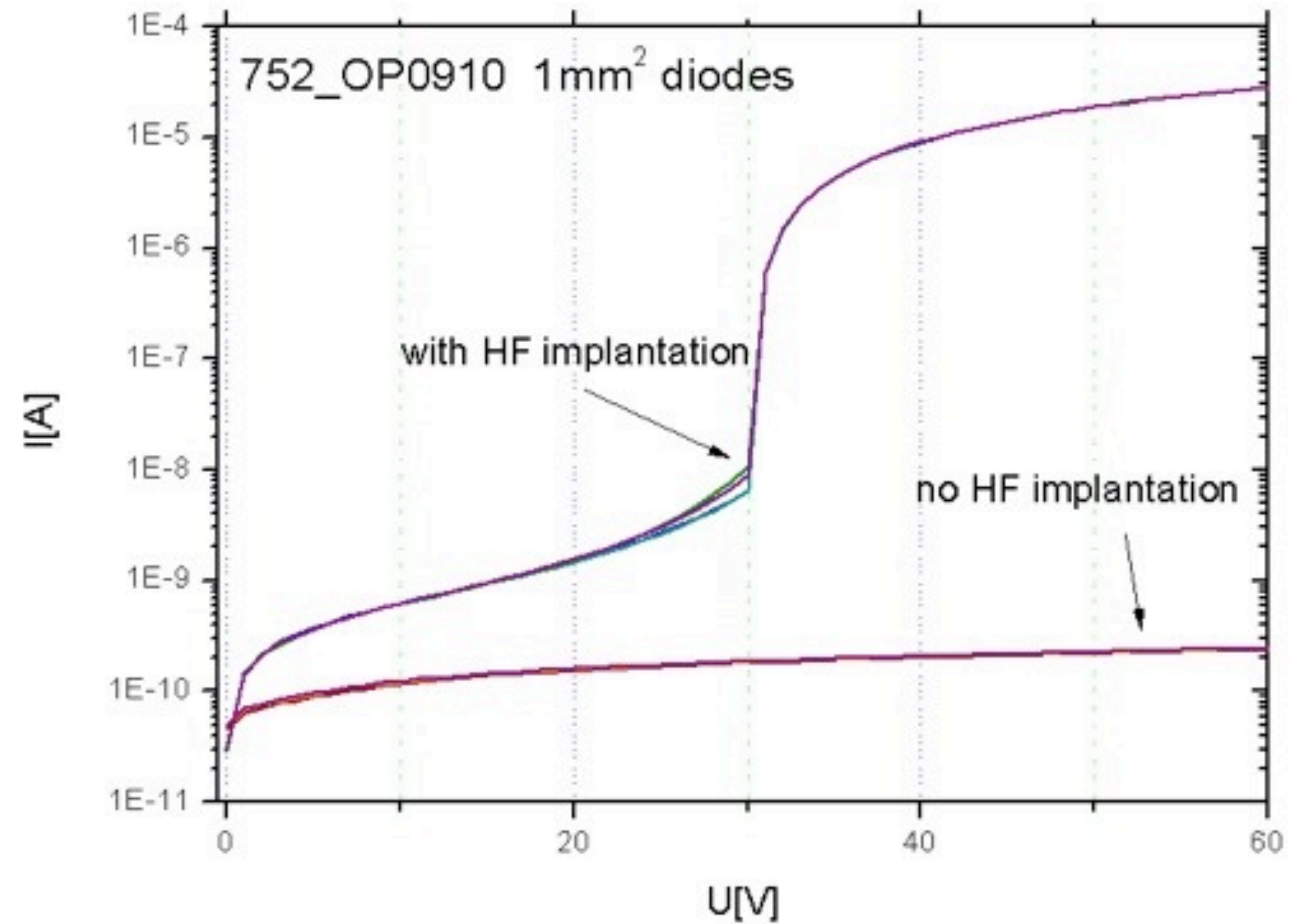

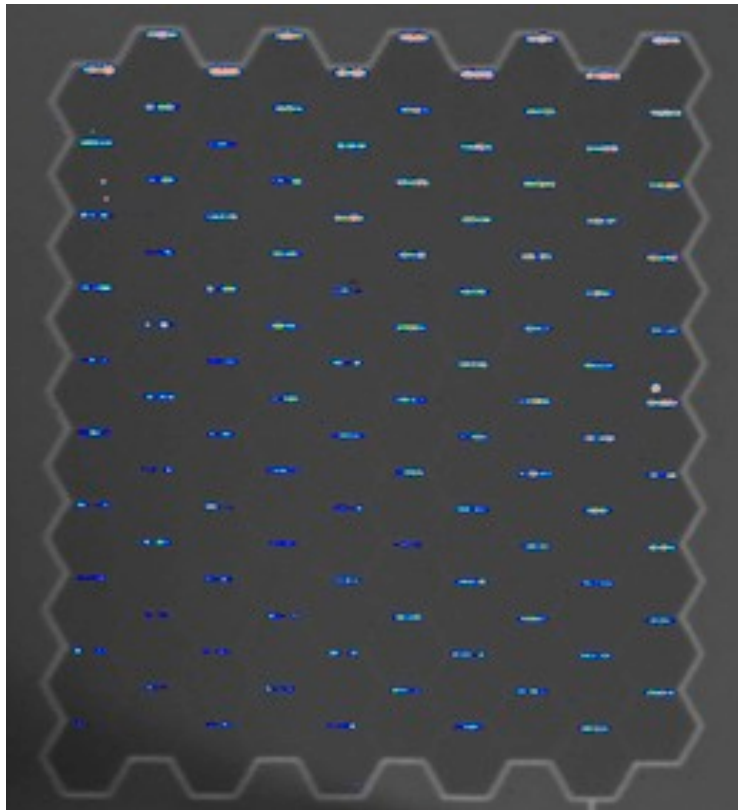

Thermal emission microscope picture

Summary

- New detector concept for the silicon photomultiplier array with individual quench resistors, integrated into the silicon bulk is proposed.
  - Required flexibility for quench resistor adjustment comes with wafer bonding technique (for small pixels an epitaxial layer is also suitable)
  - No polysilicon resistors, contacts and metal necessary at the entrance window
  - Geometrical fill factor is given by the need of cross talk suppression only
  - Very simple process, relaxed lithography requirements

    ➩ Cost reduction in mass production

- Proof of principle demonstrated – quenching works

- Next steps:
  - First prototype production is ongoing
  - Improving of dark rate and breakdown homogeneity