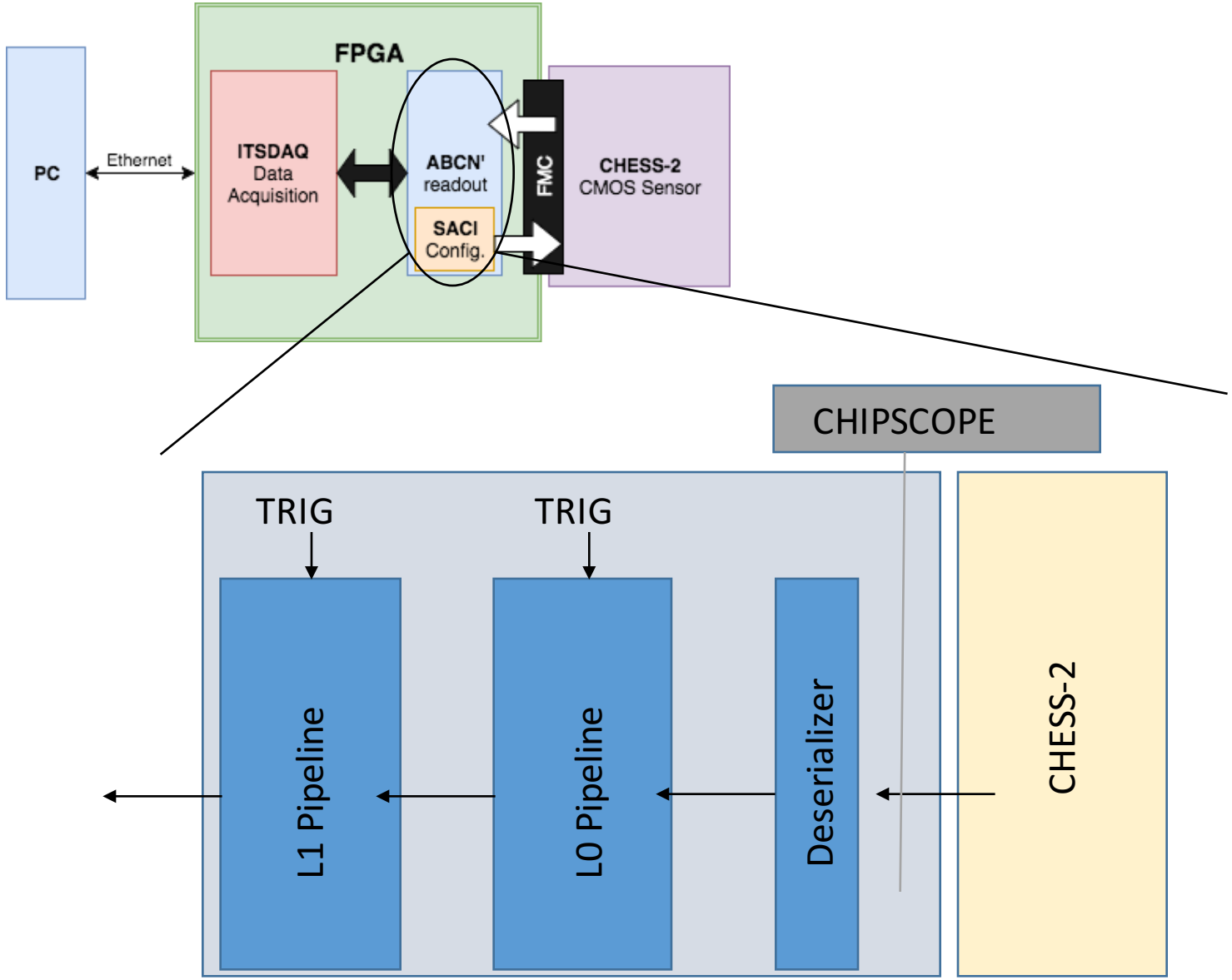
UBC CHESS-2 UPDATE

SLAC firmware build successful

- Thanks to Dionisio and Larry for helping us to figure that out

Test Mode Working Again

- Pietro suggested changing Wrd_1/ Wrd_2 to 3 [011]
  - Fixed the Test Mode functionality
- This is inconsistent with CHESS2_Spec_v1.6, which says Wrd_1/Wrd_2 should be set to 7 [111]
  - It would be great to document the functionality of these settings


PC
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FMC
CHESS-2
CMOS Sensor
CHIPSCOPE
TRIG
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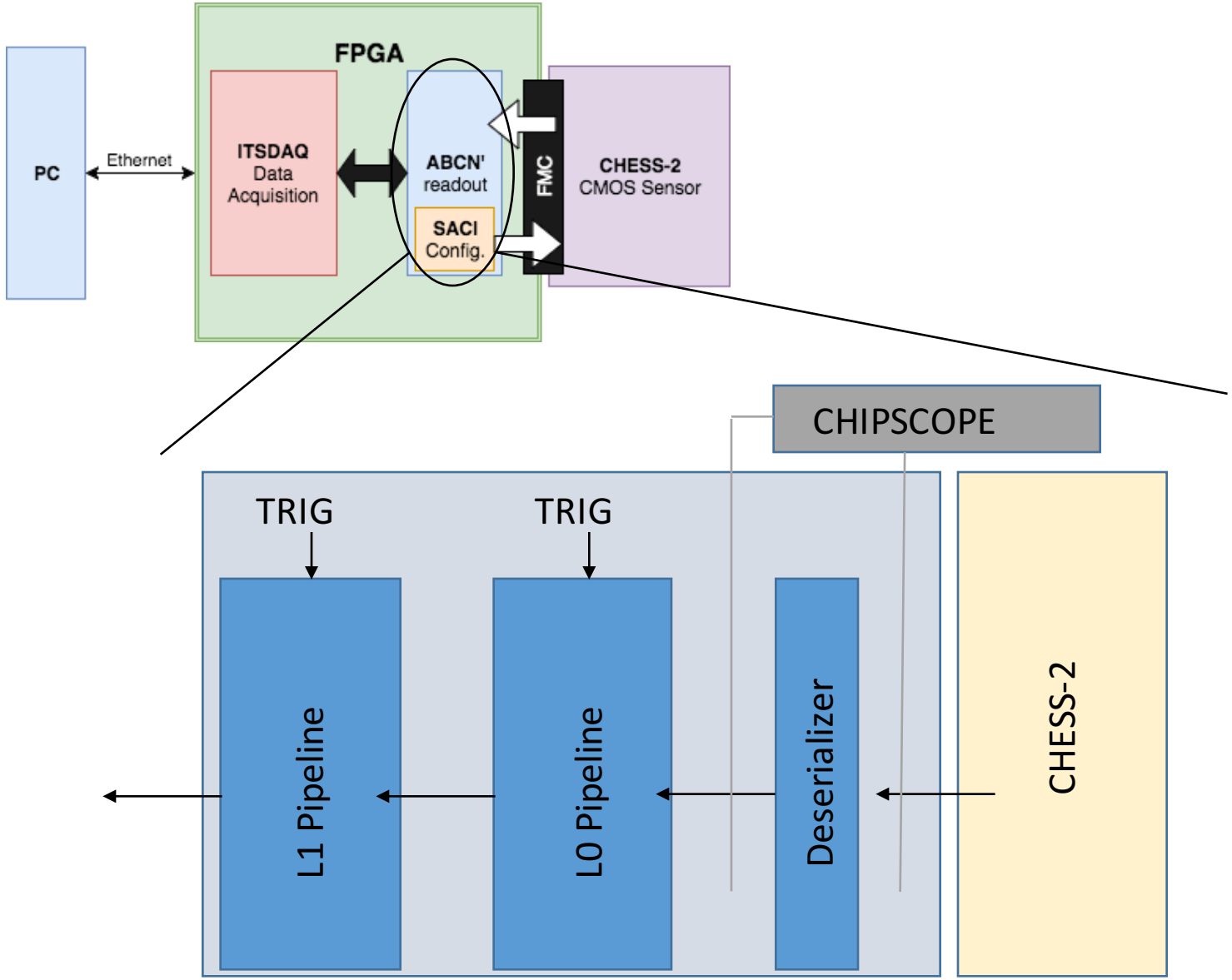
L1 Pipeline
L0 Pipeline
Deserializer
CHESS-2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Adding another ILA at next section of the pipeline breaks something

- We've checked the following manually with the oscilloscope
  - SACI_SEL
  - SACI_RESP
  - SACI_CMD
  - SACI_CLK
- According to both the oscilloscope and our software readout, most of the SACI commands are timing out with the 2-ILA configuration
  - Tried setting timeout to the max possible wait-time but it didn't solve anything
  - It's strange that some commands aren't timing out (i.e. select_row works, but select_column doesn't), however no real hypothesis of why this may be

SACI_CLK and SACI_CMD

Single ILA – not timing out

Two ILA's – timing out

- Note that the timing is extremely sketchy for both configurations
- Question: Is the data latched raising or falling edge of the SACI_CLK?

Hypothesis

- We believe that the timing is just barely working for the single ILA setup, and adding the second ILA throws it off just enough to break SACI
- We shifted the SACI_CLK phase by 180˚ to see if that fixes things
  - It made things worse, and most commands were timing out with both the single ILA and double ILA setup
- We are now attempting to force all SACI signals to be IOB registers in the firmware, but are running into some compilation issues (work in progress)
- We also are considering using a slower clock for SACI_CLK (now 4MHz)
  - Any suggestions for what frequency we might try?