Attachment 2/2009.02.12

Tasks descriptions and deliverables

---------- Adam Piotrowski/Grzegorz Jablonski ----------

Development of diagnostic system for ATCA Carrier Board ver. 1

Employees: A.Piotrowski (60%), D.Makowski (20%), G.Jabłoński (20%)

Task description: The aim of this task is to develop a set of applications to check correctness of each of the hardware subsystem located on ATCA Carrier Board ver. 1. Additionally, programs to test efficiency of communication components like PCIExpress bus, GigaBit Ethernet links and RocketIO links will be delivered.

Deliverables: A set of diagnostic and test application for PCIExpress subsystem, GBEthernet, RocketIO and additional peripheral devices located on ATCA v1 carrier board.

Total credit: ?? + 0 ke Required time: 3 mwks

Development of boot loader and operating system for PowerQUICC Mezzanine Board

Employees: A.Piotrowski (60%), D.Makowski (20%), G.Jabłoński (20%)

Task description: The aim of this task is to develop and install boot loader and operating system for mezzanine card with PowerQUICC processor and drivers for all required peripherals (memories, communication interfaces, real-time clock, etc…). The mezzanine card will be installed on the ATCA carrier board version 3 as RootComplex.

Deliverables: Boot loader application for PowerQUICC Mezzanine Board, set of configuration files and scripts for Linux kernel will be delivered.

Total credit: ?? + 0 ke Required time: 3 mwks

Development of DOOCS servers for carrier board ATCA v1

Employees: A.Piotrowski (100%)

Task description: In the frame of this task DOOCS server to manage ATCA Carrier Board ver. 1 will be designed and implemented.

Deliverables: C++ source codes for DOOCS servers responsible for management of ATCA Carrier Board ver. 1.

Total credit: ?? + 0 ke Required time: 3 mwks

Development of DMCS controller for PCIExpress-Integral Interface bridge

Employees: A. Piotrowski (50%), G. Jabłoński (50%)

Task description: The existing PCIe-II bridge will be extended with the DMA controller, whose control registers will occupy a separate BAR, allowing to program block transfers from the UserIP to host memory without the 2 microsecond latency overhead per every transferred word. Support for DMA transmission in Linux device driver will be implemented and appropriate performance tests will be performed.

Deliverables: A set of VHDL codes for Virtex V5 will be delivered. Example Linux device driver with DMA transmission will be developed.

Total credit: ?? + 0 ke Required time: 3 mwks

Design and installation of system to check radiation influence on microprocessor-based system (Atmega, Renesas, PowerQUICC, Virtex 5)

Employees: A.Piotrowski (100%)

Task description: During this task, system to check behavior of microprocessor-based systems working under radiation influence will be designed and installed in FLASH and Linac accelerator tunnels. Several types of advanced microprocessor families, like 32-bit ATmega, Renesas and PowerQUICC, will be tested. In addition, Software Implemented Hardware Fault Tolerance radiation mitigation techniques will be implemented to check, in real radiation environment, protection ability of SIHFT algorithms. Achieved results will be used to find adequate radiation protections solutions for X-FEL accelerator.

Deliverables: Results of radiation influence on microprocessor with special consideration for microprocessor families that will be used in X-FEL projects.
Total credit: ?? + 4 ke Required time: 8 mwks

Design and implementation of PCIE HotPlug support for Carrier Board Linux kernel

Employees: A.Piotrowski (75%), D.Makowski (10%), G.Jabłoński (15%)

Task description: HotPlug is a mechanism that allows users to replace devices connected to PCIExpress bus without turning off the power. It must be supported by hardware and kernel operating system. In the frame of this task set of Linux operating system kernel patches implementing HotPlug support for FPGA devices connected to AMC bays will be proposed. This task is critical for development of AMC devices because eliminate necessity of device restart after every FPGA programming.

Deliverables: Set of kernel patches and applications to enable PCIExpress HotPlug functionality for FPGA devices connected to PCIExpress bus.

Total credit: ?? + 0 ke Required time: 3 mwks

Advanced buffering with application of interrupts for data acquisition with TAMC900 module (FPGA)

Employees: **Dariusz Makowski (40%), Grzegorz Jabłoński (40%), Sergiusz Szachowalow (20%)**

Task description: The aim of this task is to develop an advanced buffering system on the TAMC900 module, allowing to store the ADC samples from the entire 2 ms pulse in the exernal SRAM memory and transfer it via the PCI Express link between the pulses.

Deliverables: VHDL code implementing the functionality.

Total credit: ?? + 0 kE Required time: 4 mwks

ATCA-carrier board firmware download controller

Employees: **Dariusz Makowski (25%), Student (25%), Grzegorz Jabłoński (25%), Adam Piotrowski (25%)**

Task description: The aim of this task is to develop a system for downloading of firmware into various components of ATCA carrier boards and AMC modules. The bitstream will be downloading via Ethernet.

Deliverables: A project and prototype of the system will be delivered. C/C++ codes and hardware required for the controller will be delivered (hardware is yet known, processor or FPGA).

Total credit: ?? + 0 kE Required time: 4 mwks

Advanced buffering with application of interrupts for data acquisition with TAMC900 module (Root Complex)

Employees: **Adam Piotrowski (40%), Grzegorz Jabłoński (40%), Student (20%)**

Task description: The aim of this task is to develop an advanced buffering system on PCIE linux driver for the TAMC900 module, allowing to store the ADC samples from the entire 2 ms pulse in the exernal SRAM memory and transfer it via the PCI Express link between the pulses.

Deliverables: C source for device driver implementing the functionality.

Total credit: ?? + 0 kE Required time: 2 mwks

Development of operating system and low level drivers for new external carrier board

Employees: **Adam Piotrowski (50%), Dariusz Makowski (25%), Grzegorz Jabłoński (25%)**

Task description: The aim of this task is to develop and install appropriate version of Linux operating system suitable for our purpose for new ATCA carrier board, compile and test PCIE device drivers and PCIE-to-Ethernet Server.

Deliverables: Working version of operating system for carrier board suitable for our purpous and source codes for PCIExpress driver and PCIE-to-Ethernet Server adjusted for new version of carrier board.

Total credit: ?? + 0 kE Required time: 3 mwks

Implementation of publisher-subscriber mechanism in PCIExpress communication subsystem

Employees: **Adam Piotrowski (40%), Grzegorz Jabłoński (40%), Student (20%)**

Task description: Publisher-subscriber is programming paradigm in which many clients (subscribers) want to listen the same information published by one server (publisher). In PCIExpress communication subsystem PCIE-to-Ethernet Server can work as Publisher and several external application like i.e. DOOCS servers can work as Subscribers. In that model correctly configured server will periodically send data read from PCIE device directly to interested servers without unnecessary read request from each of the clients. For relatively small systems, this solution provides better scalability then traditional client-server model.

Deliverables:

1. C source code for PCIE-to-Ethernet Server with implemented publisher-subscriber functionality,
2. C++ source code for High Level Application PCIE library with implemented publisher-subscriber functionality.

Total credit: ?? + 0 kE Required time: 3 mwks

Evaluation of TINE environment

Employees: **Adam Piotrowski (60%), Student (40%)**

Task description: The aim of this task is to evaluate usefulness of TINE control software for ATCA based system.

Deliverables: Example TINE client and server control application for ATCA v1 carrier board

Total credit: ?? + 0 kE Required time: 4 mwks

---------- Wojciech Cichalewski ----------

The HLA realization as a middle layer (satellite) servers.

Employees:Wojciech CICHALEWSKI (100%)

Task description:

The aim of this task is to develop the idea of the High Level Applications implementation as a set of the middle layer servers. Individual RF Station has to be equipped with the HLA functionality. In the development stage each algorithm can be implemented as a Matlab script. Nevertheless the final versions should be integrated with the Control System and should be suitable for the maintenance by the Control System expert. The proposition of HLA implementation as a set of middle layer servers for one RF station will be developed and programmed.

Deliverables:

1. The High Power Amplifier Chain characterization tool realized as a DOOCS middle layer server – source codes.
2. The High Power Amplifier Chain linearization tool realized as a DOOCS middle layer server – source codes.
3. The Beam Loading Compensation application realized as a DOOCS middle layer server – source codes.
4. The Adaptive Feed Forward application realized as a DOOCS middle layer server – source codes.

Total credit: 8,57 + 0 kE Required time: 8 mwks

Diagnostic HLA implementation and evaluation in the ATCA based system.

Employees: Wojciech CICHALEWSKI (100%)

Task description:

The aim of this task is to implement and evaluate diagnostic high level applications in ATCA based system. Currently the ATCA based system of LLRF System is being installed in one of FLASH RF Station. The diagnostic functionality available for the regular RF station system users has to be provided also for this version of the system. The DOOCS servers and Matlab script based applications will be available for the system operators during the summer 2009 ATCA system evaluation.

Deliverables:

1. The source code in C++ and Matlab of diagnostic applications for ATCA evaluation tests.
2. GUI source codes and user manual documentation for diagnostic applications.

Total credit: 6.43 + 0 kE Required time: 6 mwks

The operation procedures revision for the ATCA based system.

Employees: Wojciech CICHALEWSKI (100%)

Task description:

The aim of this task is to provide documented set of procedures necessary for the operation of the ATCA based LLRF System. The procedures for system start-up, experiments parameters settings, system short-time work brake, system shut-down, system recovery after interlock will be revised, modified, documented and verified in FLASH.

Deliverables:

1. Documented procedures for the LLRF system operation for the Summer 2009 ATCA evaluation

Total credit: 2.14 + 0 kE Required time: 2 mwks

---------- Wojciech Cichalewski ----------

---------- Bartek Sakowicz ----------

Analysis of data structures used in DOOCS servers

Employees: **Marek Kaminski (60 %), Bartosz Sakowicz (40 %)**

Task description: The aim of the task is to analyze as much as possible different DOOCS configuration files in order to find all data types used to describe calibration parameters

Deliverables: Report representing collected data

Total credit: x + x ke Required time: 2 mwks

System specification

Employees: **Bartosz Sakowicz (100 %)**

Task description: Task focuses on gathering client requirements including application usage scenarios, client interaction with the application and client requirements for future development not covered by this project. Requirements gathered need to be analyzed for possible logic errors, conflicting use case scenarios.

Deliverables: Report representing detailed idea of the system and user interface functionalities

Total credit: x ke Required time: 2 mwks

Data modeling

Employees: **Marek Kaminski (40%), Piotr Mazur (40%), Bartosz Sakowicz (20%)**

Task description: Users requirements need to be processed in order to select appropriate storage method for application data and additional methods for storage dynamic model changes that cannot be easily represented by relational database structures. Conceptual data model is used to devise entity-relationship diagram for use in database environment. Data is divided into single entities, and relations between entities. After conceptual data model processing a relational model is built that can be implemented by any relational database management system.

Deliverables: Entity-relationship diagram

Total credit: x ke Required time: 2 mwks

Database implementation

Employees: **Piotr Mazur (70%), Bartosz Sakowicz (30%)**

Task description: Entity-Relationship diagram is used to implement devised database schema in existing database management system. Data is being represented as tables, relationships are being represented as foreign keys and additional database constraints are added. Data is being normalized in order to avoid data duplication. Fully functional

database consists also of additional constraints (such as unique and check constraints). Database schema is being optimized given the criteria acquired from client requirements document. Additional database indexes are created.
Deliverables: Optimized database schema
Total credit: xke Required time: 1 mwks

Data access layer implementation

Employees: **Marek Kaminski (50%), Piotr Mazur (25%), Bartosz Sakowicz (25%)**
Task description: Data access layer is responsible for mapping between object-oriented application and relational database. All typical database operations (select, update, insert, delete) are wrapped by classes and methods
Deliverables: Java code - DAO classes
Total credit: xke Required time: 2 mwks

Service layer implementation

Employees: **Bartosz Sakowicz (60%), Marek Kaminski (30%), Piotr Mazur (10%)**
Task description: Service layer is responsible for implementation of all logic related to application. It is a bridge between user interface and DAO classes. Special attention must be put on communication part between application and DOOCS servers.
Deliverables: Java code - service layer classes
Total credit: xke Required time: 8 mwks

View and controller layer implementation

Employees: **Bartosz Sakowicz (70%), Marek Kaminski (30%)**
Task description: User interface and flow of control implementation
Deliverables: Java code - JSP pages and controller classes
Total credit: xke Required time: 6 mwks

Example DOOCS server implementation

Employees: **Piotr Mazur (100%)**
Task description: Example "dummy" DOOCS server must be implemented. Especially read and write methods must be overloaded in case to cooperate not only with configuration file but also with database with usage of some distributed protocol.
Deliverables: DOOCS server cooperating with calibration database. Report describing way of overloading read and write methods in future developed DOOCS servers (maybe some abstract classes and/or additional helper methods)
Total credit: xke Required time: 3 mwks

Application testing

Employees: **Bartosz Sakowicz (50%), Piotr Mazur (25%), Marek Kaminski (25%)**
Task description: Application must have set of testing procedures. It will be proof of correct application work as well as very good tool for future modifications
Deliverables: Java code - set of JUnit testing procedures
Total credit: xke Required time: 2 mwks

Application deployment

Employees: **Piotr Mazur (100%)**
Task description: Deployment on Desy servers.
Deliverables: Fully working application.
Total credit: xke Required time: 1 mwks

Time Sheet System: server installation and application deployment

Employees: **Bartosz Sakowicz (100%)**

Task description: Installation of all needed software on newly bought server (operating system, web server, application server, database server, security issues). Time Sheet System deployment. Backup procedures implementation.

Deliverables: Time Sheet System installed on new server.

Total credit: x + x ke Required time: 1 mwks

Work + hardware

TTS server administration

Employees: **Bartosz Sakowicz (100 %)**

Task description: Administration of TSS server

Deliverables: Continuous working of TTS.

Total credit: x ke Required time: up to 10 hours/each month

TTS improvements

Employees: **Bartosz Sakowicz (100%)**

Task description: Improvements to current version of TTS.

Deliverables: TTS improved

Total credit: x ke Required time: ??? mwks (will be precised before 20th of January)

---------- Szymon Tarnowski ----------

Development of AMC digital vector modulator board

Employees: **Szymon Tarnowski (90%) Dariusz Makowski (10 %)**

Task description: The aim of this task is to develop DVM board from level of schematic diagram to assembled and tested physical board.

Deliverables:

1. Design and assembly AMC-DVM board
2. Prepare and use simple firmware for testing components installed on board

Total credit: 2.5 + 4 kE Required time: 7 mwks

Development of firmware for AMC-DVM

Employees: **Szymon Tarnowski (90%) Adam Piotrowski (10 %)**

Task description: The aim of this task is to prepare firmware needed for operations of AMC-DVM board in accelerator controlling system environment.

Deliverables:

1. FPGA firmware (PCIe communications, IQ data transmition from controller)
2. DOOCS server/panel for configuration and management of AMC-DVM board

Total credit: 3.21 + 0 kE Required time: 9 mwks

Measurement of important parameters of AMC-DVM

Employees: **Szymon Tarnowski (100%)**

Task description: The aim of this task is to measure AMC-DVM board in laboratory and in accelerator controlling system.

Deliverable: Report on parameters and operation of AMC-DVM board;

Total credit: 1.07 + 0 kE Required time: 3 mwks

---------- Konrad Przygoda ----------

Preparation of requirements for ATCA carrier board dedicated for piezo

PhD students: **Konrad Przygoda (100%)**

Task description: The aim of this task is to help to create comprehensive requirements descriptions for ATCA based piezo control system.

Deliverables: The requirements for ATCA carrier board dedicated for piezo will be delivered in Enterprise Architect.

Total credit: 1.43 ke+ 0 ke Required time: 4 mwks

ATCA carrier board dedicated for piezo

PhD students: **Konrad Przygoda (50%)**

Employees: **Dariusz Makowski (50 %)**

Task description: The aim of this task is to design and fabricated the pcb board integrated with ATCA standards dedicated for piezo control system.

Deliverables: The pcb board (ATCA carrier) will be delivered.

Total credit: 5,71 ke+ 10 ke Required time: 8 mwks

Control software for ATCA carrier board dedicated for piezo

PhD students: **Konrad Przygoda (75%)**

Employees: **Dariusz Makowski (25 %)**

Task description: The aim of this task is to implement piezo control software for designed carrier board. The system should be able to driver 32 piezos as well as sensed 32 piezos.

Deliverables: The piezo control software for ATCA carrier board dedicated for piezo controller will be delivered.

Total credit: 4.29 ke+ 0 ke Required time: 4 mwks

DC/DC converter for ATCA carrier board dedicated for piezo

Employees: **Tomasz Pozniak (85%)**

PhD students: **Konrad Przygoda (15%)**

Task description: The aim of this task is to design the DC/DC converter for designed piezo carrier board. The system should be able to provide power supply for piezo drivers.

Deliverables: The DC/DC converter integrated into the Carrier board dedicated for piezo will be delivered.

Total credit: 4.82 ke+ 4 ke Required time: 5 mwks

---------- Wojciech Jałmużna ----------

VCO mode of operation for the controller

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to prepare the modules and configuration for the controller application, which will allow to use VCO mode of operation.

Deliverables: Controller modules and configuration files allowing the VCO operation

Total credit: 1 ke Required time: 4 mwks

Controller sources configuration system

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to prepare the new easy to use system for the configuration of the controller's sources.

Deliverables: The new framework for the controller, which allows easier configuration changes with all the modules and functionalities implemented.

Total credit: 0.5 ke Required time: 2 mwks

Technical documentation for the controller application

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to prepare full technical documentation for all parts of the controller.

Deliverables: Technical documentation for the controller project

Total credit: 1 ke Required time: 4 mwks

Controller evaluation in ATCA demonstration system

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to test the controller application in ATCA demonstration system at FLASH

Deliverables: Test report with the summary of performed measurements

Total credit: 0.75 ke Required time: 3 mwks

Vertical Test Stand controller development

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to prepare the controller for the VTS based on the prototype tested in second half of 2008.

Deliverables: Additional modules and configuration files for the controller used in VTS

Total credit: 0.75 ke Required time: 3 mwks

ATCA carrier board ver.2 debugging and drivers implementation

Employees: Wojciech Jalmuzna (100%)

Task description: The goal of this task is to debug new ATCA carrier board and prepare all the necessary drivers for the new peripherals.

Deliverables: Detailed report and suggestions for next generation of carrier and VHDL files for peripheral drivers.

Total credit: 0.75 ke Required time: 3 mwks

---------- Dariusz Makowski ----------

Collaboration

Dariusz Makowski

Task description: Management of the people on DMCS and DESY sites and supervision of cooperation with other partners

Deliverables: Paper work: agreements, verification of deliverables and acceptance tests, reports, etc…

Total credit: ke Required time: 5 mwks

Design of the second version of AMC_B universal module

Employees: **Dariusz Makowski (80 %), Piotr Krasiński (20 %)**

Task description: The aim of this task is design the second version of the universal AMC module according to agreed with DESY specification that will be used together with VM, timing and RadMon modules.

Deliverables: Schematic diagrams, PCB design, documentation and gerber files will be. Preparation of the initial requirements for AMB_C and discussion with other people responsible for VM, timing and RadMom module is a part of this deliverable.

Total credit: xxxx ke Required time: 8 mwks

Debugging, drivers implementation and test programs for second version of AMC_B module

Employees: **Dariusz Makowski (40%), Grzegorz Jabłoński (40%), Paweł Prędki (20%)**

Task description: The aim of this task is assemble and debug the exemplary AMC_B module.

Deliverables: C/C++ and VHDL codes, drivers, useful test programs and report for second version of AMC_B module will be delivered.

Total credit: xxxx ke Required time: 6 mwks

Debugging of the RootComplex module with Freescale procesor

Employees: **Dariusz Makowski (50%), Grzegorz Jabłoński (50%)**

Task description: The aim of this task is assemble and debug the RC module.

Deliverables: C/C++ and VHDL codes, drivers, useful test programs and report for RC module will be delivered.

Total credit: xxxx ke Required time: 6 mwks

Improvement and implementation of new features for the IPMC controller

Employees: **Dariusz Makowski (20%), Paweł Prędki (80%)**

Task description: The aim of this task is prepare the missing functionality of the IPMC controller for ATCA carrier board, eg. E-Keying, Power checking, Periodic sensor reading, etc...

Deliverables: C/C++ codes extending functionality of IPMC for ATMEGA and Renesas microcontrollers will be delivered.

Total credit: xxxx ke Required time: 8 mwks

Improvement and implementation of new features for the MMC controller

Employees: **Dariusz Makowski (20%), Paweł Prędki (80%)**

Task description: The aim of this task is prepare the missing functionality of the MMC controller for AMC moduled, eg. E-Keying, Power checking, Periodic sensor reading, etc...

Deliverables: C/C++ codes extending functionality of MMC for ATMEGA microcontroller will be delivered.

Total credit: xxxx ke Required time: 6 mwks

Software for semi-automatic generation of complex symbols with huge number of pins for Mentor Graphics DxDesigner

Employees: **Dariusz Makowski (50%), Wojciech Jałmużna (50%)**

Task description: The aim of this task is to write the application for semi-automatic generation of symbols for Mentor Graphics DxDesigner program. The application will read file with all signals names and pin numbers assigned to various banks and generate collection of symbols, one symbol for every bank. A second, similar application will be developed to automatically generate symbols for Xilinx FPGA. The application will use CVS files provided by Xilinx.

Deliverables: C/C++ code for for Windows/Linux operating systems will be delivered.

Total credit: xxxx ke Required time: 2 mwks

Preparation of ATCA-based controller for tests in September

Employees: **Dariusz Makowski (25%), Wojciech Jałmużna (25%), Grzegorz Jabłoński (25%), Adam Piotrowski (25%)**

Task description: The aim of this to prepare ATCA carrier boards, AMC modules, RTM modules with down converters and required firmware and application (written earlier) for the planned tests of the ATCA-based LLRF controller.

Deliverables: A set of customized firmware for FPGA and application for PC computers or blades will be delivered. Report from the test will be delivered.

Total credit: xxxx ke Required time: 6 mwks

Hardware production PCB

Employees: **ITR**

Task description:

Deliverables:

Total credit: 14 ke Required time: 0 mwks

Still under questions

Design of a demonstration Gigabit ethernet switch board for ATCA carrier board Design of the Gb ethernet switch board. Schematic diagram, PCB design and gerber files will be delivered	Dariusz Makowski (50%), Piotr Krasiński (50%)