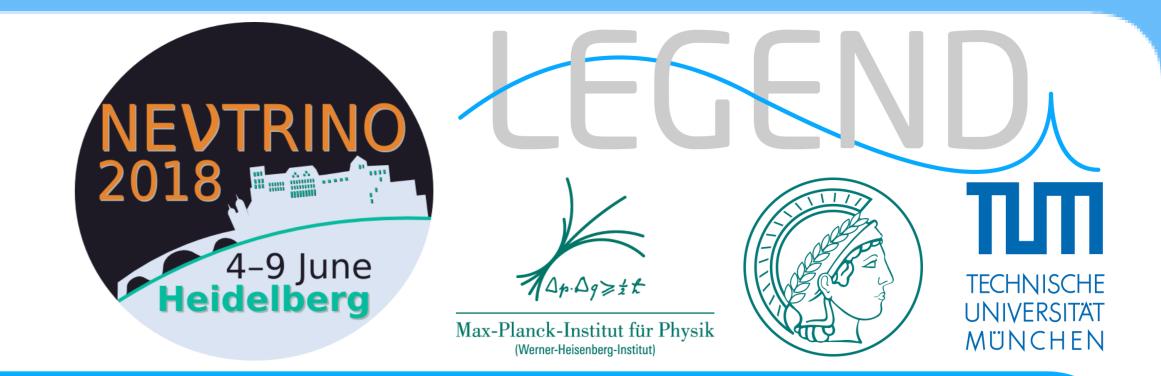
Development of Highly Integrated Low-mass Signal Readout Electronics for the LEGEND Experiment

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Large Enriched Germanium Experiment for Neutrinoless $\beta\beta$ Decay (LEGEND)

Mission

The collaboration aims to develop a phased, ⁷⁶Ge based double-beta decay experimental program with **discovery potential** at a half-life beyond 10²⁸ years, using existing resources as appropriate to expedite physics results.

Staged approach

First phase:

- Up to 200kg of Ge
- Modification of existing GERDA infrastructure at



Subsequent phases: 1000kg of Ge (staged) BG goal: 30x lower, 0.1 cts/(FWHM-t-yr)

Univ. of New Mexico L'Aquila Univ. and INFN Gran Sasso Science Inst. Lab. Naz. del Gran Sasso Univ. of Texas Tsinghua Univ. Univ. of Cal. Berkeley and LBNL Leibniz Inst. for Crystal Growth Comenius Univ. Lab. Naz. del Sud Univ. of North Carolina Sichuan Univ. Univ. of South Carolina Jagiellonian Univ. Banaras Hindu Univ. Tech. Univ. Dortmund Tech. Univ. Dresden



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- LNGS
- BG goal: 5x lower, 0.6 cts/(FWHM-t-yr)
- Sensitivity > 10^{27} yr
- Start by 2021

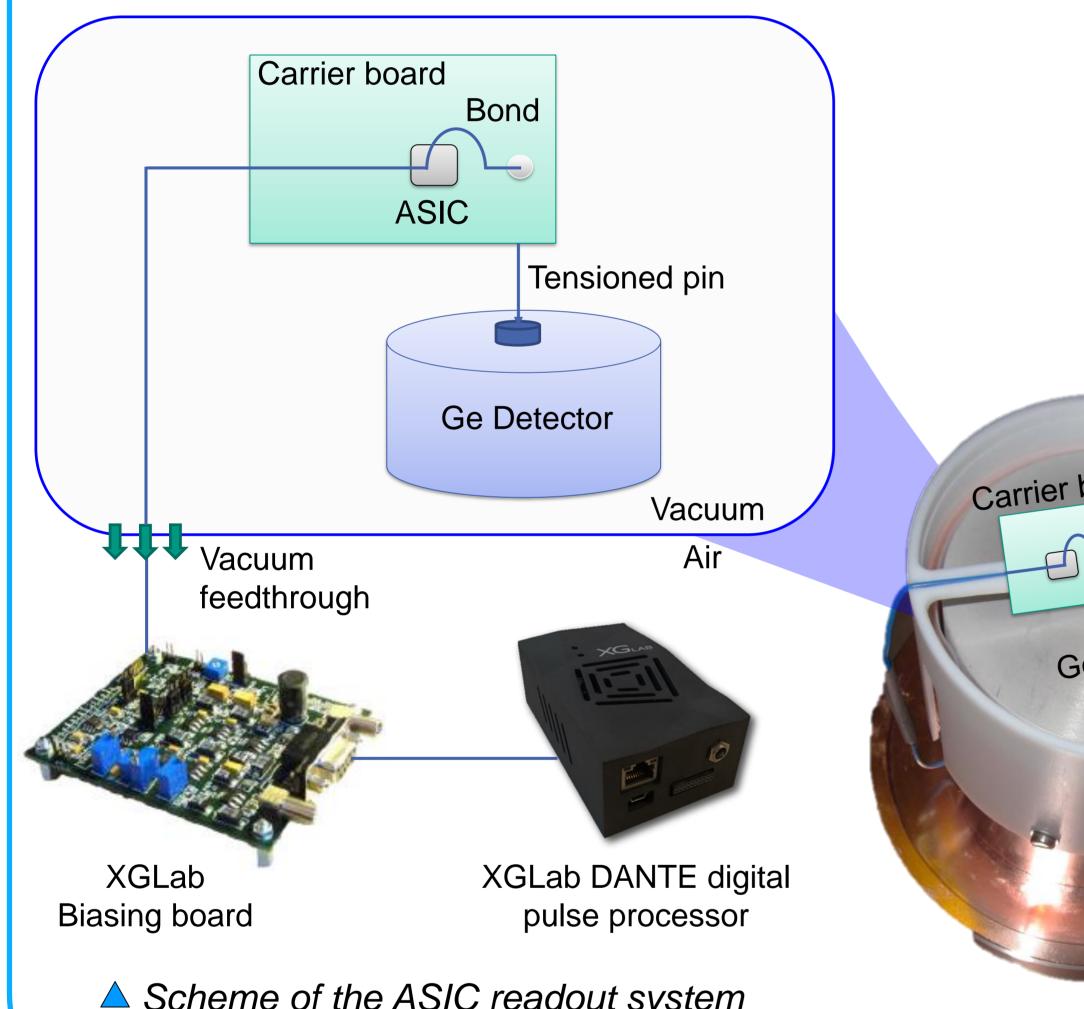


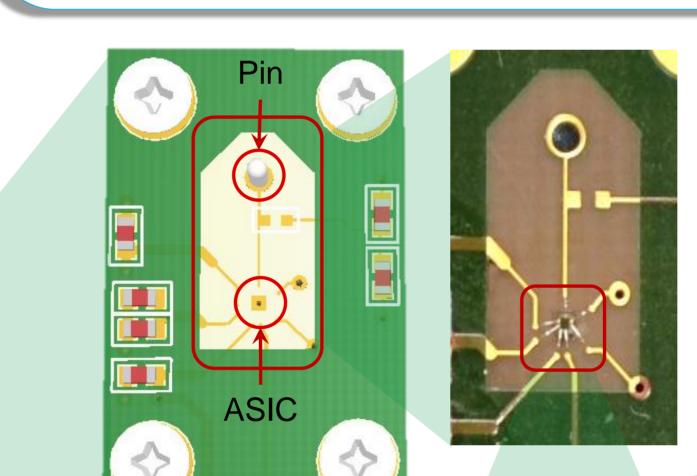
Sensitivity > 10^{28} yr Location: TBD • Required depth under investigation

Signal readout electronics for Germanium detectors

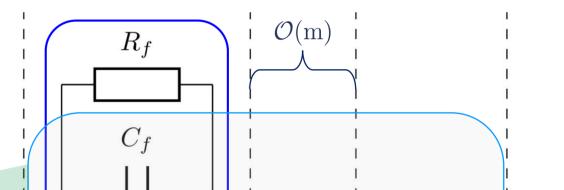
Readout electronics in the context of $0\nu\beta\beta$ decay

- For a good energy resolution and low electronic noise
- \rightarrow Place readout electronics as close as possible to detector
- Readout components contribute dominantly to background budget
- \rightarrow Front end mass should be as low as possible
- \rightarrow Use <u>application specific integrated circuit</u> (ASIC) technology





▼ Scheme of the discrete signal readout electronics used in MJD. One possible solution for the readout electronics in the LEGEND experiment is to combine the components in a single chip (ASIC).



Cables Preamplifier

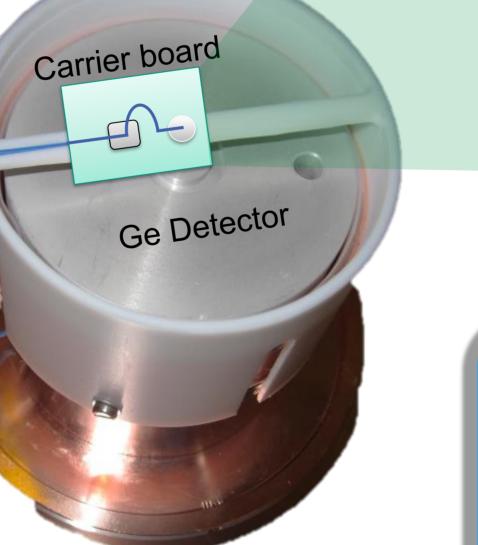
Signal

JFET

Front end

Current readout solutions for Ge-based $0\nu\beta\beta$ decay experiments

- GERDA and MAJORANA DEMONSTRATOR (MJD) use discrete readout electronics consisting of several passive components (Field effect transistor (JFET), RC-circuit, Preamplifier)
- Many single components \rightarrow contribute dominantly to background budget



Scheme of the ASIC readout system

Electronic design of the carrier board

ASIC readout technology

ASIC technology enables the development of a highly integrated signal readout solution

Detector

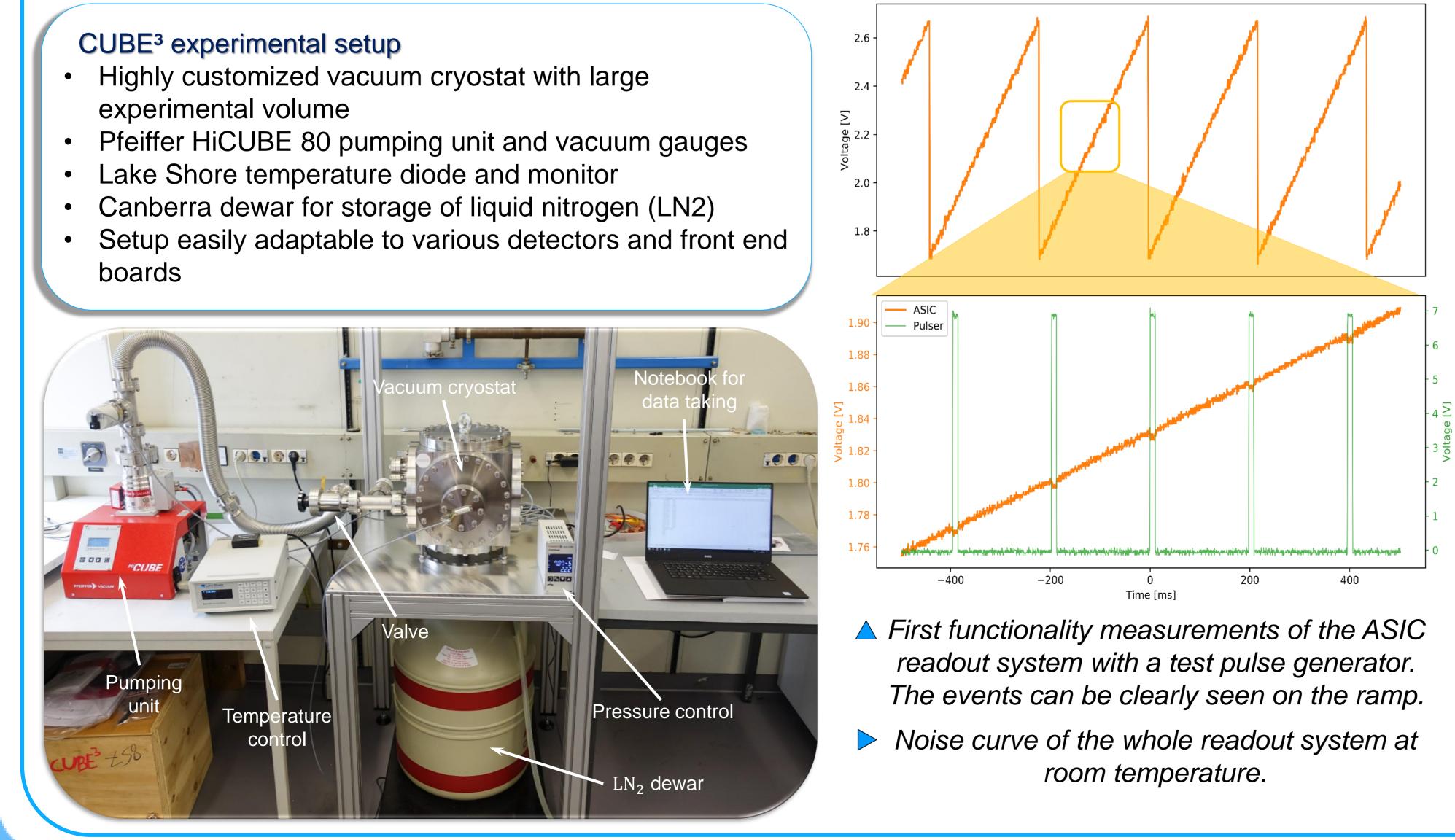
 C_D

- Charge sensitive amplifier, pre-amplifier and passive components combined in a **miniaturized single low-mass chip**
- CUBE ASIC provided by XGLab S.R.L. (Italy)

CUBE³ test stand at Technical University of Munich

Frank Edzards

- Setup easily adaptable to various detectors and front end



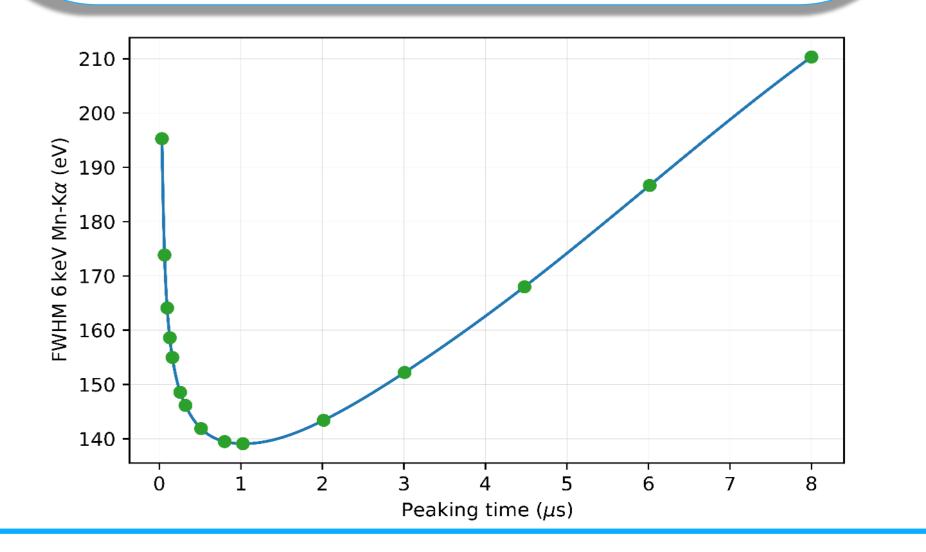
Research objectives

- Test and characterization of the performance of the novel ASIC readout system with a <u>p</u>-type point contact (PPC) Ge detector
- Specific **research questions** to be investigated:
- What is the performance of the ASIC readout system?
 - (i.e. electronic noise, energy linearity, dynamic range)
- What is the pulse shape discrimination

performance?

(i.e. discrimination between single [=signal] and multi [=background] site events)

Can the ASIC readout system be operated in liquid argon (LAr) and what is its performance in it?



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