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Integrated phase locked loop design

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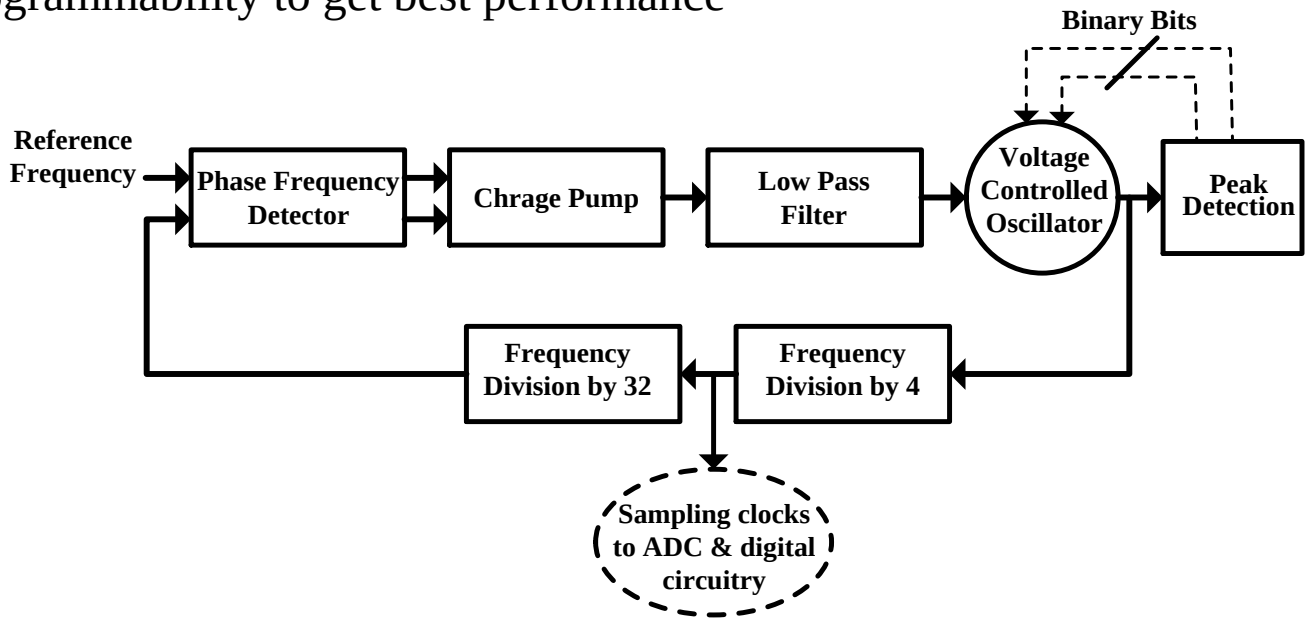
Phase locked loop (PLL)

- Generating sampling clocks for ADC and digital circuitry
- High frequency clock synchronizes with a low frequency reference clock
- Programmability to get best performance



Phase locked loop

Design specifications

The parameters of every block is determined to fulfill the requirements of the design:

- Loop bandwidth: The optimum quantity is selected to guarantee stability and low noise operation
- Phase noise: Noise requirements are considered to prevent signal to noise degradation in ADC
- Increasing reliability: Due to the long term performance of the design
- Power consumption
- Area

Chip fabrication in 65nm CMOS

- The default values for the design parameters include:

Reference frequency: 31.25MHz

Oscillator frequency: 4GHz

Sampling clock frequency: 1GHz

Divison ratio: 128

- Programmable options provide the following ranges:

15.625 MHz ≤ reference frequency ≤ 62.5MHz

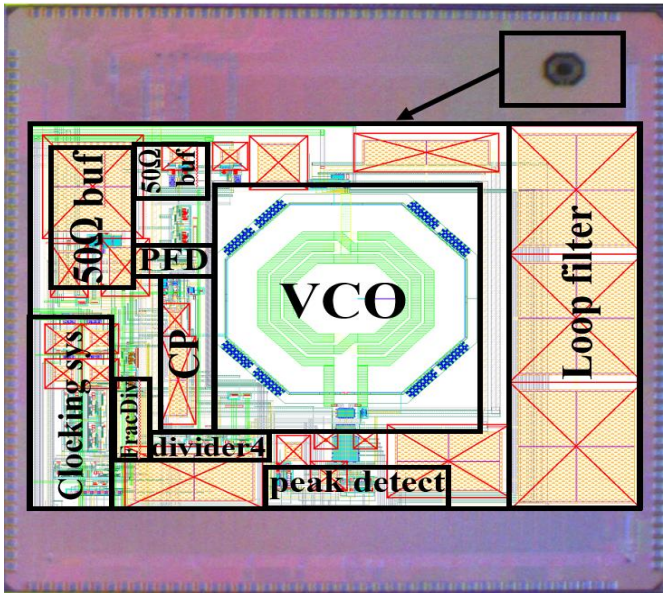
128 ≤ division ratio ≤ 1008

62.5MHz ≤ sampling clocks ≤ 1GHz

3.6GHz ≤ VCO frequency range ≤ 4.28GHz

- Power consumption: 30mW

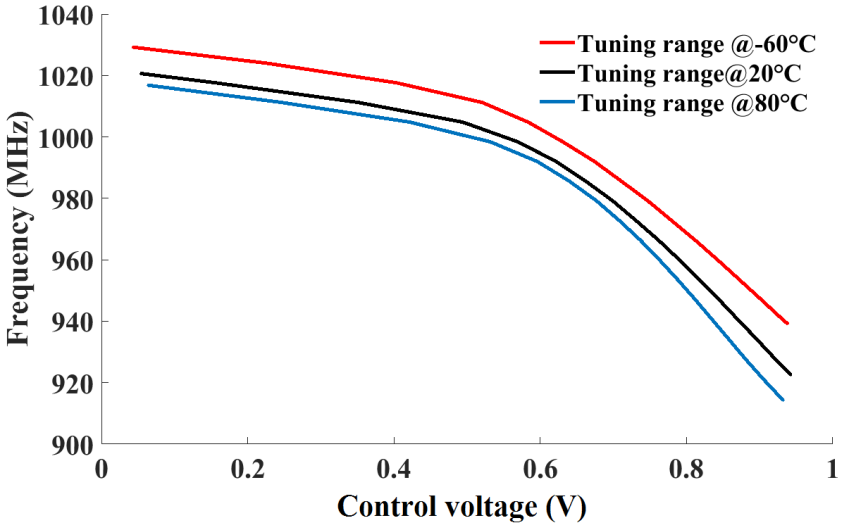
Area: 0.72μm×0.5μm



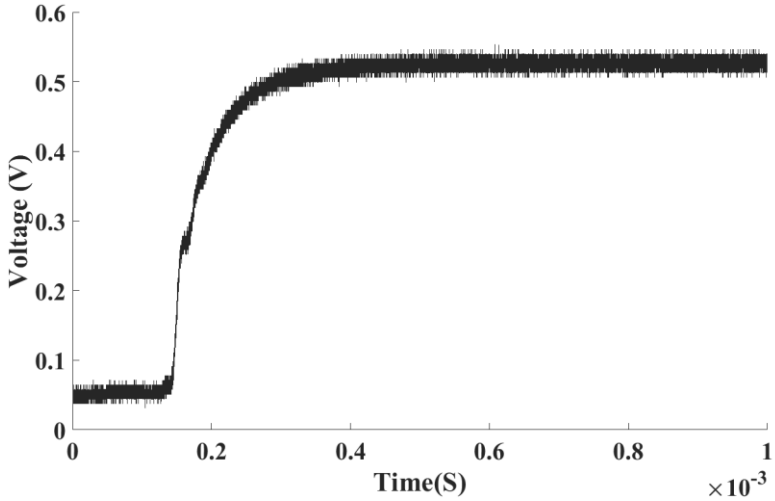
Chip micrograph and PLL layout

Measurement results

- The results of tuning range of oscillator is compatible with the expectations from simulations
- Measurements approve the functionality to generate a VCO frequency of 4GHz for sufficient temperature range



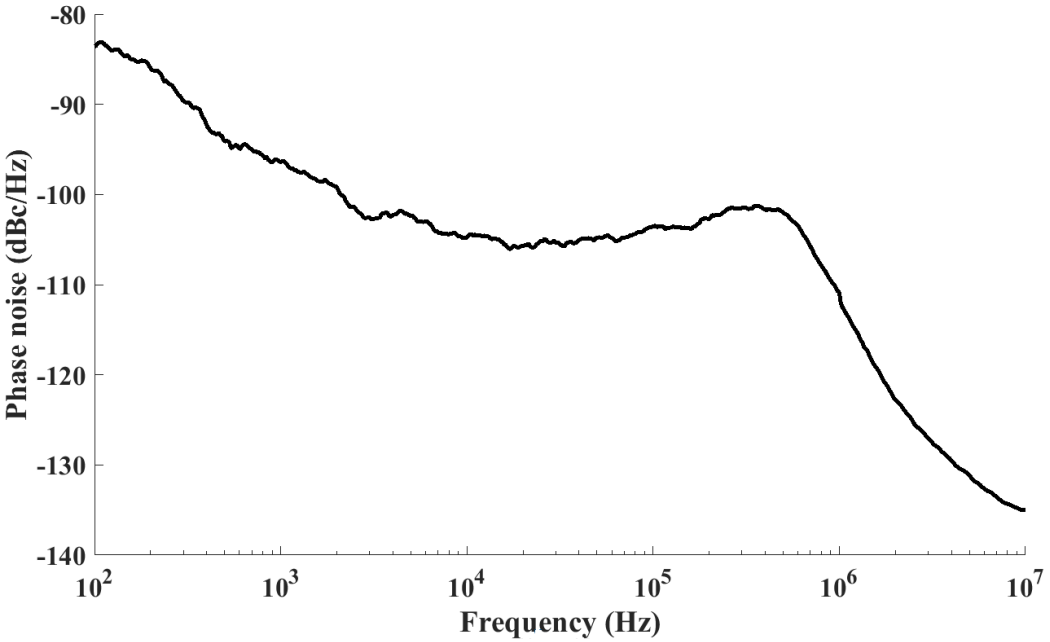
Tuning range of oscillator



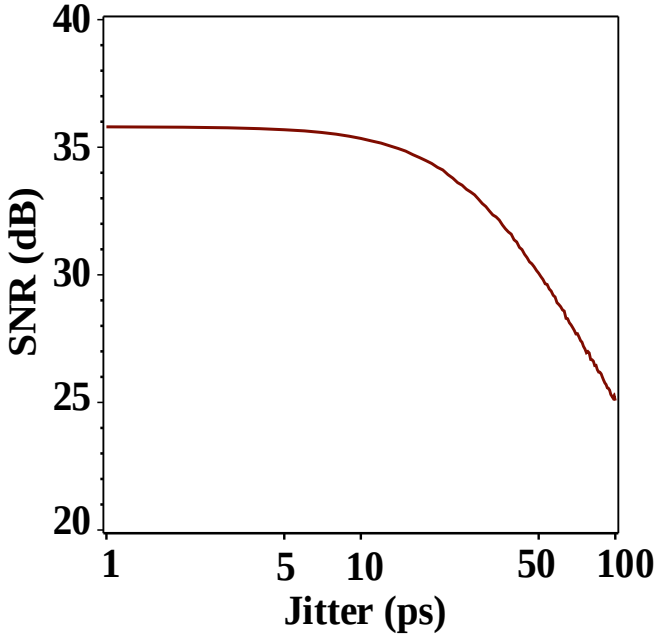
Locking process of PLL

Phase noise

- The maximum tolerable jitter for the ADC to prevent SNR degradation is 10 ps_{rms}
- The measurements show 1.4 ps_{rms} jitter for the PLL



PLL phase noise



Effect of clock jitter on signal to noise ratio (SNR) in ADC

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