JÜLICH
FORSCHUNGSZENTRUM

The Vulcan Chip

Analog

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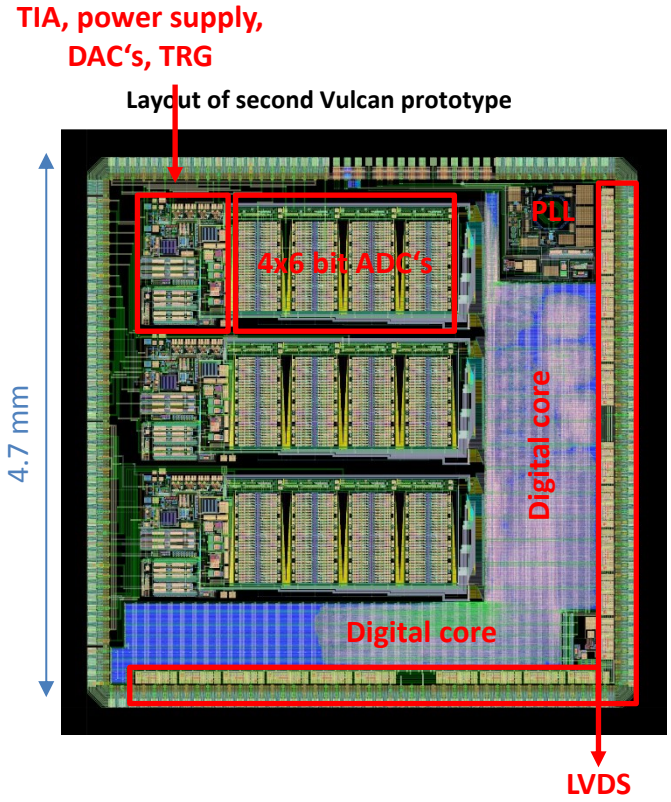
18 September 2017

VULCAN: basics and introduction

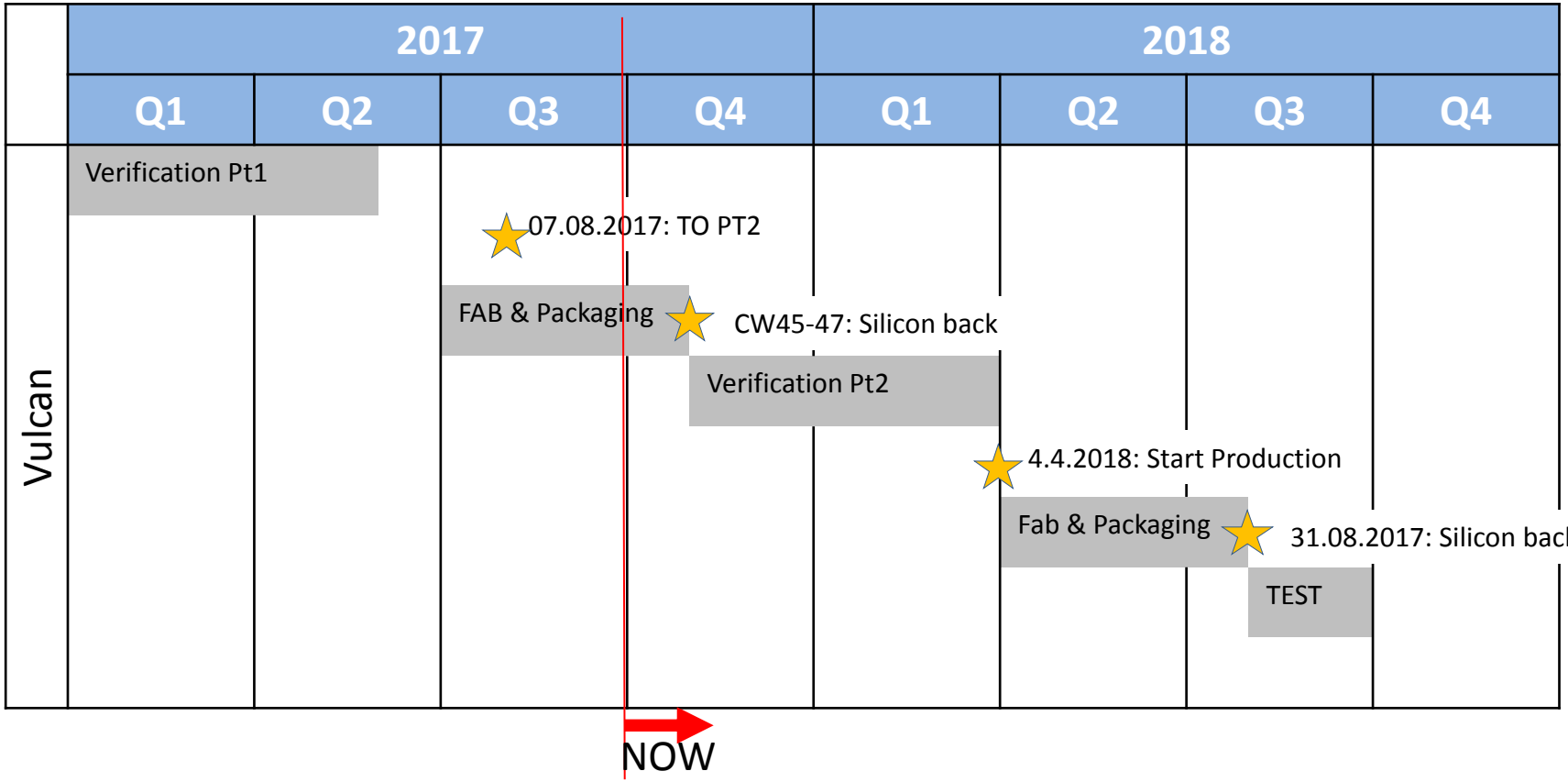
- 3 identical input channels sensing different signal ranges, all independently adjustable
- 1 amplification stage (TIA), power supplies, DAC's and 4 6-bit ADC's (8-bit if combined) per channel
- All clock signals provided by on chip PLL
- Smart data selection by digital core, buffers available for short term storage
- Data output by 16 LVDS pairs
- 4.7mmx4.7mm (ca 22mm²) with TSMC65 GP, QFN88 double row package



VULCAN: Overview of current status

- 1 test chip (all units as stand-alone blocks) and 2 prototypes (full signal chain) successfully tapeouted
- Test chip and 1st prototype measured, verified. Christian Roth will present.
- 1st prototype served as platform for debugging errors, all mended before 2nd prototype
- 2nd prototype is production ready version, will arrive at CW 45-47
- Verification plan being assembled now
- Production run (dedicated mask set) due in 2018

Vulcan Schedule



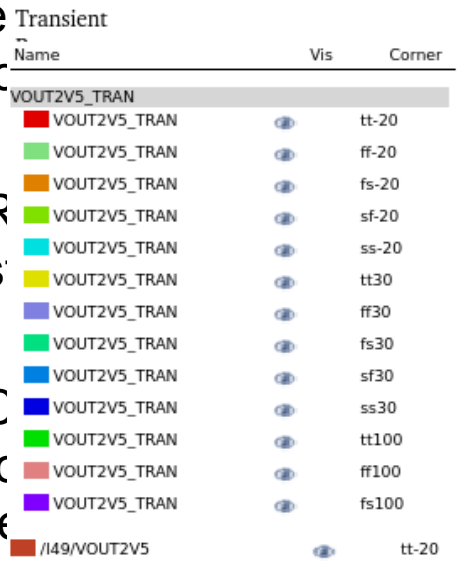
VULCAN: 1st → 2nd prototype

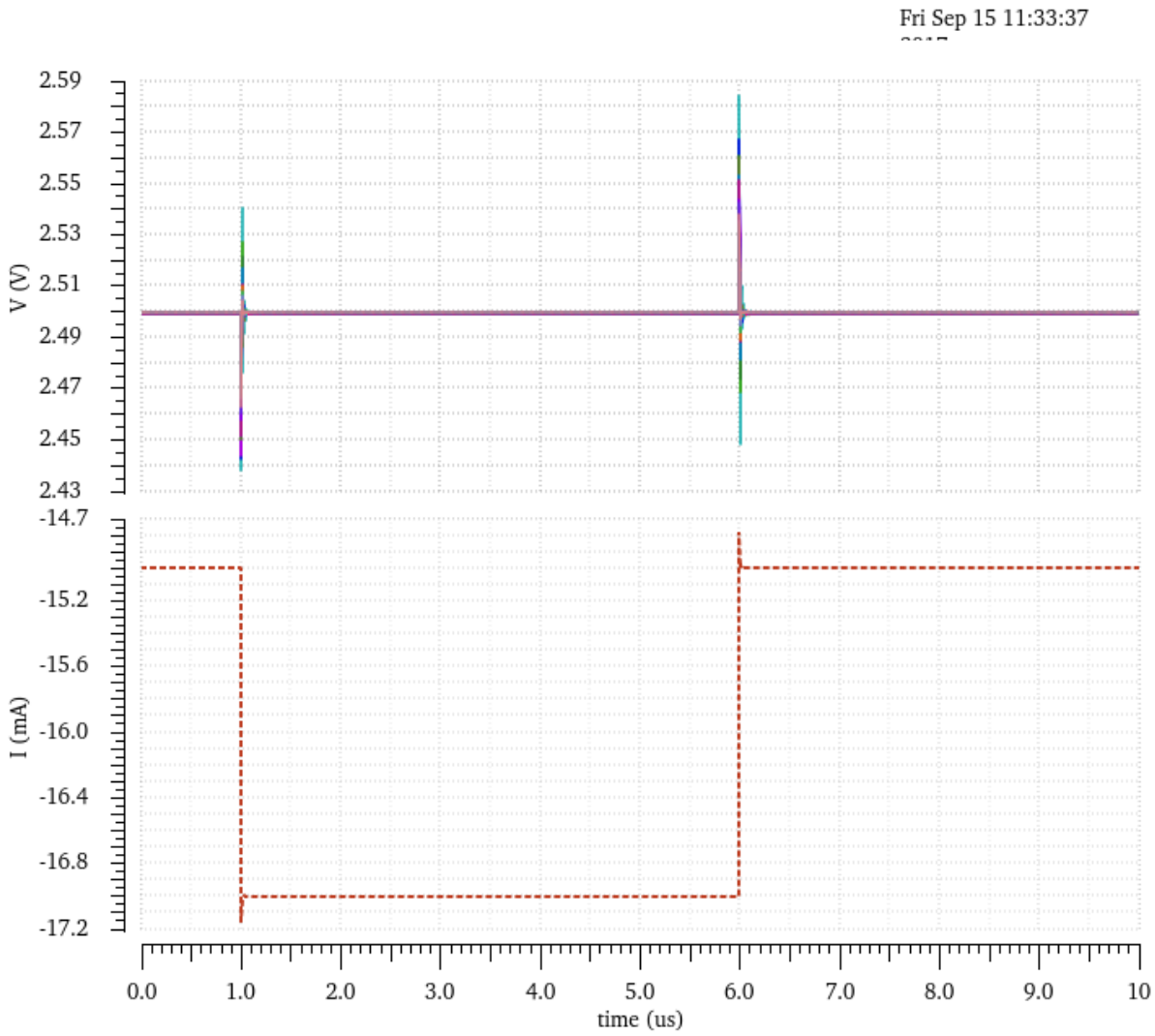
- All functional blocks already included on 1st prototype
- Minor bugs preventing plug&play operation, solved by FIB
- Improvements implemented on 2nd prototype
  - Digital
    - Timing of clocktree (for both digital circuits and ADC) and LVDS improved significantly
    - Scanchain test implemented
    - Power routing improved significantly
  - Power
    - Capless LDO‘s improved to serve different current consumption windows
    - Improved power supply for TIA to match for low input impedance over bandwidth
    - Optional 1-supply voltage only operation implemented
  - TIA
    - Improved measurability and power supply strategy for biasing
  - PLL
    - Improved linearity of amplitude
    - Output buffer made bypassable

Featuring: Power management

- Capless regulators to reduce risk of
  e
  lc
- R
  s
- C
  tc
  re
- D
  p
- T
  d
- E

VDD_ext (3.3V or 1.8V)

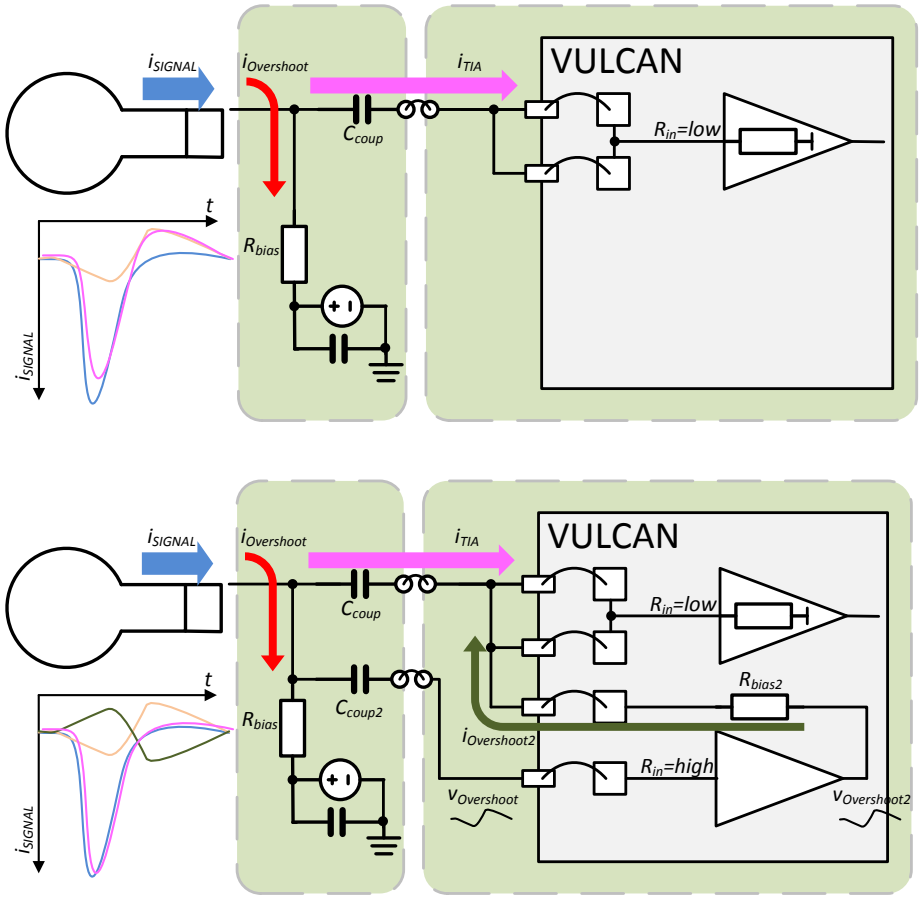




ode

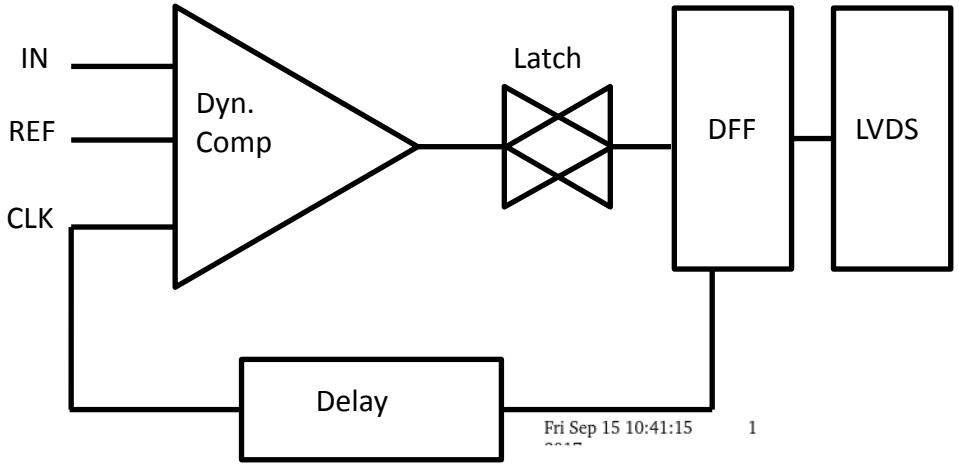
Featuring: Overshoot

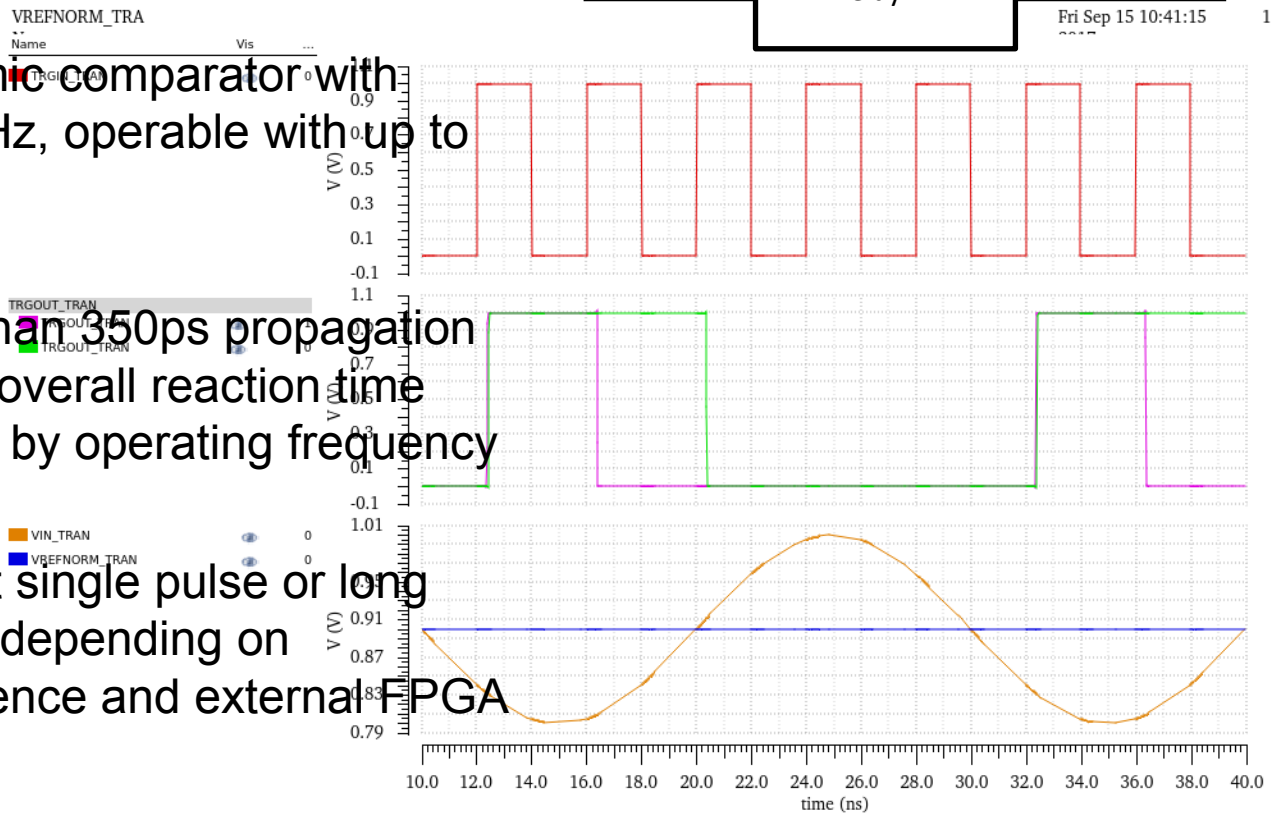
- Implemented to compensate the overshoot effect at the TIA input
- Excess current generated by input bias resistor generated by OSC instead of TIA
- For low gain channel, OSC performs as ADC input stage
- Versatile switching structure allows OSCOUT to perform as test input for ADC

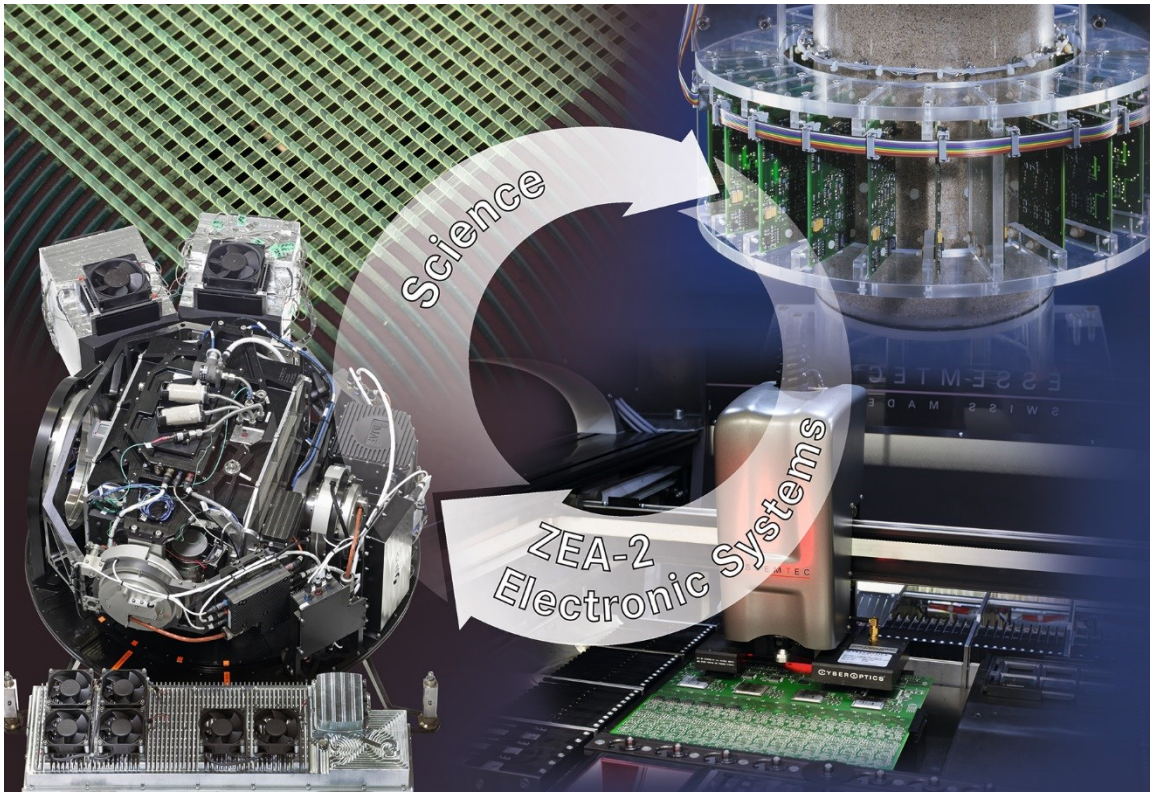


Featuring: Analog Trigger

- Independent trigger structure signalling events
- Dedicated LVDS output to bypass ADC and digital core
- Dynamic comparator with 250MHz, operable with up to 1GHz
- Less than 350ps propagation delay, overall reaction time limited by operating frequency
- Output single pulse or long pulse, depending on preference and external FPGA



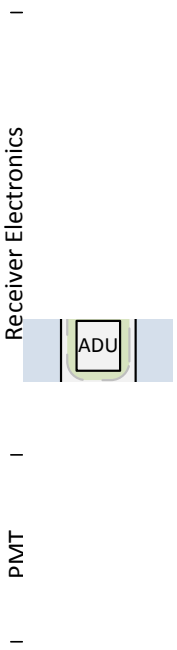




Thank you very much for your attention!

Backup slides

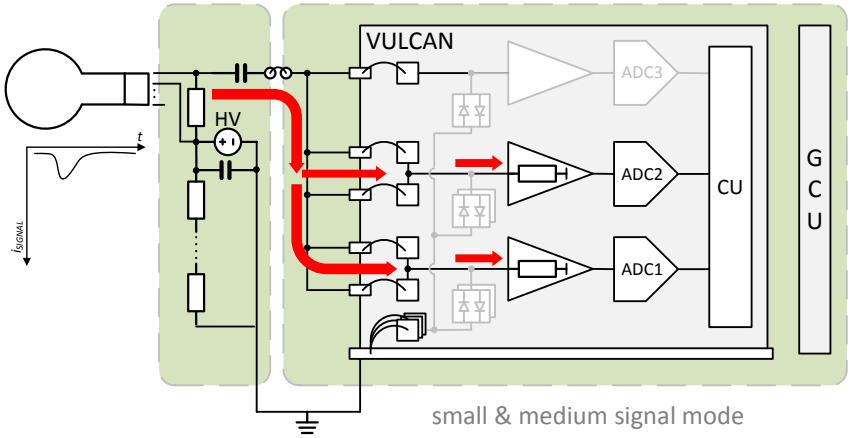
VULCAN: Overview of current status



- Highly linear, fully integrated circuit – **Vulcan**
  - Sampling ADC with approx. 80 dB linearity
    (3 signal chains with 3 different gains)
  - No external components required
  - On-chip clock generation from ref. clock
- Precise signal reconstruction
  - No analog delay line
    (reducing noise & distortion)
  - Control loop to suppress DC variations
  - Optional overshoot compensation
- Further key parameters of Vulcan:
  - ADC with 9.5 bit (3x 8 bit), 1 Gsample/s
  - Input impedance of < 10 Ohm
  - Power consumption ~ 1.2 Watt

Key Parameter of Vulcan	
Process	65 nm CMOS
Active Area	22 mm^2
Power	~ 1.2 W
Input Impedance	< 10 Ohm
Input Bandwidth	500 MHz
Sampling Rate	1 Gsample/s
Dynamic Range	80 dB
ADC Resolution	3x 8 bit
High Gain	0.06 p.e./bit
Medium Gain	0.4 p.e./bit
Low Gain	8 p.e./bit

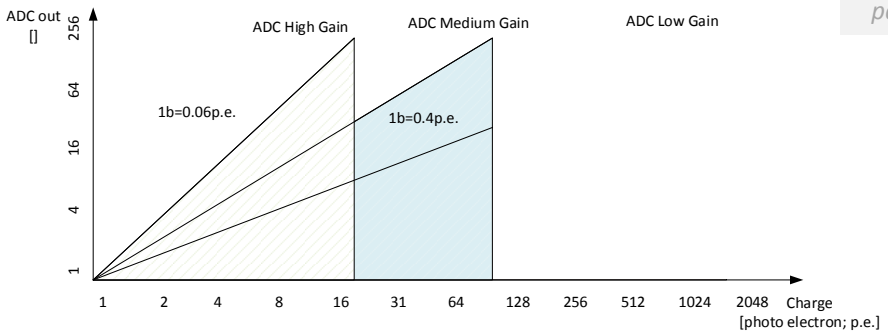
Signal Modes – Small & Medium Signals



small & medium signal mode

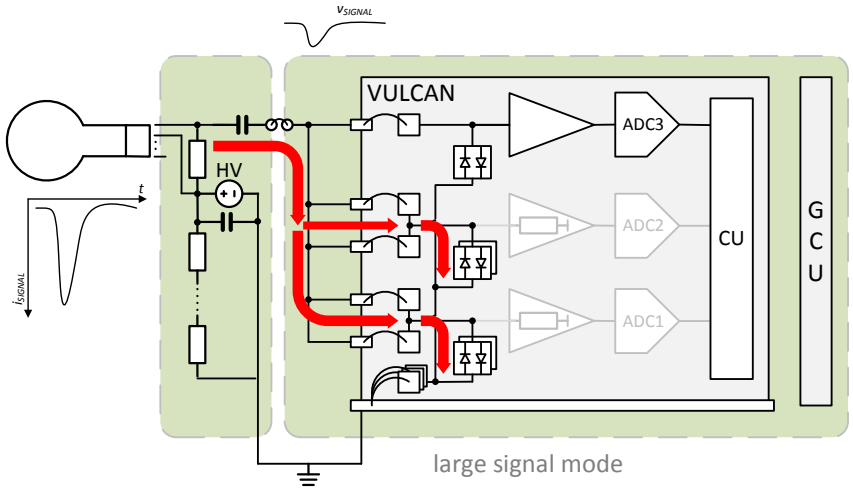
First two signal chains

- Parallel TIA input
- Programmable gains
- Combined input resistance $R \approx 5\ \Omega$



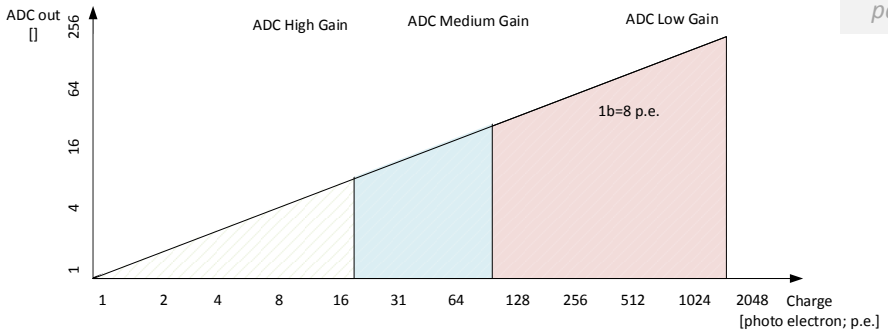
patent pending

Signal Modes – Large Signals



Third signal chain

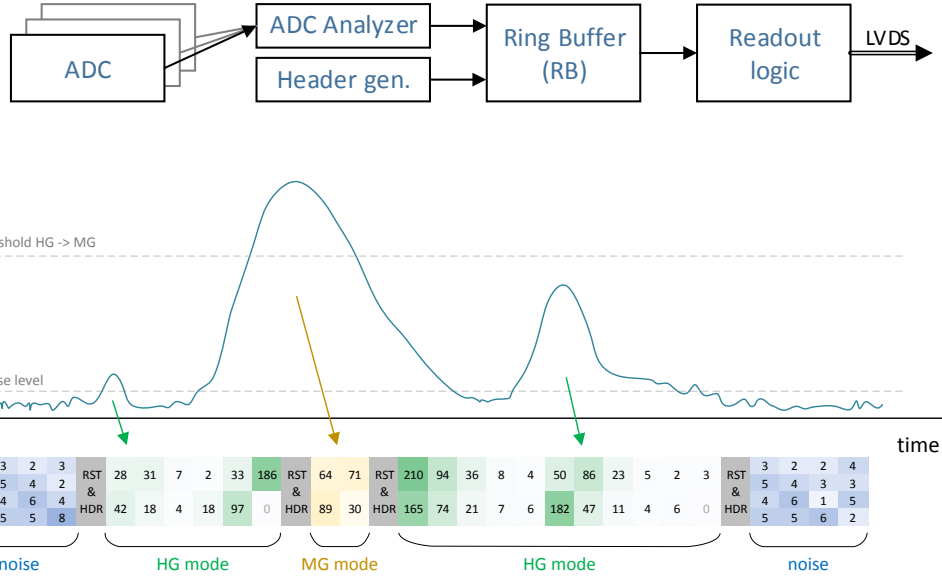
- Current > 20 mA
- TIA input saturates, ESD diodes open
- Voltage over diodes measured
- Combined input resistance $R \approx 5\ \Omega$

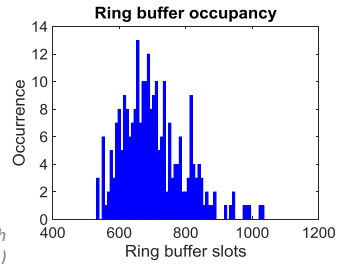


patent pending

Data Processing System

- Major tasks of digital processor:
  - Data selection
    (3 ADC → 1 sample)
  - Meta data generation
    (ADC source, system events)
  - Data buffering
    (Deal with meta data overhead)
- Data suppression for noise
  - Determined by threshold
  - Cut off 4 MSBs
- Buffer size based on supernova simulation



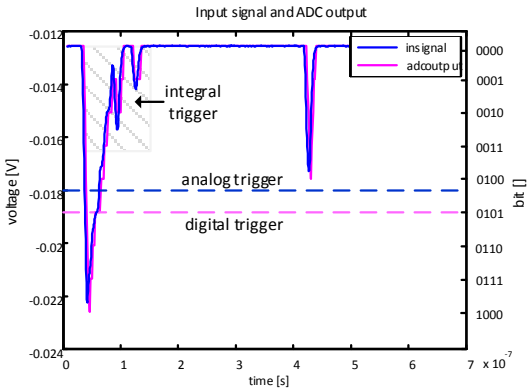


*Simulation in cooperation with **F. Lenz** (RWTH Aachen)*

Additional Digital Features

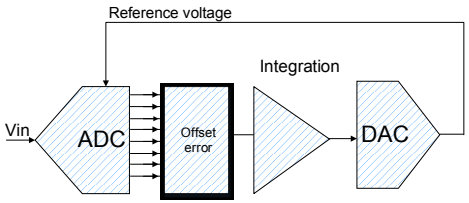
Dedicated Trigger Lines

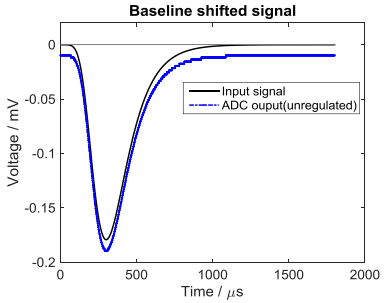
- Fast response on signals
  - One LVDS line per ADC
- Source selectable during runtime
  - Analog or digital threshold trigger
  - Two integral triggers

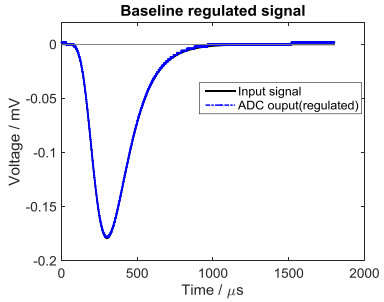


Baseline Regulation

- Feedback loop to correct baseline
  - Regulation only in noise mode
- Configurable during runtime
  - Enable
  - Threshold
  - Speed

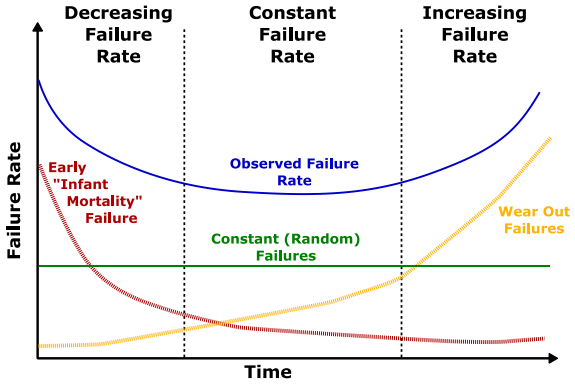






Reliability Measures

- Generally: Product failures in different phases:
  - Infant mortality due to manufacturing defects
  - Normal life & ware-out due to electromigration
    - Electromigration covered by design & simulation
- Manufacturing defects due to process variations
  - Varying between wafers and with position on wafer
  - Goal: Filter out all unreliable ICs, only stable survive
- Extensive verification plan for product tests
  - Structural scan test and IDDQ test for digital circuits
  - Stress test to verify electro migration
  - Functionality test and performance selection



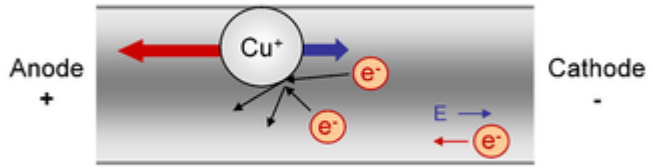
Bathtub curve, source: Wikipedia

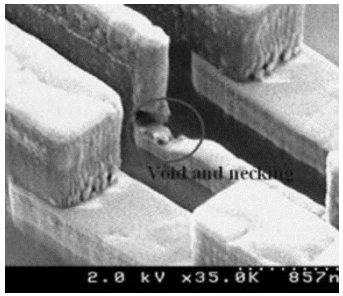
Strong Defects
- Not operational transistors/wires
- Immediate impact on functionality

Weak Defects
- Weakened wire, wears out over time
- Fails with stress on circuit

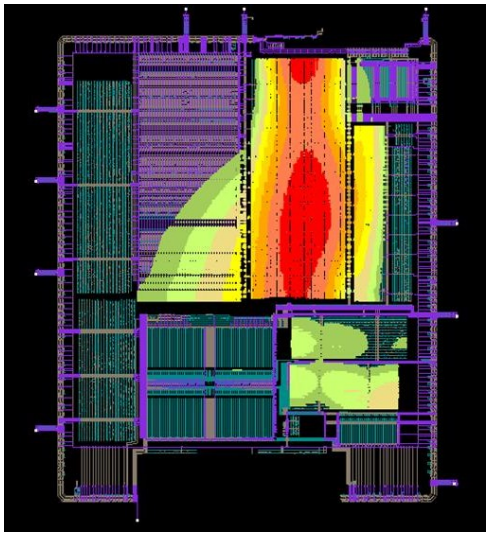
Electromigration-Aware Design

- Material transport by gradual movement due to electron collisions
  - Dependent on current density in the conductor
  - Degradation of the metal over time
  - Leads to connection faults in the design
- Prevent by design methods
  - Use wider/multiple conducting wires
  - Use multiple vias instead of single vias
- Perform electromigration studies to estimate degradation prior tapeout
  - Based on IR drop simulation
  - Detailed power consumption analysis
  - Critical areas are easily visible





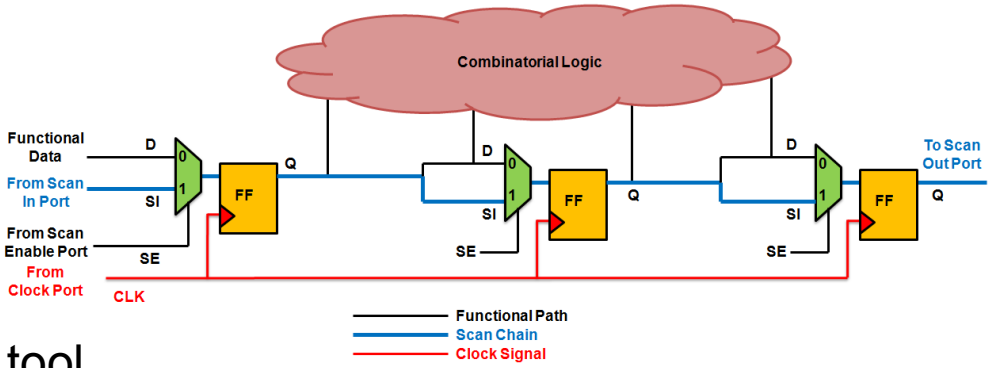
Electromigration effect



IR drop analysis

Structural Scan Tests

- Digital part composed of combinatorial and sequential logic
  - Goal: Test the functionality of digital gates
  - Method: Include a scan chain to determine faulty gates
- Flip flops (FFs) exchanged by scan FF
  - Two modes for operation: regular and scan
  - Scan data loaded through scan chain, representing logic state
  - Data is processed through combinatorial logic
  - Data shifted out to scan output
- Scan pattern generated by ATPG tool
- Detects single stuck-at-fault gates and delay faults



ATPG = automatic test pattern generator

Vulcan: 140,000 FFs

Vulcan Schedule