## Status of the ATCA Carrier Board V1 (unsolder V5, missing wires and pads under V5, the board in Lodz)

|                  | Subsystem / part                         |                  | Status             | Remarks  |
|------------------|--|------------------|--------------------|----------|
| Power regulators |  |                  |                    |          |
| regulators       | Main DC/DC converter                     |                  | OK                 |          |
|                  | V5                                       |                  | OK                 |          |
|                  | AMC bays                                 |                  | OK                 |          |
|                  | IPMC                                     |                  | OK                 |          |
|                  | DSP                                      |                  | OK                 |          |
|                  | Configuration                            |                  | OK                 |          |
|                  | Clk & Trg                                |                  | OK                 |          |
|                  | PCIExpress                               |                  | OK                 |          |
| Functionality    |  |                  |                    |          |
|                  | JTAG to FPGA IPMC                        |                  | OK                 |          |
|                  | JTAG Switch                              |                  | OK                 |          |
|                  | JTAG V5                                  |                  | OK                 |          |
|                  | Microcontroller IPMC                     |                  | OK                 |          |
|                  | FPGA Configuration (connection to target |                  | OK                 |          |
|                  | devices)                                 |                  |                    |          |
|                  | FPGA IPMC                                |                  | OK                 |          |
|                  | PCIExpress Switch                        |                  | OK                 |          |
|                  | Cross-switches                           |                  | Not tested         |          |
|                  | Gigabit Ethernet PHY                     |                  | Impossible to      |          |
|                  |  |                  | test               |          |
| Communication    |  |                  |                    |          |
|                  | JTAG to all components                   |                  |                    |          |
|                  | PCIExpress to                            |                  |                    |          |
|                  |  | Switch           | OK                 |          |
|                  |  | AMC bays         | OK                 |          |
|                  |  | V5               | Impossible to      | critical |
|                  |  |                  | test               |          |
|                  |  | Ext. connector   | OK                 |          |
|                  |  | Cross-switch     | Not tested         | critical |
|                  |  | Fabic interface  | Not tested         | critical |
|                  | Gigabit Ethernet from                    |                  |                    |          |
|                  |  | Base interface   | Impossible to test |          |
|                  |  | Ext. connector   | Impossible to test |          |
|                  | Low Latency Link to                      |                  |                    |          |
|                  |  | AMC bays         | Impossible to test | critical |
|                  |  | Fabric interface | Impossible to test | critical |

| Rocket IO to fabric interface | Impossible to | critical |
|-------------------------------|---------------|----------|
|                               | test          |          |
| V5 <-> DSP                    | Impossible to |          |
|                               | test          |          |
|                               |               |          |
|                               |               |          |
|                               |               |          |
|                               |               |          |
|                               |               |          |
|                               |               |          |
|                               |               |          |

Remarks:

 $\underline{Impossible\ to\ test}-due\ to\ unsoldered\ V5$