Status of the ATCA Carrier Board V1 (board with V5, the board at DESY)

Subsystem / part			Status	Remarks
Power regulators				
	Main DC/DC converter		OK	
	V5		Not tested (26.02) [TJ]	critical
	AMC bays		OK	
	IPMC		OK	
	DSP		OK	
	Configuration		OK	
	Clk & Trg		OK	critical
	PCIExpress		Not tested (10.03) [DM]	critical
Functionality				
	JTAG to FPGA IPMC		OK	
	JTAG Switch		OK	
	JTAG V5		Not tested (26.02) [TJ]	Critical
	Microcontroller IPMC		OK	
	FPGA Configuration (connection to target devices)		OK	
	FPGA IPMC		OK	
	PCIExpress Switch		Not tested (10.03) [DM]	Critical**
	Cross-switches		Not tested (10.02) [DM]	Critical
	Gigabit Ethernet PHY		Not tested (15.03) [WJ]	
	Clk & trg		Not tested (component not arrived)	
Communication				
	JTAG to all components			
	PCIExpress to			
		Switch	Not tested (10.03) [DM]	Critical**
		AMC bays	Not tested (10.03) [DM]	critical**
		V5	Not tested (10.03) [DM]	Critical
		Ext. connector	Not tested (10.03) [DM]	critical**
		Cross-switch	Not tested (10.03) [DM]	Critical

		Fabic interface	Not tested (10.03) [DM]	critical
	Gigabit Ethernet from			
		Base interface	Not tested (15.03) [WJ]	
		Ext. connector	Not tested (15.03) [WJ]	
	Low Latency Link to			
		AMC bays	Not tested (15.03) [WJ]	critical
		Fabric interface	Not tested (15.03) [WJ]	critical
	Rocket IO to fabric interface		Not tested (15.03) [WJ]	critical
	V5 <-> DSP		Not tested	

Remarks:

**PCIExpress has been already tested on previous board, except communication to V5.

(26.02) – date when test should be done
[WJ] – Wojciech Jalmuzna, responsible for tesr
[DM] – Dariusz Makowski, responsible for tesr
[TJ] – Tomasz JezynskiWojciech Jalmuzna, responsible for tesr