AMC DESY Carrier Board (V1)

Technical Design Proposal

MSK Group

March 2008
Version 1.0 (Draft)

Please send comments to: Tomasz.Jezynski@desy.de
Deutches Elektronen-Synchrotron,
Notkestr. 85
22607 Hamburg
Germany

Revison History

Date	revison	Change	Signature
01.03.2007	0	Created	Tomasz Jezynski
01.02.2008	1.0	Change to 3 bay version (read version 0.1 for comparison)	

1. Introduction

The presented work in this document is a result of several discussions between collaboration members from DESY, Lodz Univ. and Warsaw Univ. devoted to conversion of the VME base LLRF system to the system base on the ATCA form factor. The project should be completed at the end of 2007.The carrier boar is one of the most important part of the system. Parallel to the carrier board following AMC modules are developed (described in separated papers):

- 8 x ADC, 14 bits, sampling rate up 105 MHz
- timing module
- digital up-converter (vector modulator - VM)
- conventional up-converter (vector modulator - VM)
- communication module (optical receiver)

The ATCA Carrier Board has to support a distributed and centralized version LLRF control system.

2. Description

The carrier board is a main processing unit for a low latency RF controller. Different AMC modules are plugged to the carrier at any AMC bay. All signals required by AMC modules are provided through the carrier board. These signals are available on AMC connector, and connected to the carrier through ZONE3 connector. Clock and trigger signals are generated on AMC module, plugged to any bay and can be distributed to others carrier boards. The carrier board can also receive clock and trigger signals through ZONE3 connector and distributed to all AMC bays on the carrier. Full remote control of the board (vi Shelf Manager) is possible. The carrier board should also operate in standalone mode.

3. Requirements

- The carrier board must:
  - be compatible with any standard, single width, single or half high, AMC.1 module
  - compliance with AdvancedTCA spec (interfaces to the fabric)
  - provide computing power for LLRF algorithms
  - support floating point operations
  - handle hot-swap for the carrier and AMC modules
  - work in the crate and standalone
  - distribute timing signals to AMC slots and other carrier boards
- no permanent front panel connection (diagnostic connectors allowed), and fiber optic connections
  - all characteristic signals for the LLRF must be provided to AMC bay
- AMC bays must
  - support hot-swap functionality for the AMC modules
  - provide clock and trigger signals
  - provide characteristic signals for the LLRF
  - support low latency link to processor unit on the board

4. Specification

- 3 x AMC-DESY bay
- IPMC 2.0 controller on the carrier, controlled by Shelf Manager or by Mainframe FPGA in case of standalone operation
- 1 x DSP TigerSHARC processor on board, connected via 4-bits link to main FPGA
- low latency link between main FPGA and any AMC bay – 10 differential lines between each AMC bay and main FPGA
- clock and trigger distribution system
- 14 lines (for analog signals), up to 1.3GHz, 0dBm
    - 10 x probe signal
    - 2 x RF reference signal
    - 2 x RF out
- 2 x differential line for coded clock signal - 2.6 GHz, 0dBm
- 3 x clock signal, differential LVDS, bus
- 3 x trigger signal, differential LVDS bus
- 10 x line for low latency protocol, up to 3.5Gbps
- PCIExpress communication on fabric interface
- Rocket IO communication on fabric interface
- Low Latency communication on fabric interface
- Gigabit Ethernet on base interface

RF data

Isolation:	RF and LO at IF < 50 dBm
Crosstalk:	better than -45 dB between any two RF channels

Environmental condition:

Operating temperature range:	-10 deg. C to +70 deg.C
Humidity:	max 95 % non condensing

4. Concept of the carrier board

4.1 Block diagram

A block diagram of the carrier board is shown in Figure 1. Main components are: FPFA (XILINX Virex5), DSP processor, power supplies, AMC connectors, PCIExpress switch, clock distribution, and IPMI controller. Specific signals for the LLRF are connected to AMC bays through ZONE3 connector (analog signals, clock signals).

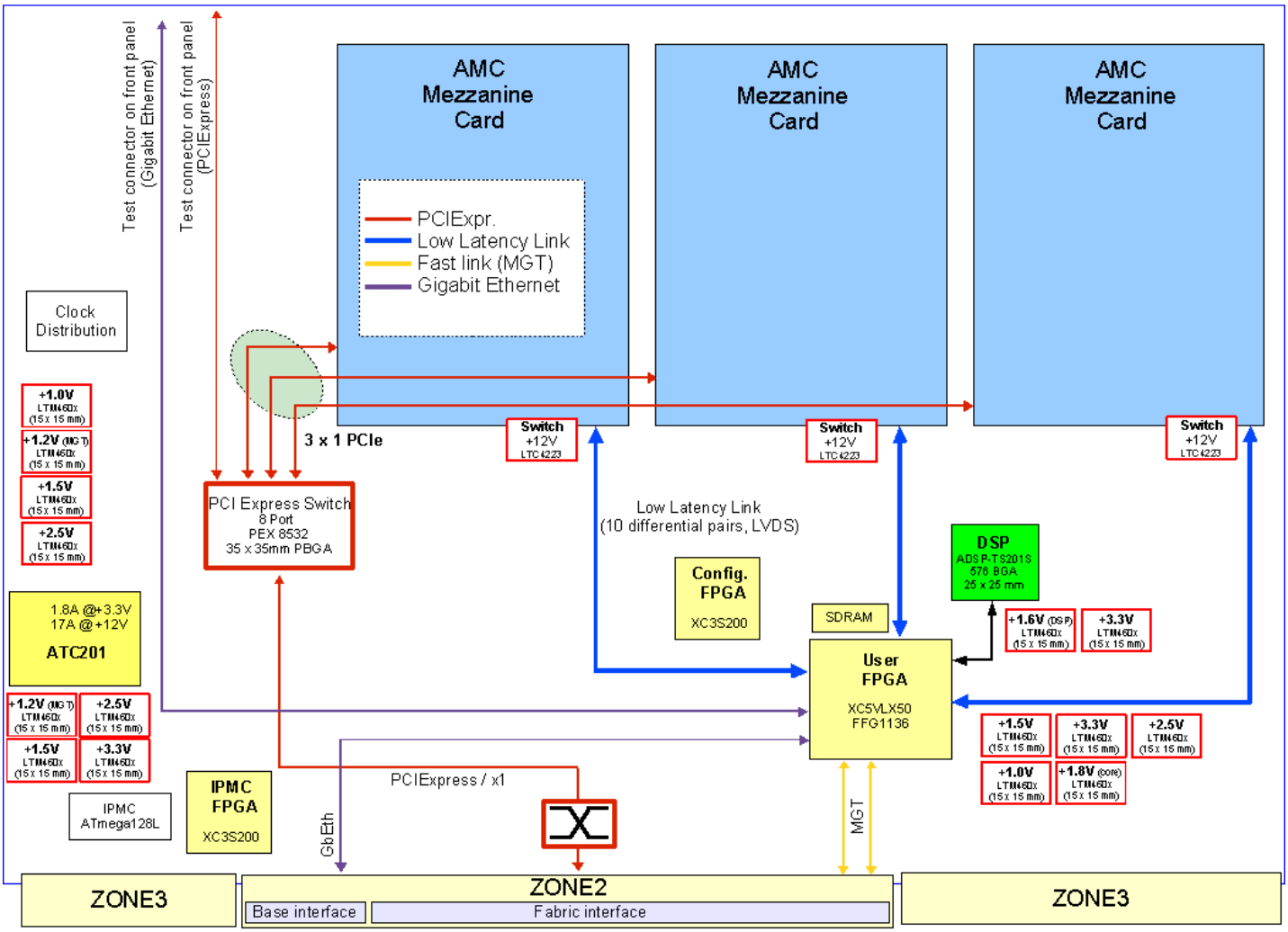


Fig. 1 Block diagram of the carrier board.

4.2 Computing power and communication links

The processor unit of the carrier board is build base on the Xilixn Virtex5 FPGA and Analog Devices DSP TigerSHARC TS201, floating point processor. The user FPGA and DSP are connected together by 4-bits DSP link (link is made according to AD specification).

Communication links

Following communication links must be implemented on the carrier:

- DSP link to main FPGA
- PCIExpress to:
  - fabric interface
  - main FPGA
  - AMC bays

- test front panel connector
- Gigabit Ethernet from base interface to:main FPFA
- Gigabit Ethernet from front panel to main FPGA (test)
- Rocket IOs (10) between main FPGA and fabric interface
- Low Latency Link (2 differential pairs) between fabric interface and main FPGA
- Low Latency Links (10 differential pairs) between each AMC bay and main FPGA
- RS232 from front panel connector to FPGA (test, service connector)

PCIExpress is connected to the fabric interface through 2 cross-switches. MGTs and LLL from main FPGA are directly connected to the fabric interface. Pin assignment for the fabric interface is shown in Fig 2.

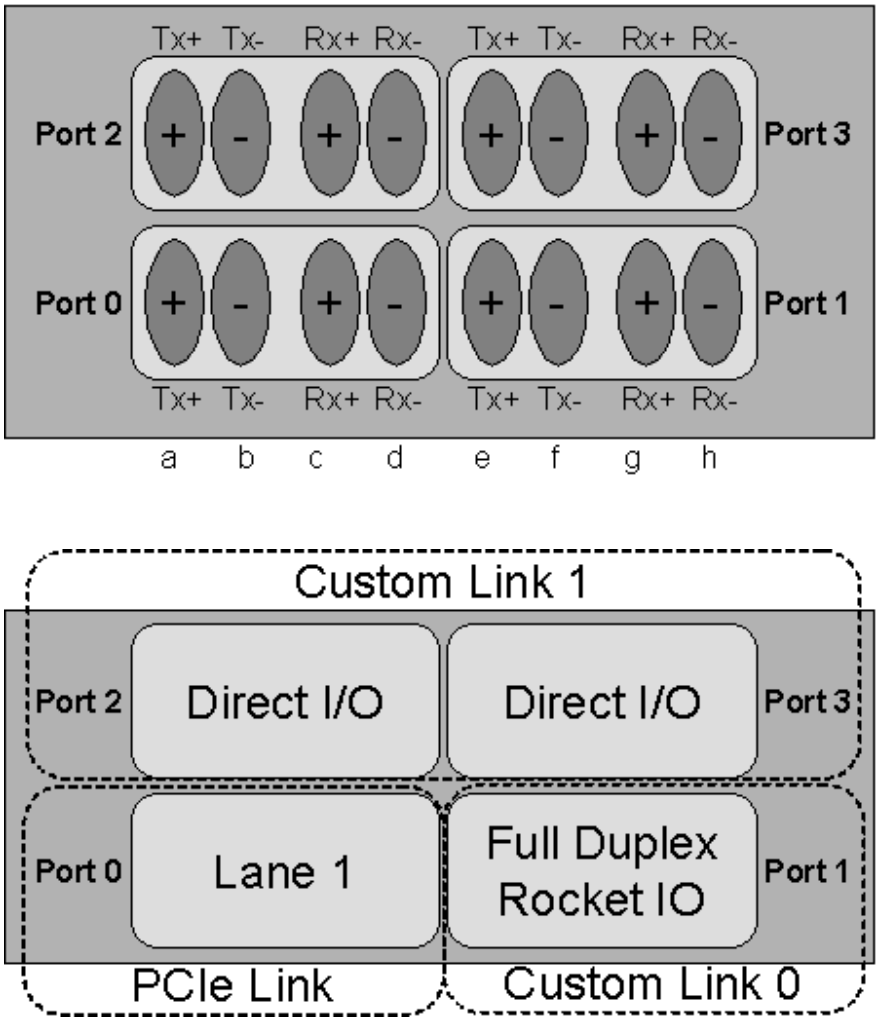


Fig. 2 Channel definition on the fabric interface. (W.Koprek)

PCIExpress

The user FPGA, AMC slots have connection between themselves, and the fabric interface through PCIExpress switch. Device which can handle this function is PEX8532 (8-port, 32-lane) from Vitesse.

RS232

Mini RS232 connector located on the front is connected to main FPGA. On the board there is level adapter for serial link. PC can be directly connected to the carrier board.

Giga Bit Ethernet

The main FPGA has to Gigabit Ethernet connection. One is provided directly from a base interface, second from front panel connector. There is no switch on the board.

4.3. JTAG, configuration and booting

The JTAG chain is shown in Figure 3. The JTAG switch is controlled from Shelf Manager, over IPMC controller

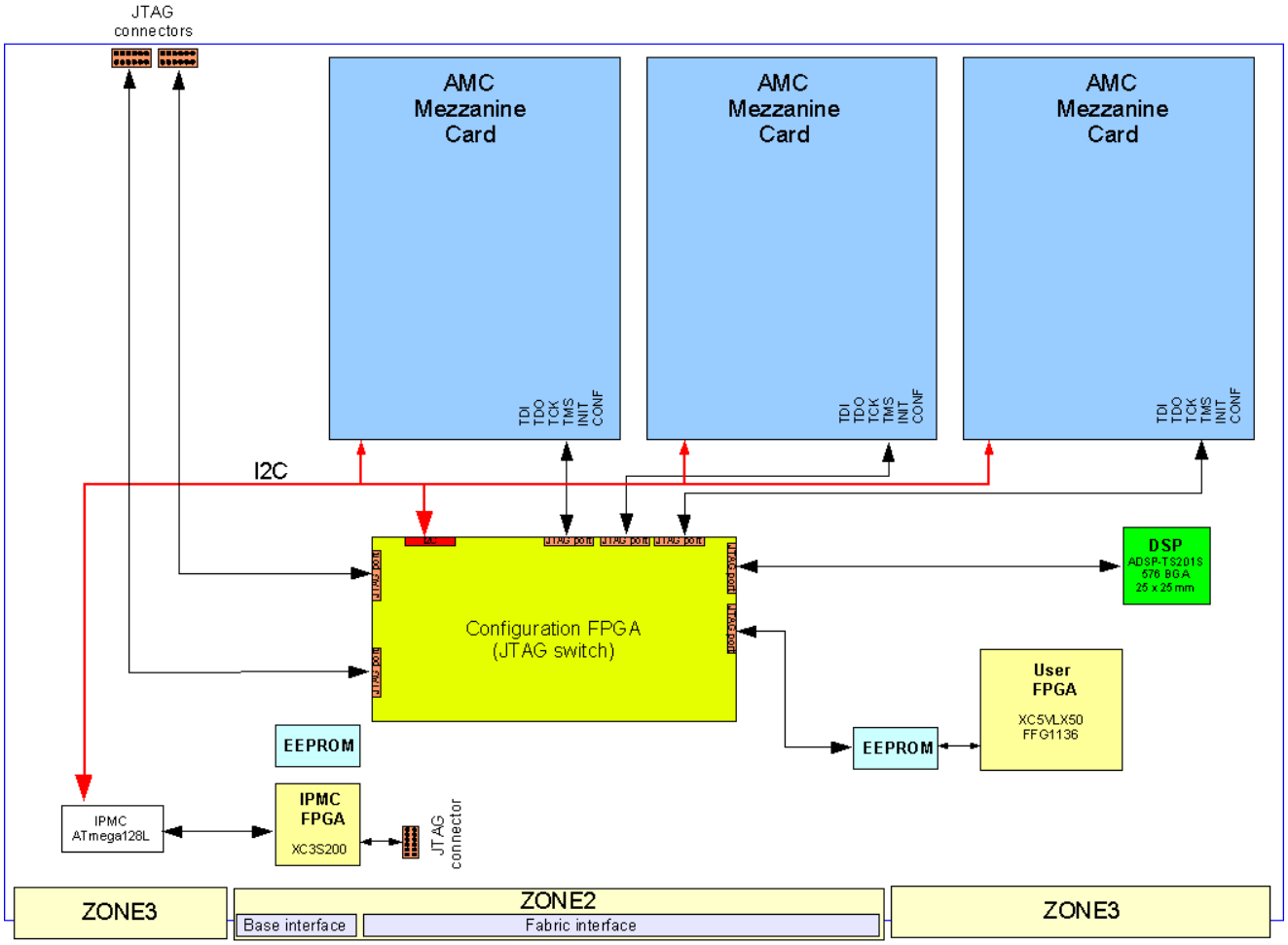


Fig. 3 JTAG configuration. (RS232 missing….)

4.4 Power regulators and IPMI

An IPMI controller is base on an ATMEL AVR microcontroller and compatible with IPMI v. 2.0 specification. The IPMI provides following interfaces to the carrier:

- SPI
- JTAG
- RS232

The IPMI control power supplies, monitor power consumption, configure FPGAs, DSPs, and AMC modules. It also provides remote reset, power enable signals to the power regulators. The carrier board can operate without the ShelfManager (standalone mode). The standalone mode is set by special configuration switch (S1). In this mode a firmware FPGA must be powered all the time. The firmware FPGA takes functions of the ShelfManager during standalone work. Control of the IPMI is done by Ethernet and firmware. Block diagram of the power regulators and IPMI is shown in Fig.5. Figure XX shows available power on the ZONE1 connector and signals for IPMI controller.

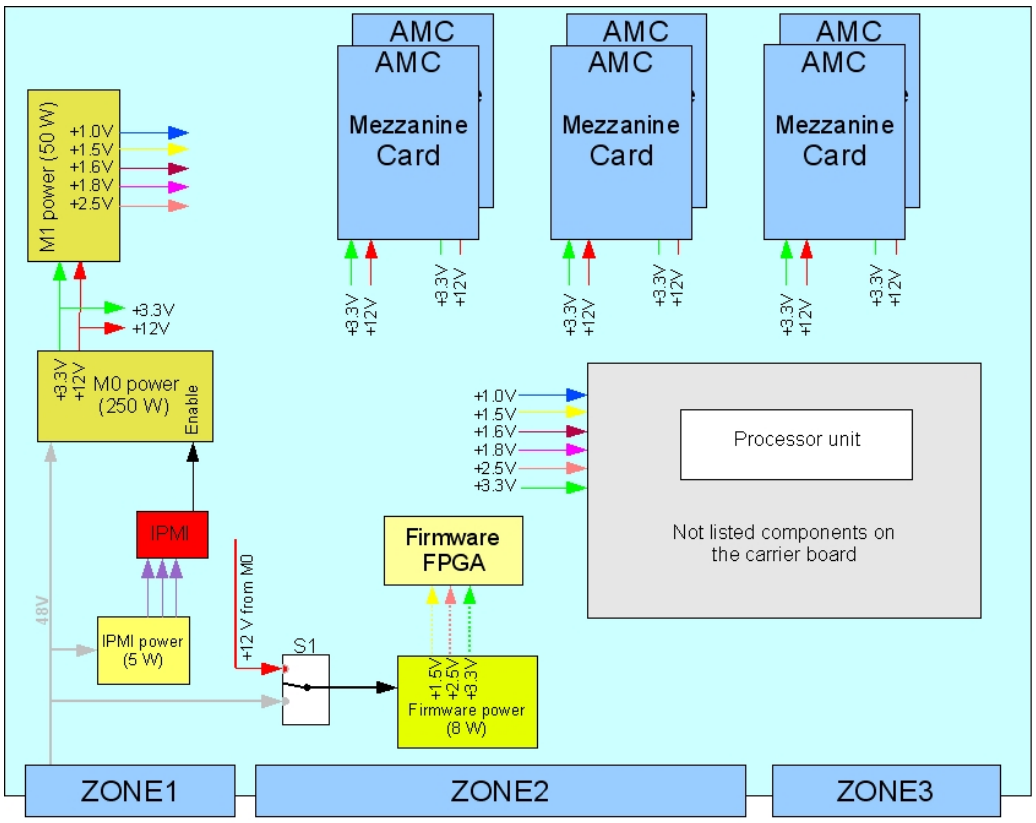


Fig. 5 Power regulators

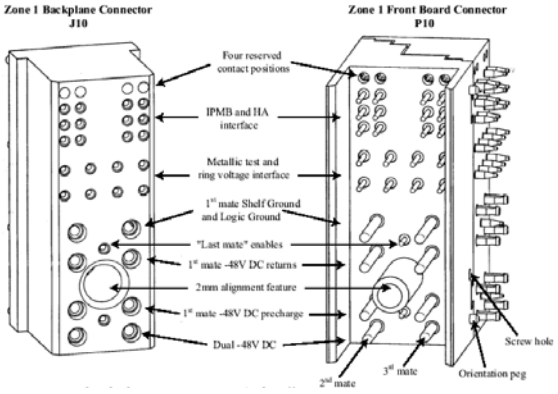


Fig. 6 ZONE1 connector.

Functions of the IPMI controller are following:

- Switch on/off the carrier
- Handle hot-swap
- Identify the carrier
- Read voltage, current, temperature
- SEU errors
- Status of switch
- Remote reset
- configure EEPROMs
- boot FPGAs, DSP (JTAG)
- access to registers
- Readout logfiles
- provide interfaces to the carrier & AMC modules
    - JTAG
    - I2C
    - SPI
    - RS232

Block diagram modules connected to IPMI is shown in Figure xx.

Fig. xx IPMI

4.5 Firmware FPGA

4.6 AMC bay

The board is equipped with 3 AMC-DESY slots. The connectors and its signals are described in the AMC-DESY specification and AMC.1 specification. The same set of signals is available in each slot.

4.7 Clock and trigger distribution

The clock and trigger signals distribution (for single signal) schema is shown in Figure xx. These signals can be generated nt any AMC slot or received through backplane and then distributed to the carrier and all slots. Signals are distributed vi LVDS bus connection. Distribution of clock and trigger signals is shown in Figure xx.

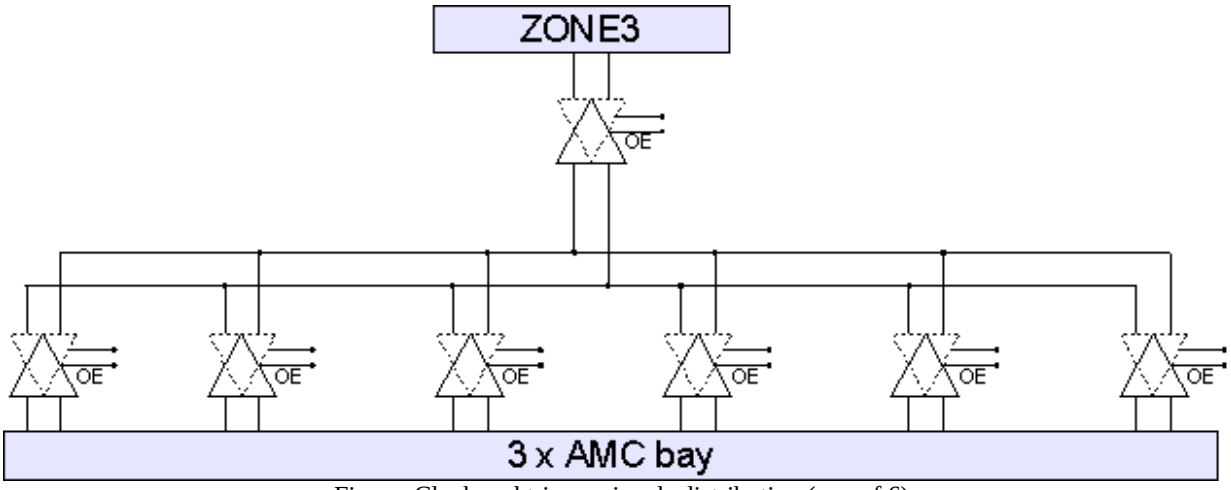


Fig. xx Clock and trigger signals distribution (one of 6)

4.8 Mechanical construction

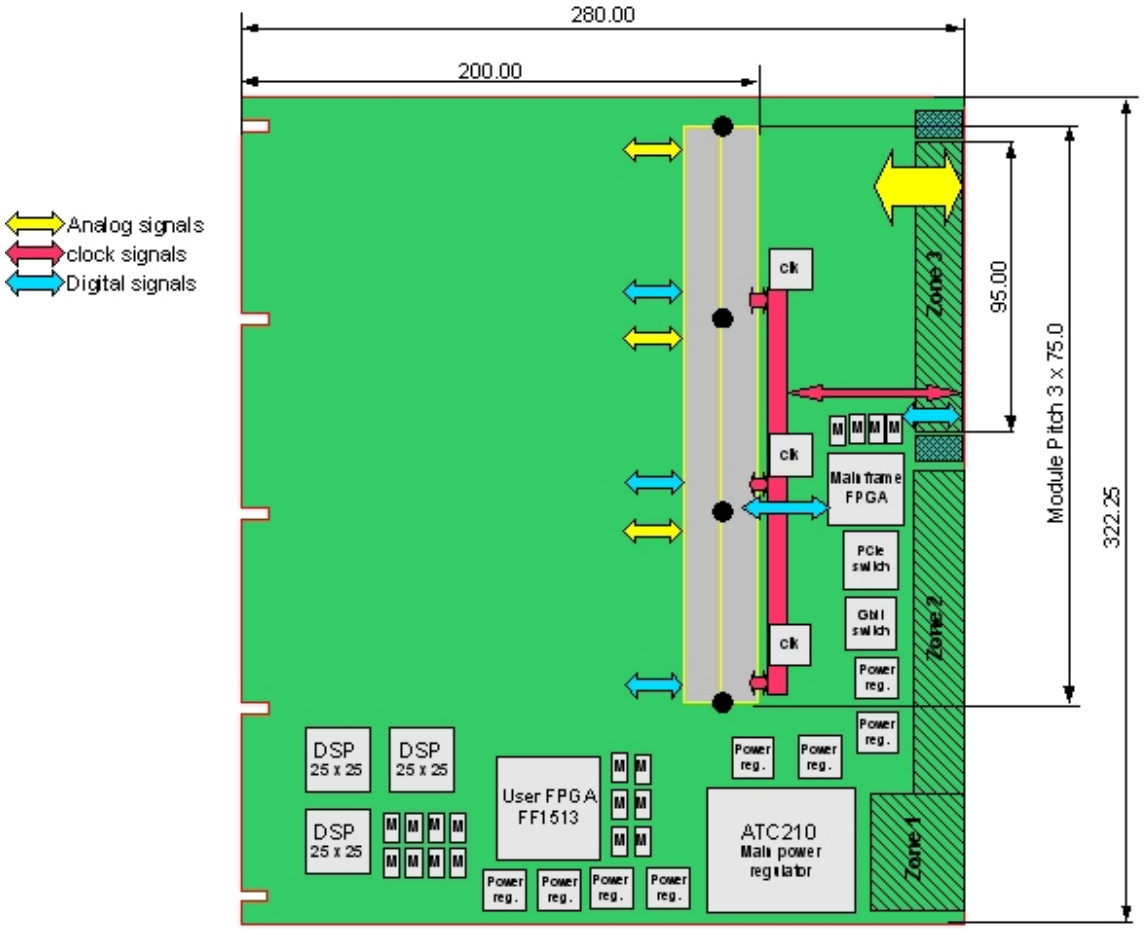
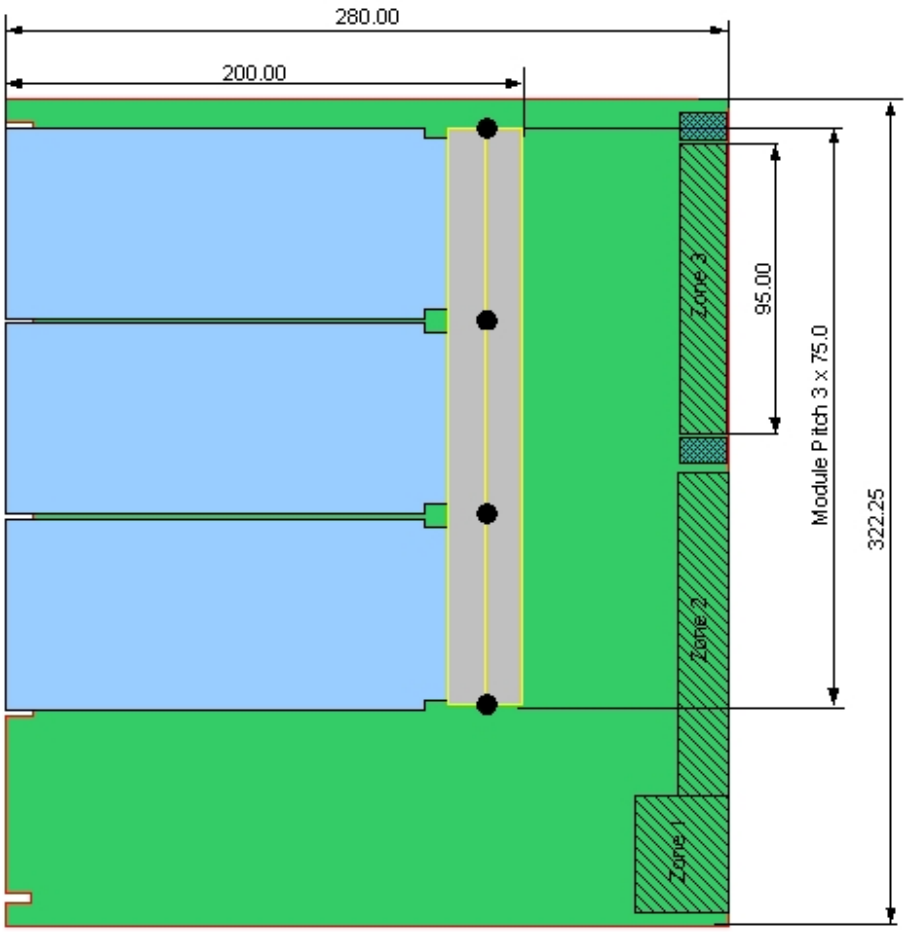


Fig. xx Mainframe FPGA and its connection to other components on the carrier board.

Component profile, cooling, and shielding



Top view

Component profile for AMC modules

Possible solution is shown in Figure 1.

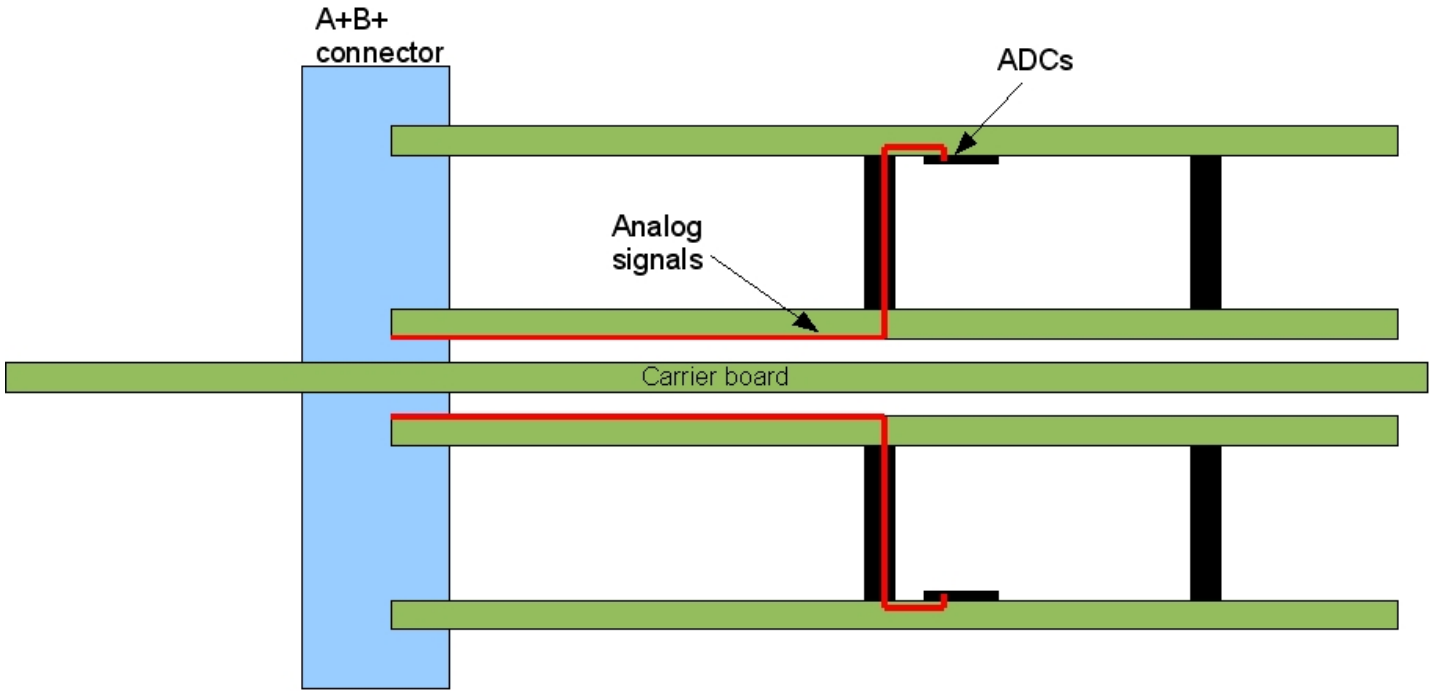


Fig. xx AMC bays on both sides of the carrier board.