SYSTEMACE

SPARTAN3

VIRTEX5

Main FPGA and configuration

CLK

PCIECROSSSWITCH

DSP

POWERSUPPLY

SRAM

SDRAM

Memory blocks

RS232

PHY

IPMC

PCIE

Communiation blocks

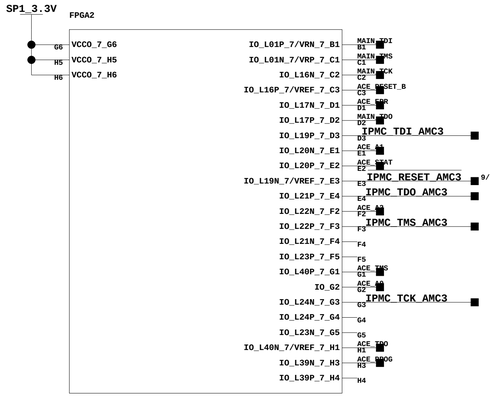
AMC_A_CON

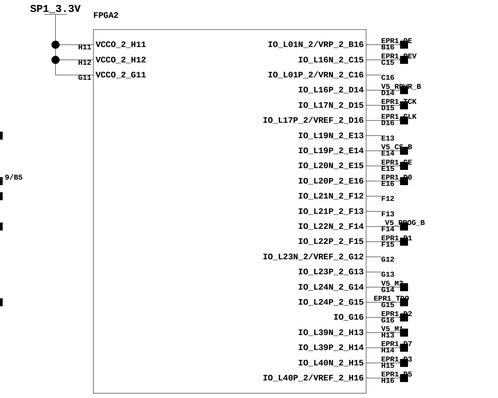
Z3_CON

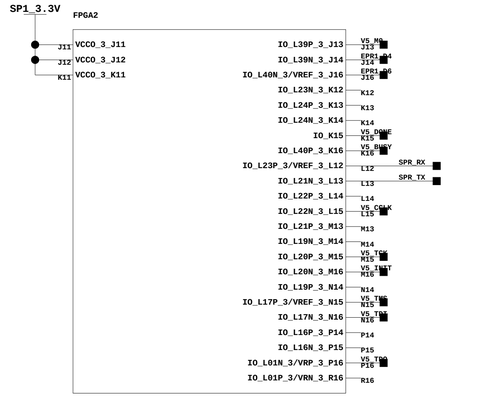
ATCA connectors

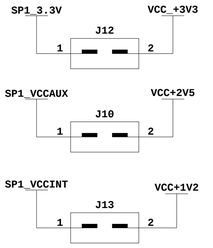
Engineer	DESY- Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev:
		Sheet: 1 of 1	
Drawn by:	Title:		
Changed by:			
Date Changed:	Board Nr: <NR>	Drawing Nr: <NR>	

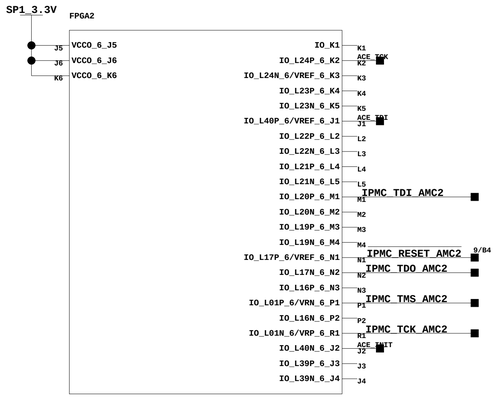
Spartan-3 configuration part

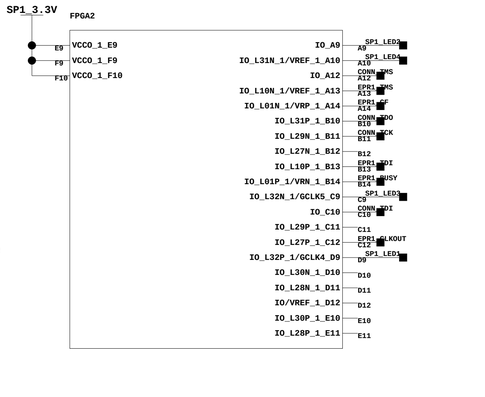


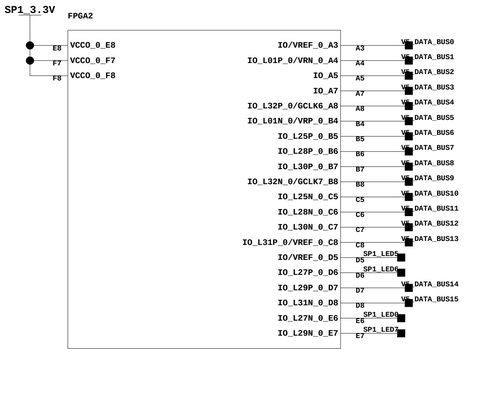


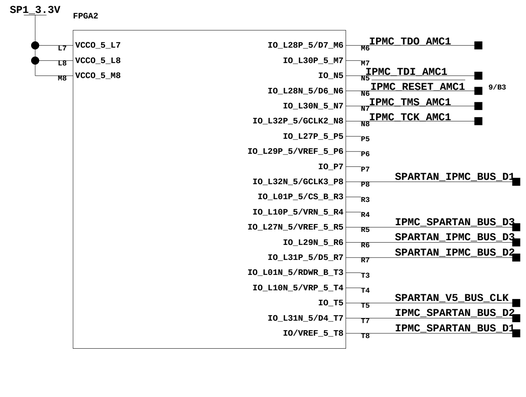


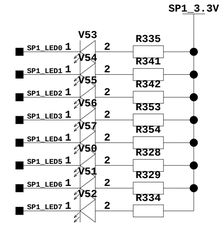


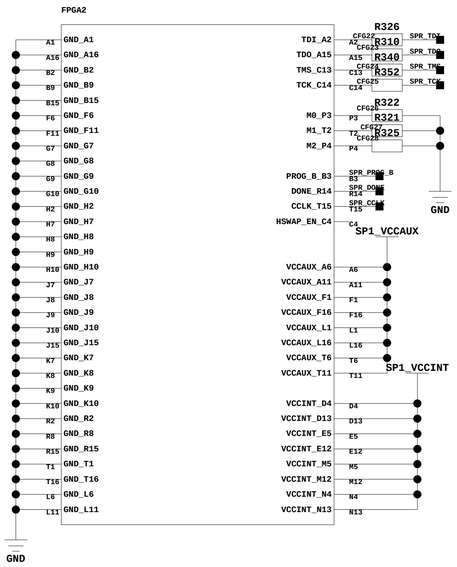


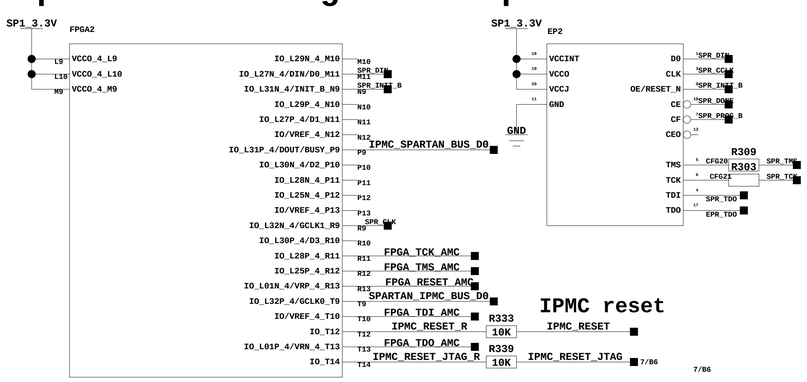


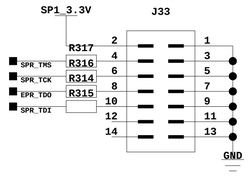


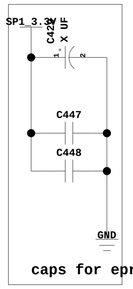


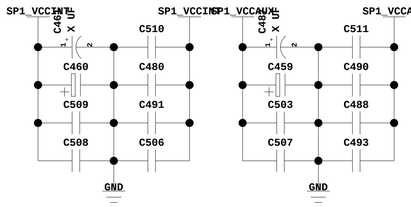




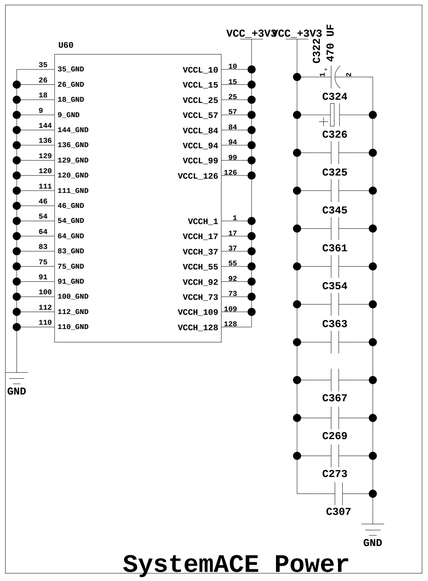


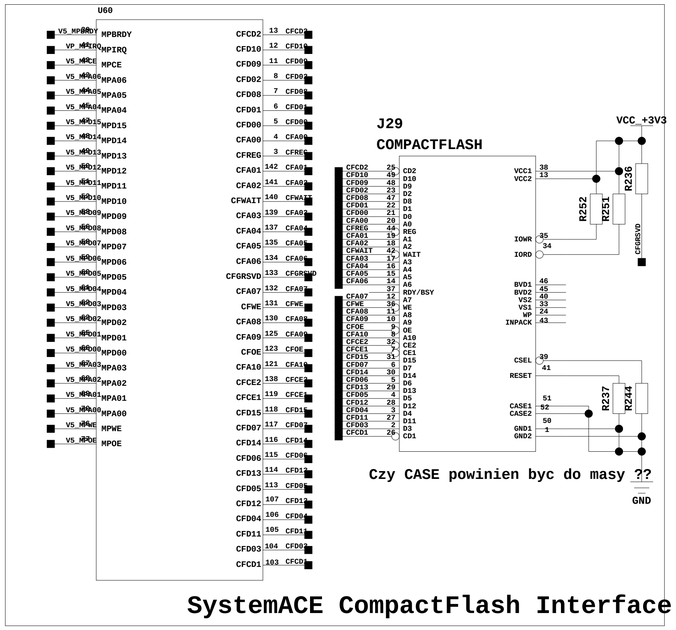






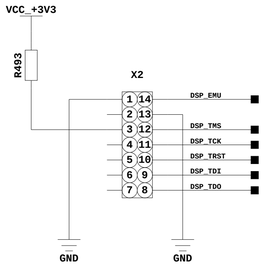
Engineer: WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: SPARTAN 3 FOR VIRTEX 5 CONFIGURATION MANAGE		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

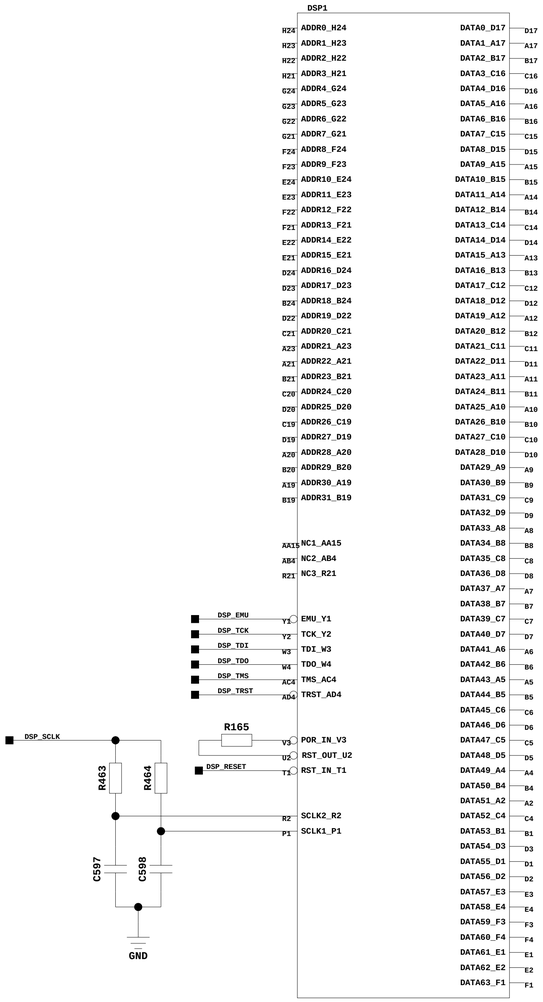


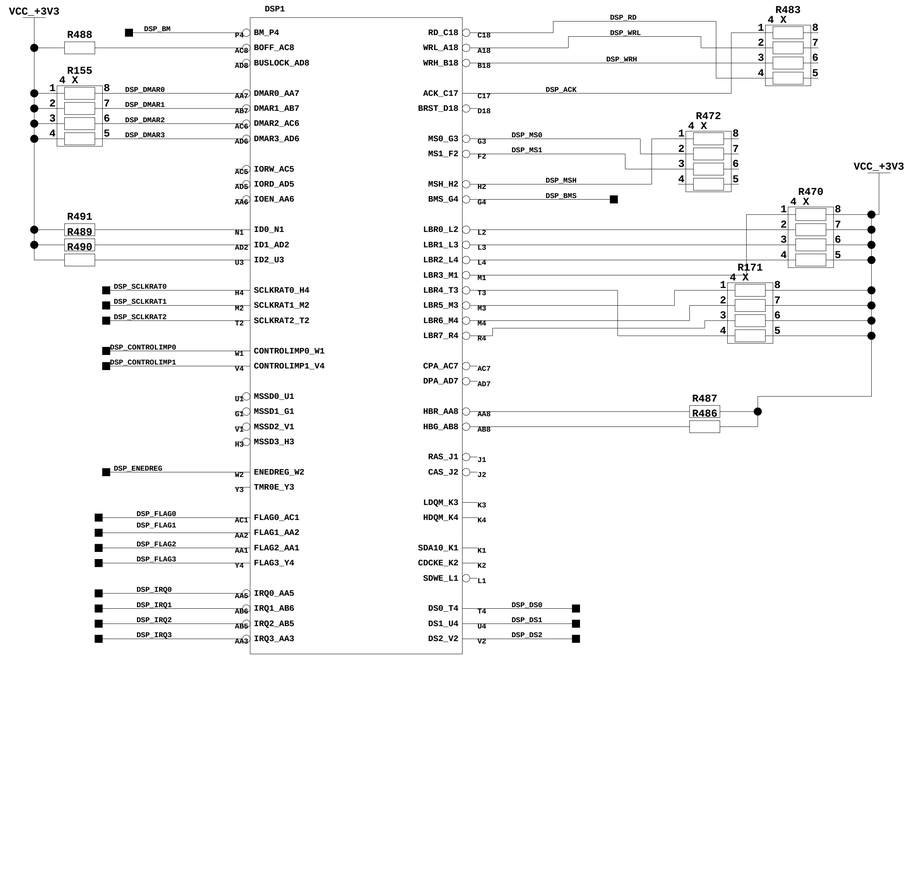


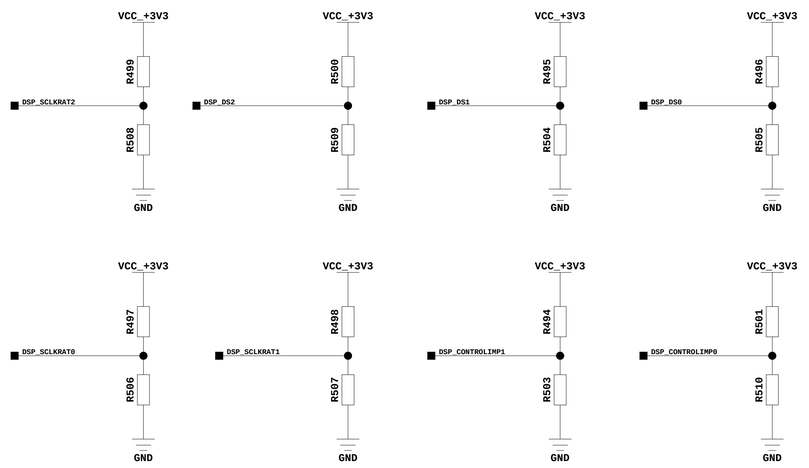
Engineer WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: SYSTEM ACE - COMPACT FLASH PART		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

DSP.1



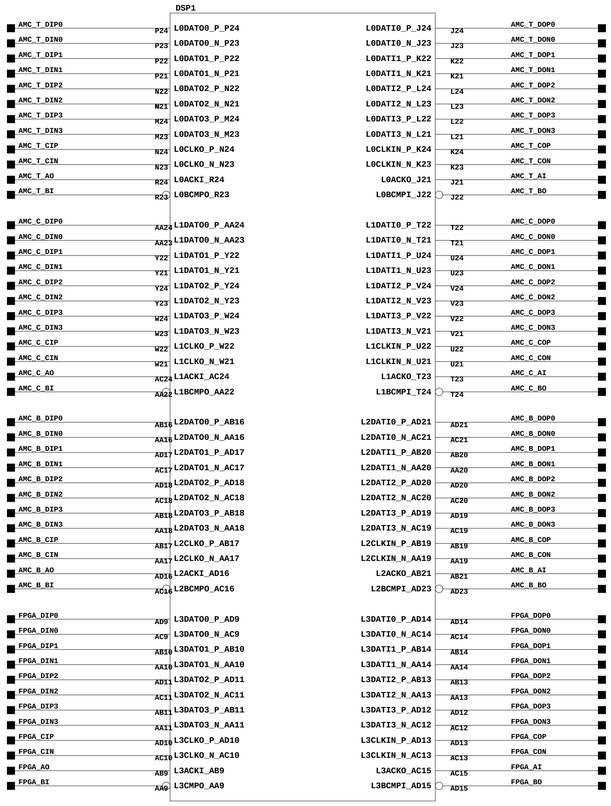


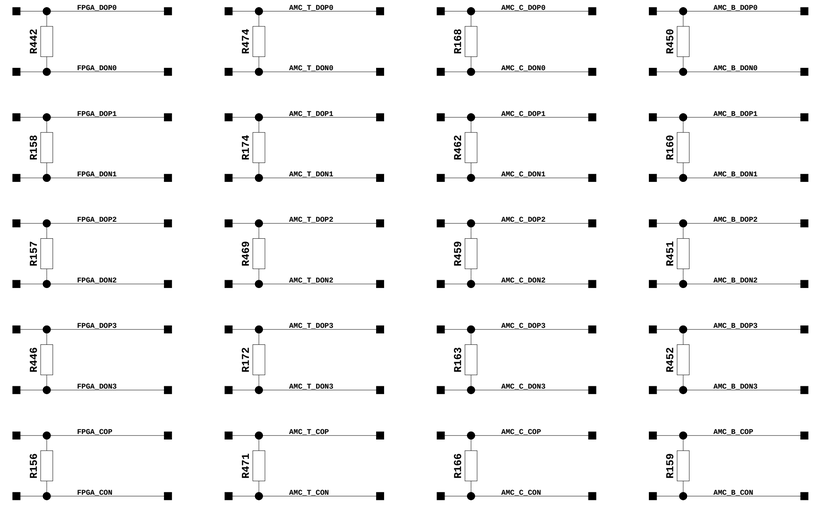




Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet:1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

DSP.2
DSP LINKS





Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

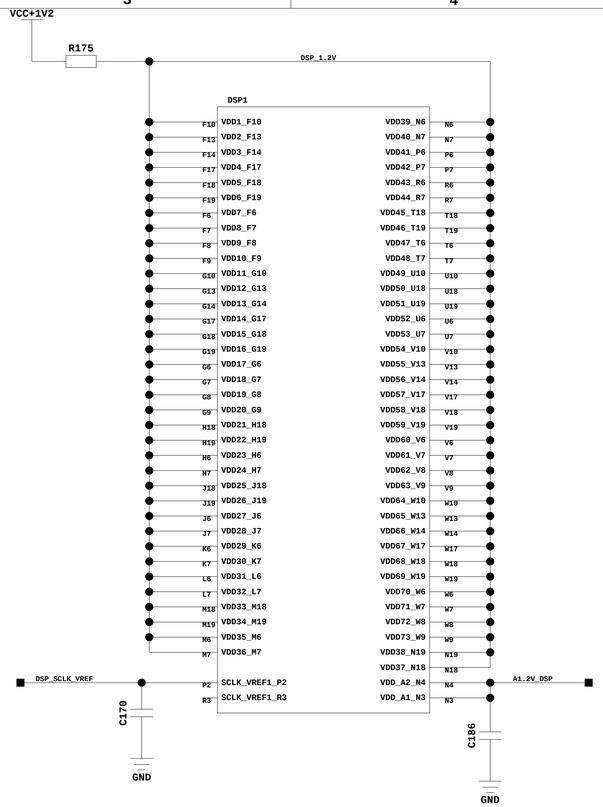
DSP.3
DSP POWER

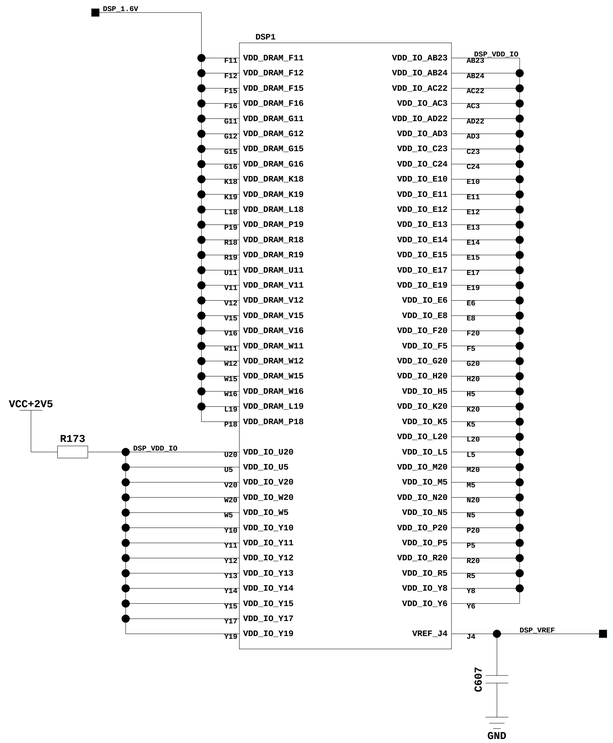
Inputs voltages:

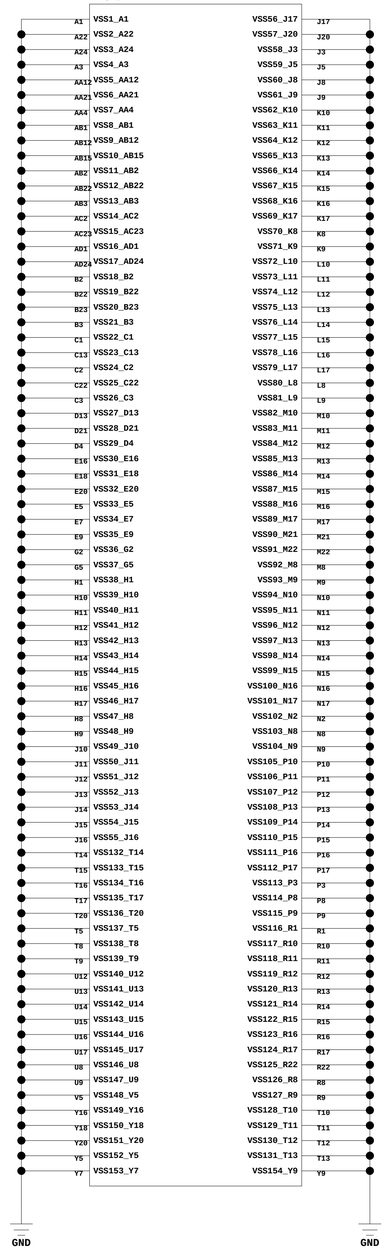
Inputs voltages: 1.2 V @ 3.1 A

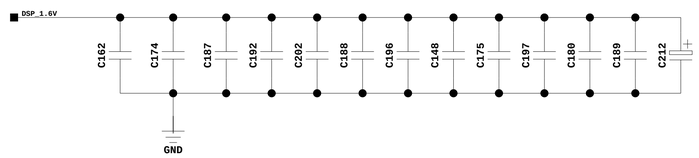
Inputs voltages: 2.5 V @ 250 mA

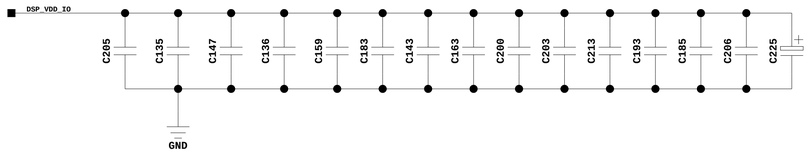
Inputs voltages: 3.3 V @ 500 mA

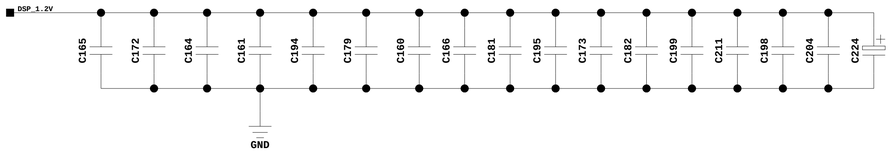








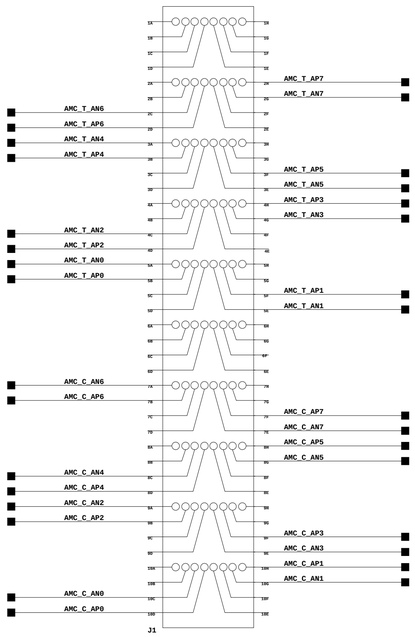




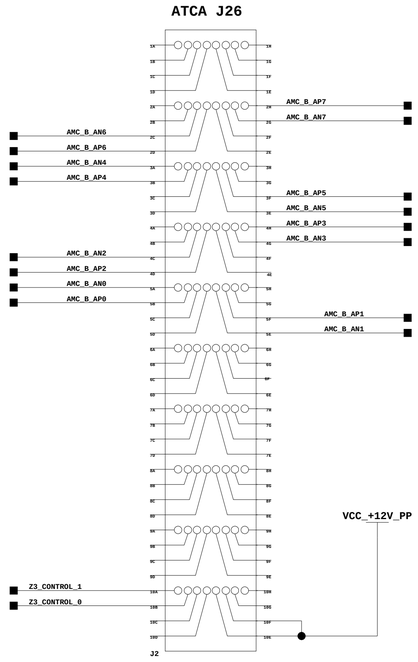
Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet:1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

z3_con

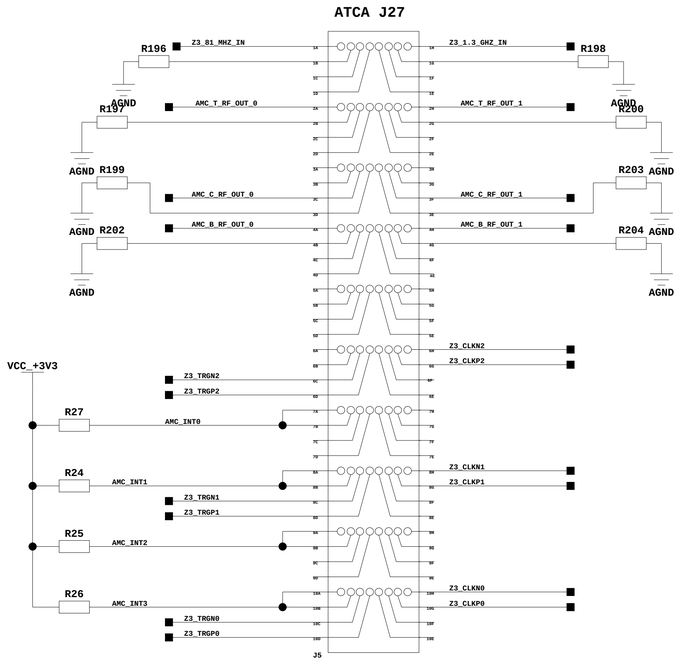
Z3 - TOP - downconverter



Z3 - MIDDLE - downconverter



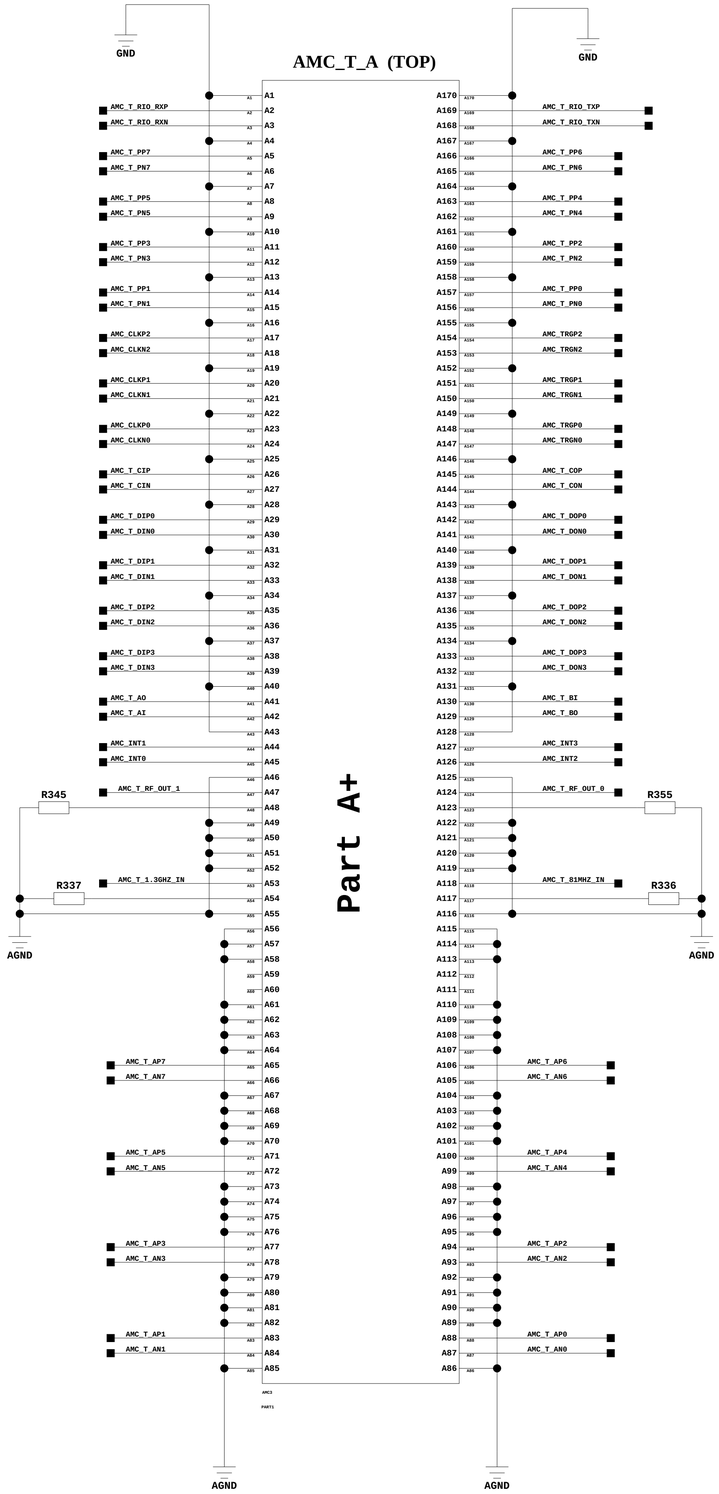
Z3 - BOTTOM - bus

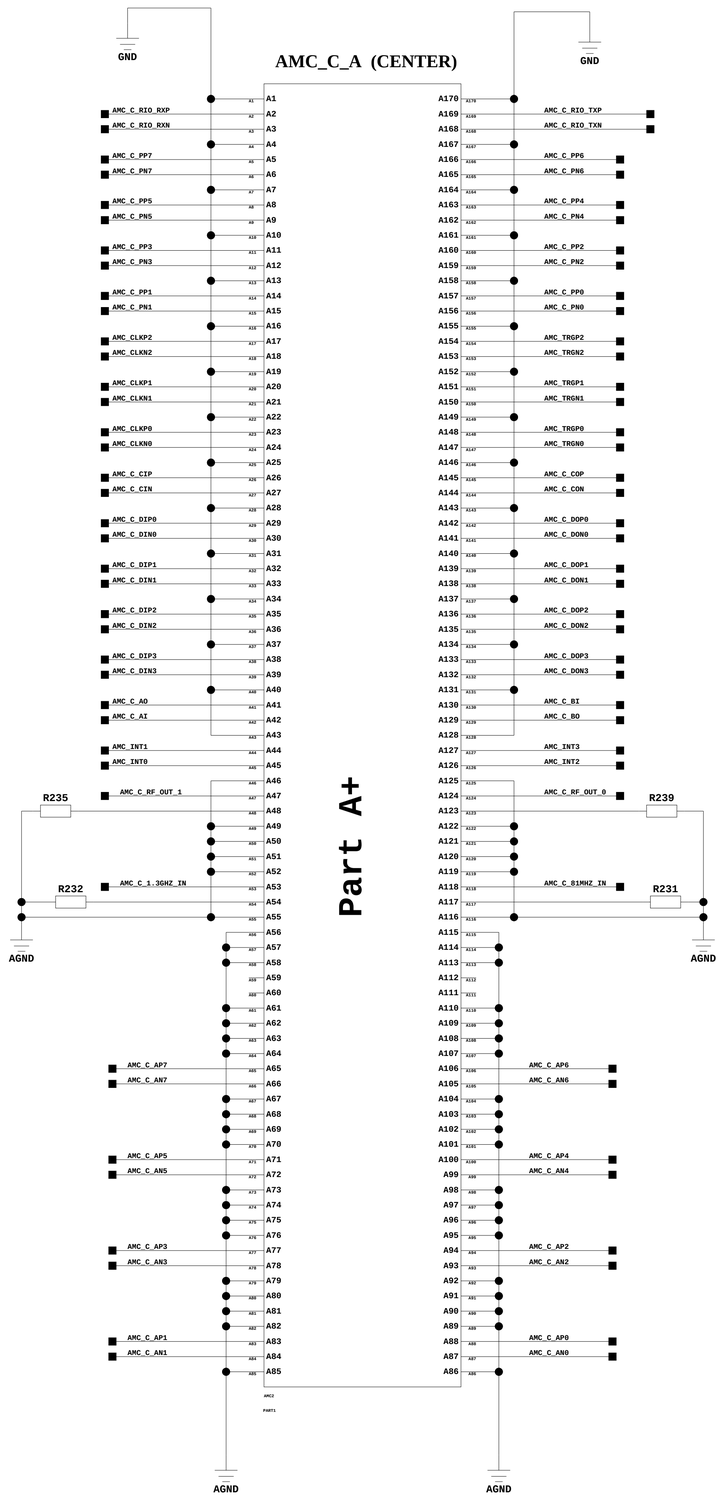


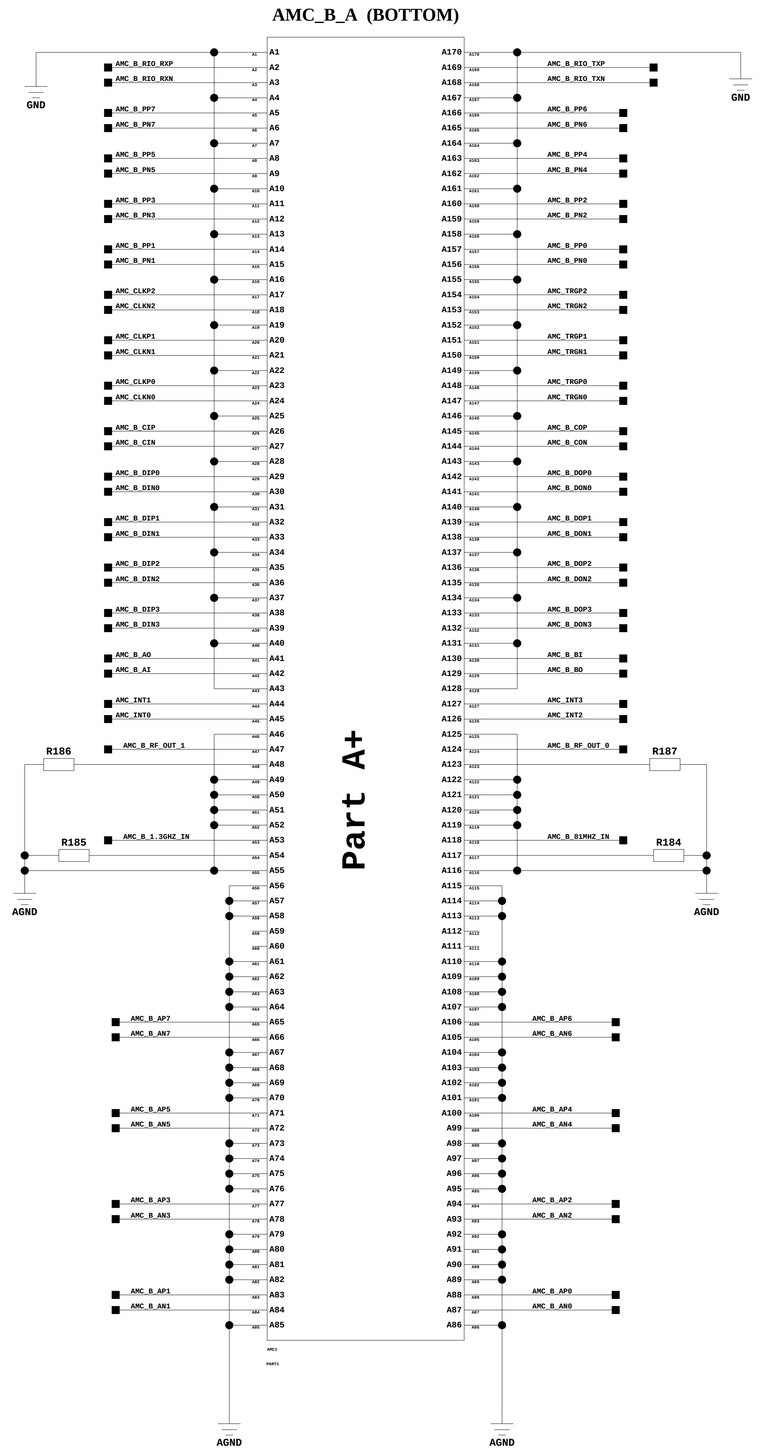
from IPMI or Spartan

Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

amc_a_con





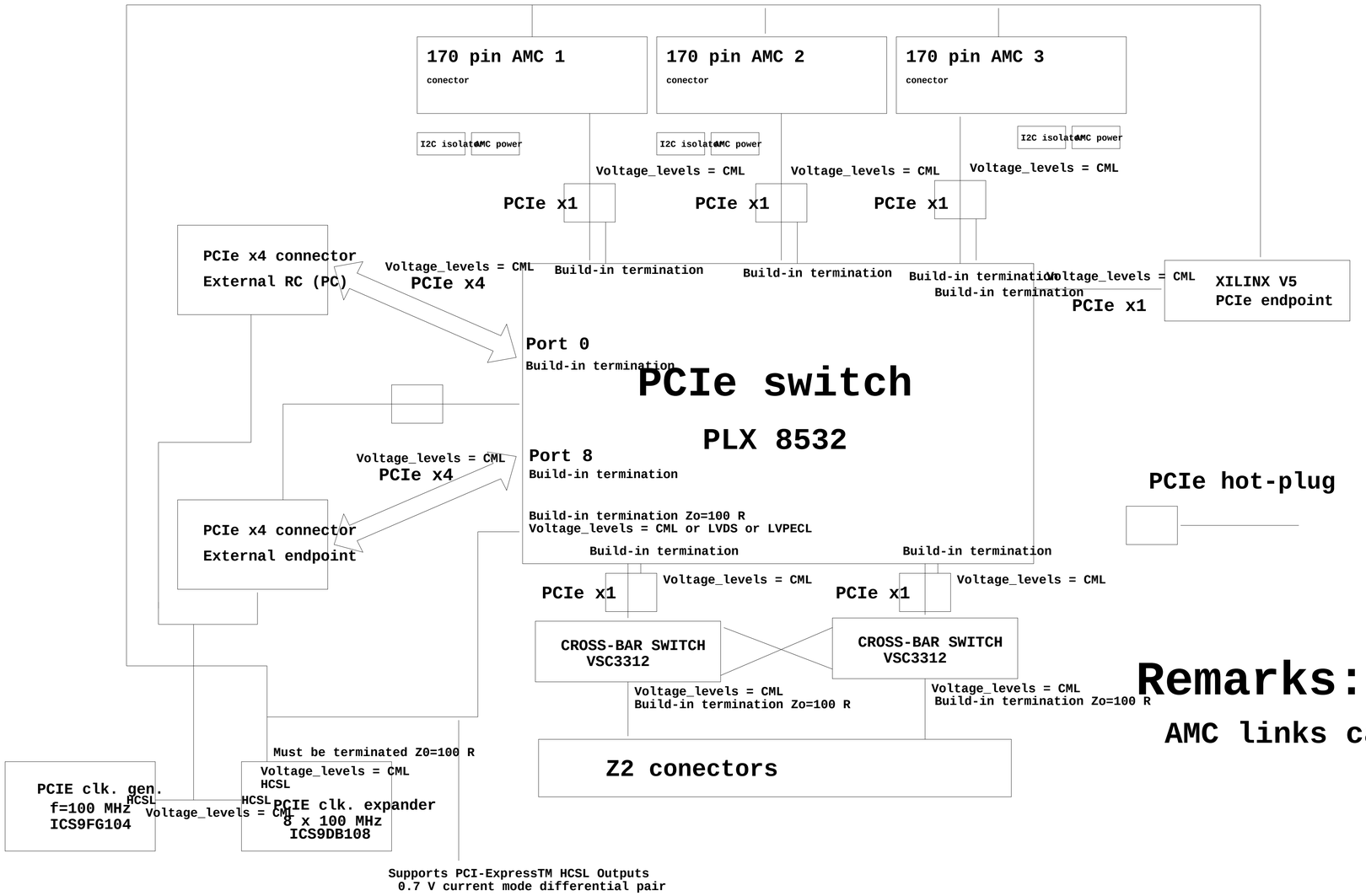


Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

PCIe transmission according to PICMG 3.4, option 1 (x1)

PCIe signals on FAT pipe region ports 4-7, AMC.1 types 1 or 4

PCIe reference clk on CLK3 pins



PCIe hot-plug

Remarks:

AMC links can be routed as PCIe x4 i

Check if lane polarity, lane ordering, lane width are supported b

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE BLOCK DIAGRAM		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

PCIe switch power supply (2)

PCIE_+3V3_IO

Upstream NT-port selection
All conf. possible
No upstream = [H, H, H, H]

R313 3 10K
R308 3 10K
DEFAULT_SETTING=2-3
DEFAULT_SETTING=2-3
R232 4X4K7
SW5

Upstream port selection
All conf. possible
Port 0 = [L, L, L, L]

Transparent mode
Transp. = [H, H]

R233 4X4K7
SW7

GND

Hardwired configuration to 4x4/4x4
LLLLL = [x4, x4, x4, x4]

PCIE_+3V3_IO

R312 4X4K7
R105 4K7
R104 4K7
R307 4X4K7
R290 4K7

R93 0R PCIE_RESET_0# → 6/F1
R94 DNM PCIE_SWITCH_PERST_I → 4/D3

Analogue part capacitors

PCIE_+1V5_VTT
PCIE_+3V3_IO
PCIE_+1V_CORE
PCIE_+1V_CORE

U32

2/B7 PCIE_JTAG_TCK J2 → JTAG_TCK
2/B7 PCIE_JTAG_TDI K2 → JTAG_TDI
2/B7 PCIE_JTAG_TDO J3 → JTAG_TDO
2/B7 PCIE_JTAG_TMS J4 → JTAG_TMS
2/B7 PCIE_JTAG_TRST_N K4 → JTAG_TRST#
JTAG PORT

PERST_in cold/warm reset, min. 100 ms, no glitch allowed
PCIE_SWITCH_RESET_O_N J1 → PEX_NT_RESET#
PCIE_SWITCH_PERST_SW_I_N N1 → PEX_PERST#
REFERENCE CLOCK AND RESET

5/A8 PCIE_CLK_SWITCH_P AL2 → PEX_REFCLKP
5/A8 PCIE_CLK_SWITCH_N AL1 → PEX_REFCLKN

7/D5 CS_PCIE_EEPROM# AG32 → EE_CS#
7/D5 SO_PCIE_EEPROM AG34 → EE_DO
7/D5 SI_PCIE_EEPROM AH34 → EE_DI
EEPROM_PRESENT 7/D5 AH33 → EE_PRE
7/D5 SCK_PCIE_EEPROM AG33 → EE_SK
EEPROM INTERFACE

AF4 → NC_PROCMON

PCIE_STRAP_NT_UPSTREAM_1 K32 → STRAP_NT_UPSTRM_PORT_SEL[0]
PCIE_STRAP_NT_UPSTREAM_2 L32 → STRAP_NT_UPSTRM_PORT_SEL[1]
PCIE_STRAP_NT_UPSTREAM_2 L31 → STRAP_NT_UPSTRM_PORT_SEL[2]
PCIE_STRAP_NT_UPSTREAM_3 M31 → STRAP_NT_UPSTRM_PORT_SEL[3]
NON-TRANSPARENT UPSTREAM PORT SELECTION

G1 → STRAP_MODE_SEL[0]
H2 → STRAP_MODE_SEL[1]

M3 → STRAP_UPSTRM_PORT_SEL[0]
N3 → STRAP_UPSTRM_PORT_SEL[1]
M4 → STRAP_UPSTRM_PORT_SEL[2]
N4 → STRAP_UPSTRM_PORT_SEL[3]
UPSTREAM PORT SELECTION

AE32 → STRAP_STN0_PORTCFG[0]
AD31 → STRAP_STN0_PORTCFG[1]
AD32 → STRAP_STN0_PORTCFG[2]
AC31 → STRAP_STN0_PORTCFG[3]
AC32 → STRAP_STN0_PORTCFG[4]
STN0 PORT CONFIGURATION

M32 → STRAP_STN1_PORTCFG[0]
N31 → STRAP_STN1_PORTCFG[1]
N32 → STRAP_STN1_PORTCFG[2]
P31 → STRAP_STN1_PORTCFG[3]
P32 → STRAP_STN1_PORTCFG[4]
STN1 PORT CONFIGURATION

H3* → STRAP_PROBE#
K3* → STRAP_PROM#
J3* → STRAP_DEBUG_SEL1
J31 → STRAP_DEBUG_SEL2
DEBUG MODE SELECTION (FACTORY USE)

AH* → STRAP_PLL_BYPASS#
AH* → STRAP_FACTORY_TEST1#

G34 → STRAP_TEST_MODE[0]
G33 → STRAP_TEST_MODE[1]
H34 → STRAP_TEST_MODE[2]
H33 → STRAP_TEST_MODE[3]
AG3* → STRAP_FACTORY_TEST2#
TEST MODE SELECTION (FACTORY USE)

PCIE_+3V3_PLL
H31 NC-3
G32 NC-1
G2 NC-2
AH5 VDD33A
AH4 VSSA_PLL

PEX8532BC_EHBGA680

GND

Supply voltage filter (use inductance if required)

PCIE_+3V3_IO — R285 10R — PCIE_+3V3_PLL
C390 100NF → GND

PLX PEX 8532BC - EHBGA680

POWER, CONFIGURATION,EEPROM,JTAG

JTAG connector

PCIE_+3V3_IO
R401 4K7
R405 4K7
R410 4K7
J14
2/B2 PCIE_JTAG_TRST_N 1 2
2/B2 PCIE_JTAG_TDI 3 4
2/B2 PCIE_JTAG_TDO 5 6
2/B2 PCIE_JTAG_TMS 7 8
2/B2 PCIE_JTAG_TCK 9 10
R413 1K5
GND
GND

PCIE_+1V_CORE

C406 100NF C444 100NF C378 100NF C397 100NF C437 100NF C379 100NF
C419 100NF C446 100NF C450 100NF C454 100NF C453 100NF C439 100NF C371 100NF C414 100NF
C373 100NF C442 100NF C445 100NF C452 100NF C391 100NF C376 100NF C464 100NF C456 100NF
C443 10NF C382 10NF C440 10NF C383 10NF C466 10NF C438 10NF C405 10NF C394 10NF
C395 10NF C384 10NF C393 10NF C385 10NF C386 10NF C422 10NF C441 10NF C392 10NF
GND

PCIE_+3V3_IO PCIE_+1V5_VTT PCIE_+1V_CORE
C415 100UF C470 100UF C402 100UF
GND GND GND

PCIE_+1V5_VTT
C372 100NF C368 100NF C370 100NF C463 100NF
C471 10NF C465 10NF C472 10NF C377 10NF
GND

PCIE_+3V3_IO
C401 100NF C416 100NF C407 100NF C410 100NF C425 100NF C420 100NF C435 100NF C418 100NF
C421 10UF C398 100NF
GND

Analogue part capacitors

PCIE_+1V_CORE
C451 100NF C411 100NF C434 100NF C375 100NF
C455 100NF C374 100NF C426 100NF C396 100NF
GND

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 2 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE CONFIGURATION AND POWER SUPPLY #1		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

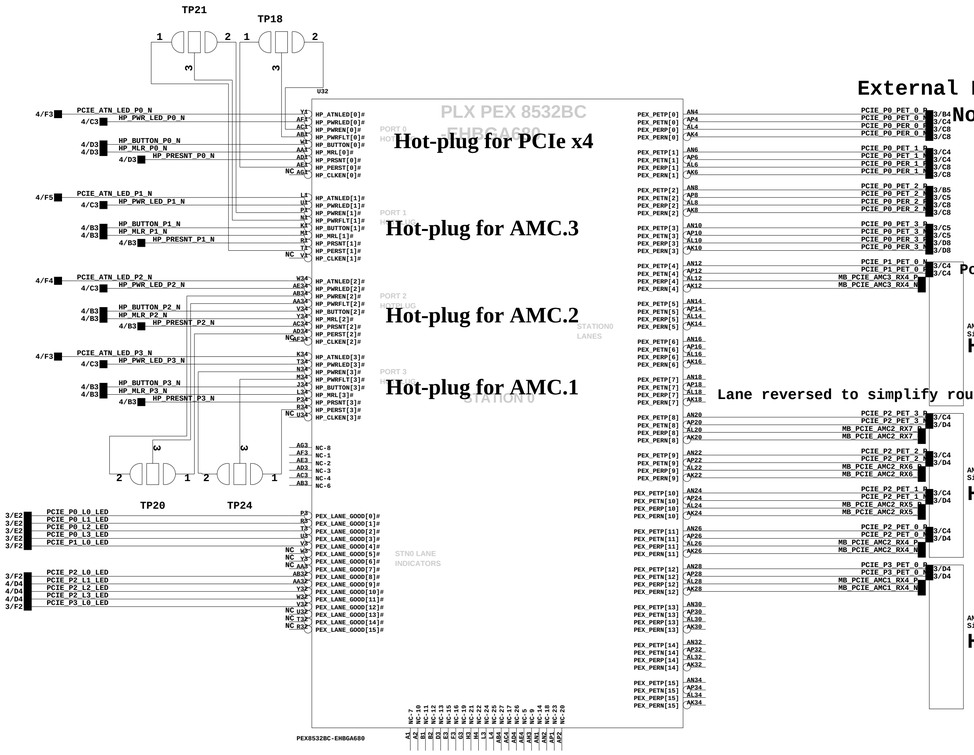
PCIe switch - slot 0

Main logic and Xilinx IO/3.3V power supply 10A/3V3

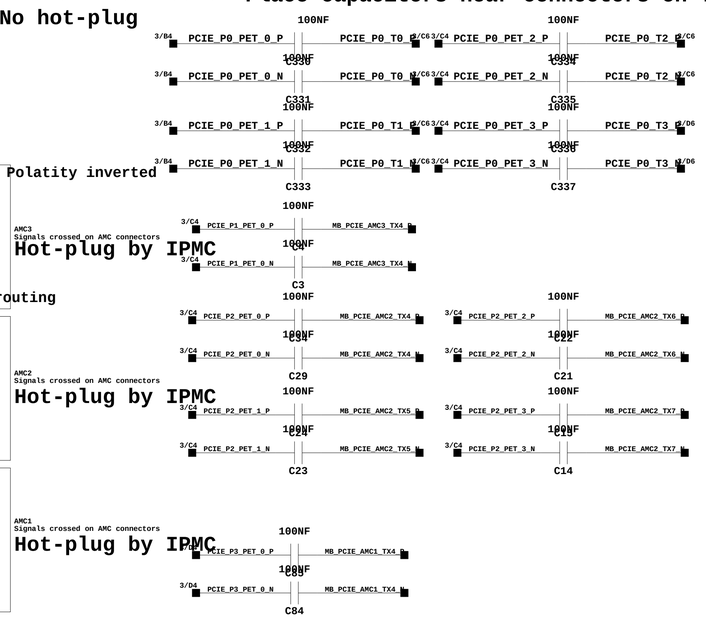
MLR connect to PRSNT

PER/PET must be crossed on the PCIE external cable

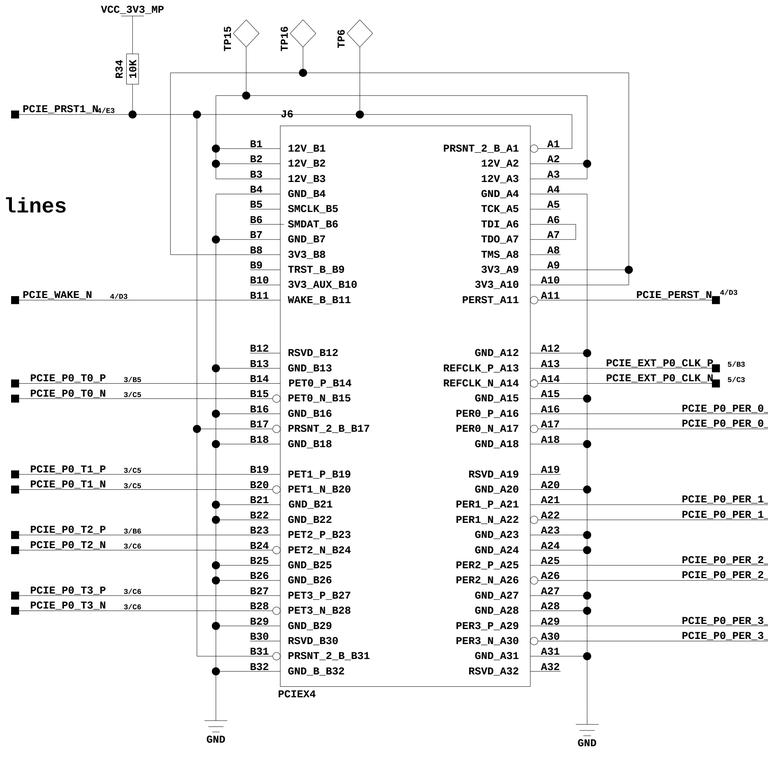
PET_p/PET_n are transmitter outputs from ATCA switch
PER_p/PER_n are receiver inputs of the ATCA switch

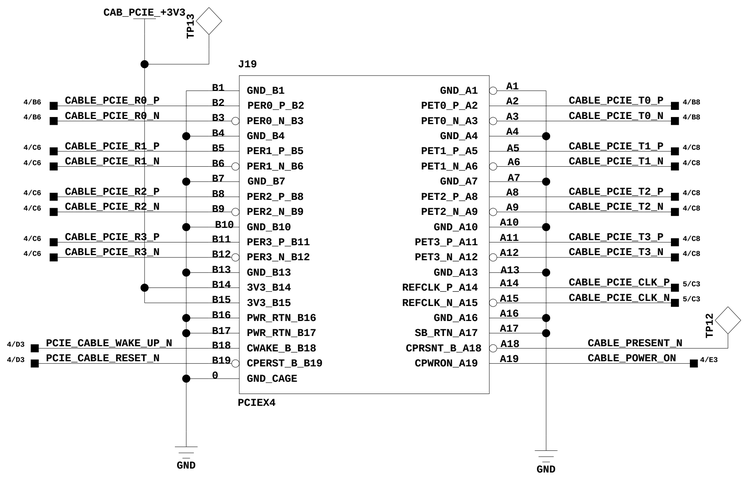


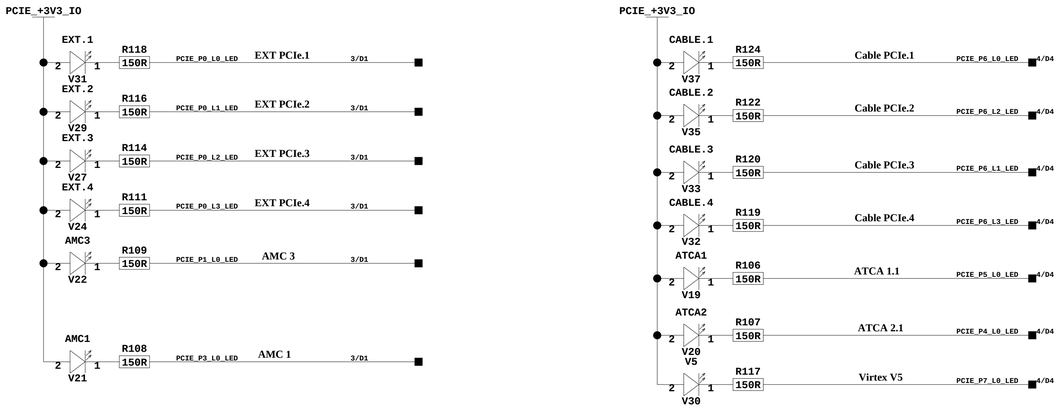
External PCIe x4 standard connector
No hot-plug
Polatity inverted
Lane reversed to simplify routing

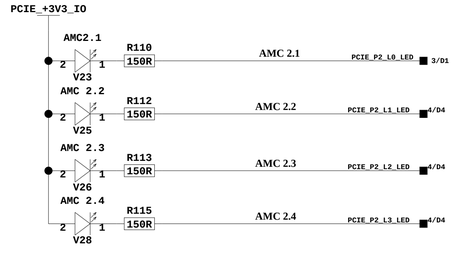


Place capacitors near connectors on Tx lines









ext+cable PCIE x4, 2x ATCA x1, 3x AMC x1 + V5 = 8+6 = 14 LED

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 3 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE I/O #1		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

PCIe switch - slot 1

5x MLR, SWITCH, PRST, PWRLED = 20 signals to FPGA

VCC_3V3_MP

FPGA1

J5	VCCO_6_J5	IO_K1	K1	HP_PRESNT_P10_N 4/C4
J6	VCCO_6_J6	IO_L24P_6_K2	K2	HP_PRESNT_P3_N 3/C1
K6	VCCO_6_K6	IO_L24N_6/VREF_6_K3	K3	HP_MLR_P10_N 4/C4
		IO_L23P_6_K4	K4	CABLE_POWER_ON 3/E8
		IO_L23N_6_K5	K5	
		IO_L40P_6/VREF_6_J1	J1	HP_BUTTON_P3_N 3/C1
		IO_L22P_6_L2	L2	HP_PWR_LED_P3_N 3/C1
		IO_L22N_6_L3	L3	HP_BUTTON_P10_N 4/C4
		IO_L21P_6_L4	L4	PCIE_CABLE_RESET_N 3/E6
		IO_L21N_6_L5	L5	
		IO_L20P_6_M1	M1	HP_BUTTON_P11_N 4/C4
		IO_L20N_6_M2	M2	HP_PWR_LED_P11_N 4/C4
		IO_L19P_6_M3	M3	HP_MLR_P2_N 3/C1
		IO_L19N_6_M4	M4	PCIE_CABLE_WAKE_UP_N 3/E6
		IO_L17P_6/VREF_6_N1	N1	HP_PRESNT_P11_N 4/C4
		IO_L17N_6_N2	N2	HP_PWR_LED_P2_N 3/C1
		IO_L16P_6_N3	N3	HP_MLR_P11_N 4/C4
		IO_L01P_6/VRN_6_P1	P1	HP_PRESNT_P2_N 3/C1
		IO_L16N_6_P2	P2	HP_BUTTON_P2_N 3/C1
		IO_L01N_6/VRP_6_R1	R1	PCIE_ENABLE_I /D1,7/C5
		IO_L40N_6_J2	J2	HP_PWR_LED_P10_N 4/C4
		IO_L39P_6_J3	J3	HP_MLR_P3_N 3/C1
		IO_L39N_6_J4	J4	

VCC_3V3_MP

FPGA1

G6	VCCO_7_G6	IO_L01P_7/VRN_7_B1	B1	MMC_LED0 7/B2
H5	VCCO_7_H5	IO_L01N_7/VRP_7_C1	C1	HP_PWR_LED_P0_N 3/B1
H6	VCCO_7_H6	IO_L16N_7_C2	C2	HP_MLR_P9_N 4/C4
		IO_L16P_7/VREF_7_C3	C3	HP_BUTTON_P9_N 4/C4
		IO_L17N_7_D1	D1	HP_PRESNT_P0_N 3/B1
		IO_L17P_7_D2	D2	HP_MLR_P0_N 3/B1
		IO_L19P_7_D3	D3	HP_PRESNT_P9_N 4/C4
		IO_L20N_7_E1	E1	HP_PWR_LED_P9_N 4/C4
		IO_L20P_7_E2	E2	HP_BUTTON_P0_N 3/B1
		IO_L19N_7/VREF_7_E3	E3	HP_BUTTON_P1_N 3/C1
		IO_L21P_7_E4	E4	PCIE_CROSS_STAT0 2/C3
		IO_L22N_7_F2	F2	HP_PWR_LED_P8_N 4/B4
		IO_L22P_7_F3	F3	HP_MLR_P1_N 3/C1
		IO_L21N_7_F4	F4	PCIE_CROSS_CONFIG 2/C3
		IO_L23P_7_F5	F5	PCIE_CROSS_STAT1 2/C3
		IO_L40P_7_G1	G1	HP_BUTTON_P8_N 4/B4
		IO_G2	G2	HP_PWR_LED_P1_N 3/C1
		IO_L24N_7_G3	G3	HP_MLR_P8_N 4/B4
		IO_L24P_7_G4	G4	
		IO_L23N_7_G5	G5	PCIE_RESET_O# /C3,4/B4
		IO_L40N_7/VREF_7_H1	H1	HP_PRESNT_P1_N 3/C1
		IO_L39N_7_H3	H3	HP_PRESNT_P8_N 4/B4
		IO_L39P_7_H4	H4	

VCC_3V3_MP

FPGA1

E8	VCCO_0_E8	IO/VREF_0_A3	A3	MMC_LED1 7/B2
F7	VCCO_0_F7	IO_L01P_0/VRN_0_A4	A4	PCIE_CLK_EN0 5/C5
F8	VCCO_0_F8	IO_A5	A5	PCIE_CLK_GOOD
		IO_A7	A7	PCIE_CLK_EN6 5/C5
		IO_L32P_0/GCLK6_A8	A8	PCIE_CLK_EN1 5/C5
		IO_L01N_0/VRP_0_B4	B4	RIO_CROSS_STAT0 4/B4
		IO_L25P_0_B5	B5	PCIE_CLK_EN3 5/C5
		IO_L28P_0_B6	B6	PCIE_CLK_EN4 5/C5
		IO_L30P_0_B7	B7	PCIE_CLK_EN5 5/C5
		IO_L32N_0/GCLK7_B8	B8	PCIE_CLK_EN2 5/C5
		IO_L25N_0_C5	C5	RIO_CROSS_CONFIG 4/B4
		IO_L28N_0_C6	C6	PCIE_CLK_EN7 5/D5
		IO_L30N_0_C7	C7	I2C_EN_ATCA_A
		IO_L31P_0/VREF_0_C8	C8	
		IO/VREF_0_D5	D5	RIO_CROSS_STAT1 4/C4
		IO_L27P_0_D6	D6	PCIE_SWITCH_PERST_N
		IO_L29P_0_D7	D7	HP_BUTTON_1
		IO_L31N_0_D8	D8	
		IO_L27N_0_E6	E6	PCIE_SWITCH_RESET_O_N
		IO_L29N_0_E7	E7	I2C_EN_ATCA_B

TP19 TP23

TP25 TP22

PCIE_P4_L0_LED 3/E4

PCIE_P5_L0_LED 3/F4

PCIE_P6_L0_LED 3/F4
PCIE_P6_L1_LED 3/E4
PCIE_P6_L2_LED 3/E4
PCIE_P6_L3_LED 3/E4
PCIE_P7_L0_LED 3/F4

U32

PLX PEX 8532BC -FHBGA680

PEX8532BC-EHBGA680

4/F3	PCIE_ATN_LED_P8_N	4/C3	HP_PWR_LED_P8_N
4/B3	HP_BUTTON_P8_N	4/B3	HP_MLR_P8_N
4/B3	HP_PRESNT_P8_N		
4/F3	PCIE_ATN_LED_P9_N	4/C3	HP_PWR_LED_P9_N
4/B3	HP_BUTTON_P9_N	4/B3	HP_MLR_P9_N
4/B3	HP_PRESNT_P9_N		
4/F3	PCIE_ATN_LED_P10_N	4/C3	HP_PWR_LED_P10_N
4/B3	HP_BUTTON_P10_N	4/B3	HP_MLR_P10_N
4/B3	HP_PRESNT_P10_N		
4/F3	PCIE_ATN_LED_P11_N	4/C3	HP_PWR_LED_P11_N
4/D3	HP_BUTTON_P11_N	4/D3	HP_MLR_P11_N
4/D3	HP_PRESNT_P11_N		

Hot-plug for CON x4

Hot-plug for ATCA.2

Hot-plug for ATCA.1

Hot-plug for V5

STATION 1

STATION1 LANES

STN1 LANE INDICATORS

PEX_PETP[16]	B4	PCIE_ATCA2_TXP	
PEX_PETN[16]	A4	PCIE_ATCA2_TXN	
PEX_PERP[16]	D1	PCIE_ATCA2_RXN	
PEX_PERN[16]	E1	PCIE_ATCA2_RXP	
PEX_PETP[17]	B6		
PEX_PETN[17]	A6		
PEX_PERP[17]	D5		
PEX_PERN[17]	E5		
PEX_PETP[18]	B8		
PEX_PETN[18]	A8		
PEX_PERP[18]	D9		
PEX_PERN[18]	E8		
PEX_PETP[19]	B10		
PEX_PETN[19]	A10		
PEX_PERP[19]	D10		
PEX_PERN[19]	E10		
PEX_PETP[20]	B12	PCIE_ATCA1_TXN	
PEX_PETN[20]	A12	PCIE_ATCA1_TXP	
PEX_PERP[20]	D12	PCIE_ATCA1_RXP	
PEX_PERN[20]	E12	PCIE_ATCA1_RXN	
PEX_PETP[21]	B14		
PEX_PETN[21]	A14		
PEX_PERP[21]	D14		
PEX_PERN[21]	E14		
PEX_PETP[22]	B16		
PEX_PETN[22]	A16		
PEX_PERP[22]	D16		
PEX_PERN[22]	E16		
PEX_PETP[23]	B18		
PEX_PETN[23]	A18		
PEX_PERP[23]	D18		
PEX_PERN[23]	E18		
PEX_PETP[24]	B20	PCIE_P8_PET_0_N	4/B7
PEX_PETN[24]	A20	PCIE_P8_PET_0_P	4/B7
PEX_PERP[24]	D20	CABLE_PCIE_R0_N	3/D6
PEX_PERN[24]	E20	CABLE_PCIE_R0_P	3/D6
PEX_PETP[25]	B22	PCIE_P8_PET_1_N	4/C7
PEX_PETN[25]	A22	PCIE_P8_PET_1_P	4/C7
PEX_PERP[25]	D22	CABLE_PCIE_R1_N	3/E6
PEX_PERN[25]	E22	CABLE_PCIE_R1_P	3/E6
PEX_PETP[26]	B24	PCIE_P8_PET_2_N	4/C7
PEX_PETN[26]	A24	PCIE_P8_PET_2_P	4/C7
PEX_PERP[26]	D24	CABLE_PCIE_R2_N	3/E6
PEX_PERN[26]	E24	CABLE_PCIE_R2_P	3/E6
PEX_PETP[27]	B26	PCIE_P8_PET_3_N	4/C7
PEX_PETN[27]	A26	PCIE_P8_PET_3_P	4/C7
PEX_PERP[27]	D26	CABLE_PCIE_R3_N	3/E6
PEX_PERN[27]	E26	CABLE_PCIE_R3_P	3/E6
PEX_PETP[28]	B28	PCIE_P11_PET_0_N	4/D7
PEX_PETN[28]	A28	PCIE_P11_PET_0_P	4/D7
PEX_PERP[28]	D28	PCIE_P11_PER_0_N	4/D7
PEX_PERN[28]	E28	PCIE_P11_PER_0_P	4/D7
PEX_PETP[29]	B30		
PEX_PETN[29]	A30		
PEX_PERP[29]	D30		
PEX_PERN[29]	E30		
PEX_PETP[30]	B32		
PEX_PETN[30]	A32		
PEX_PERP[30]	D32		
PEX_PERN[30]	E32		
PEX_PETP[31]	B34		
PEX_PETN[31]	A34		
PEX_PERP[31]	D34		
PEX_PERN[31]	E34		

Link polarity inverted

ATCA 2 down-link x1 connector
Hot-plug by IPMC
Signals must be crossed Txd (Switch_Out) <-> RxD (CrossSwitch_In)

Link polarity inverted

ATCA 1 up-link x1 connector
Hot-plug by IPMC
Signals must be crossed Txd (Switch_Out) <-> RxD (CrossSwitch_In)

External PCIe x4 connector
Hot-plug

Link polarity inverted

Line reversal

Link polarity inverted

Link polarity inverted

PCIe from V5
No hot-plug
Signals must be crossed Txd<-> RxD

Place near connector PCIe x4

4/B6	PCIE_P8_PET_0_P	CABLE_PCIE_T0_P	3/D8
4/B5	PCIE_P8_PET_0_N	CABLE_PCIE_T0_N	3/E8
4/B6	PCIE_P8_PET_1_P	CABLE_PCIE_T1_P	3/E8
4/B6	PCIE_P8_PET_1_N	CABLE_PCIE_T1_N	3/E8
4/C6	PCIE_P8_PET_2_P	CABLE_PCIE_T2_P	3/E8
4/C6	PCIE_P8_PET_2_N	CABLE_PCIE_T2_N	3/E8
4/C6	PCIE_P8_PET_3_P	CABLE_PCIE_T3_P	3/E8
4/C6	PCIE_P8_PET_3_N	CABLE_PCIE_T3_N	3/E8

100NF C600 C601 C602 C603 C595 C596 C597 C598

Place near Virtex V5 (less than 1/3

4/D6	PCIE_P11_PET_0_P	V5_PCIE1_RXP	
4/D6	PCIE_P11_PET_0_N	V5_PCIE1_RXN	
4/D6	PCIE_P11_PER_0_P	V5_PCIE1_TXP	
4/D6	PCIE_P11_PER_0_N	V5_PCIE1_TXN	

100NF C64 C65 C66 C67

PCIE_+3V3_IO

R129	150R	V41	ATT.AMC1
R161	150R	V18	ATT.CABLE
R128	150R	V40	ATT.AMC2
R98	150R	V17	ATT.ATCA1
R127	150R	V39	ATT.AMM3
R125	150R	V38	ATT.V5
R121	150R	V34	ATT.PCIE_CON
R123	150R	V36	ATT.ATCA2

3/C1	PCIE_ATN_LED_P3_N
4/C4	PCIE_ATN_LED_P10_N
3/C1	PCIE_ATN_LED_P2_N
4/C4	PCIE_ATN_LED_P9_N
3/C1	PCIE_ATN_LED_P1_N
4/C4	PCIE_ATN_LED_P11_N
3/B1	PCIE_ATN_LED_P0_N
3/B1	PCIE_ATN_LED_P8_N

PCIE_+3V3_IO

R255 10K

HP_BUTTON_1

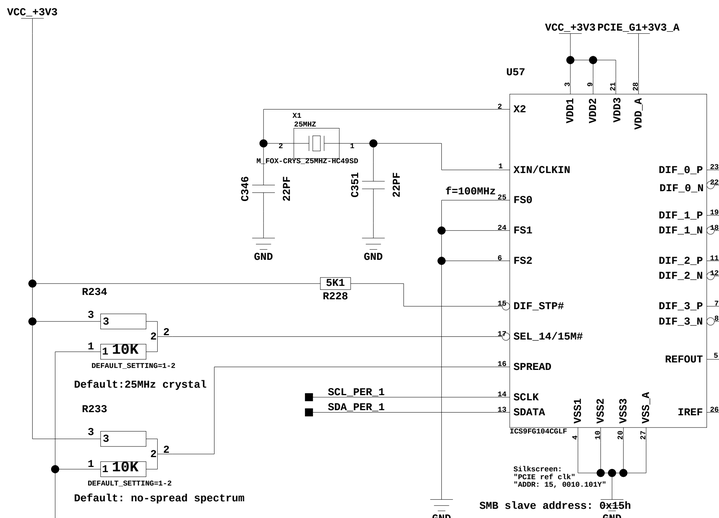
SW4

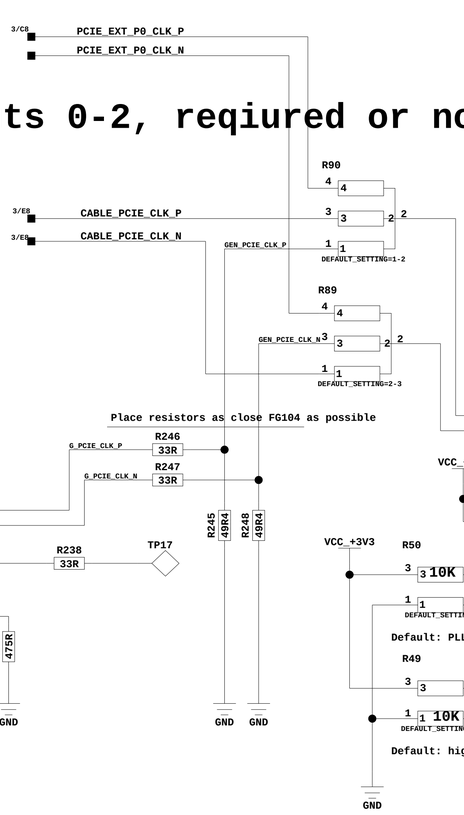
GND

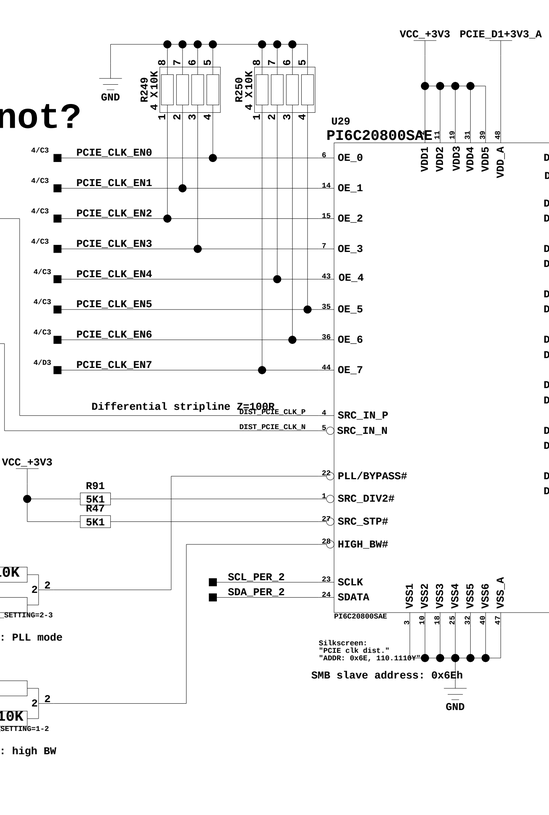
Engineer	DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3 / Rev: 0
Drawn by:	DARIUSZ MAKOWSKI	Title: PCIE I/O #2	Sheet:4 of 8
Changed by:	DARIUSZ MAKOWSKI		
Date Changed:	10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>

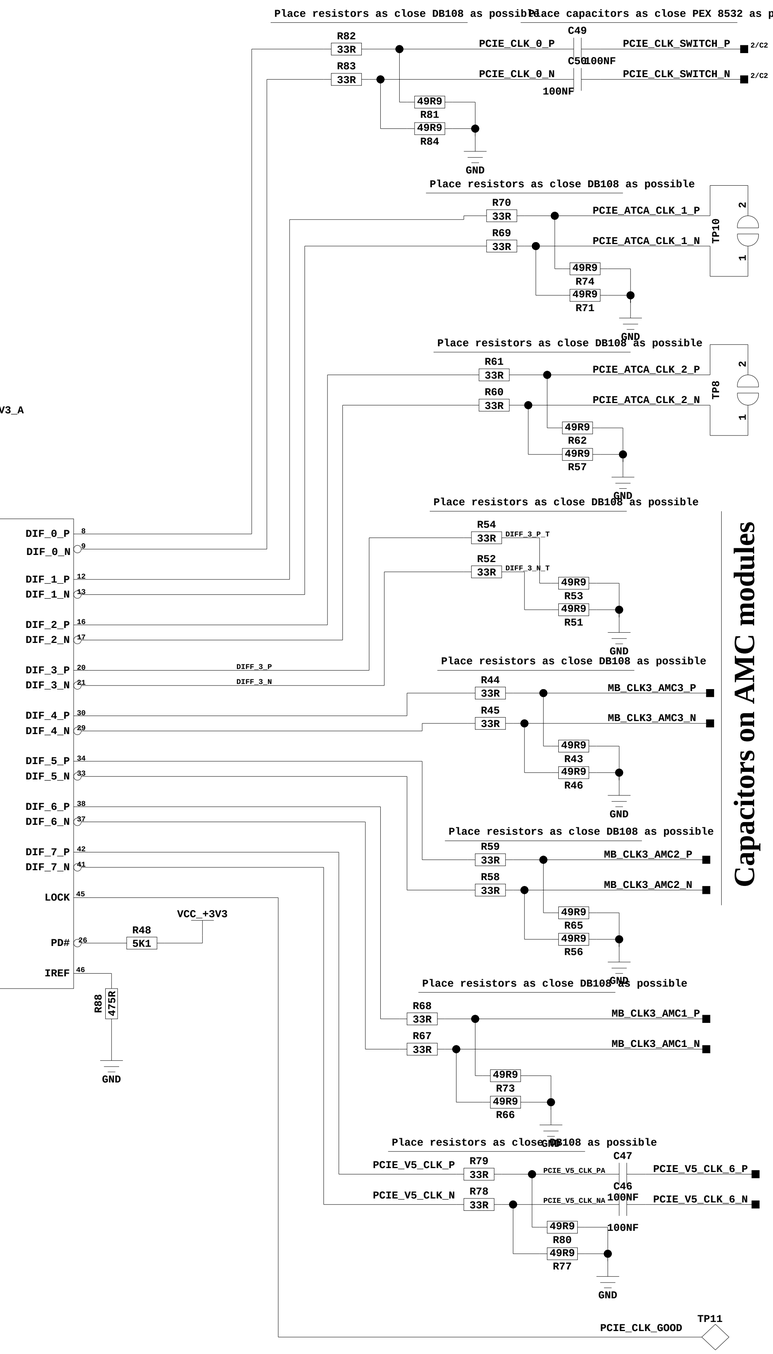
PCIE clock reference and distribution, f=100 MHz

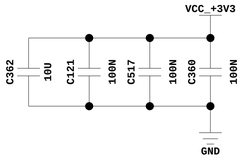
Check termination of outputs 0-2, reqiured or not?

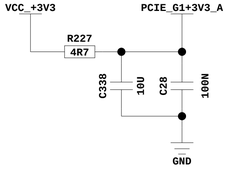


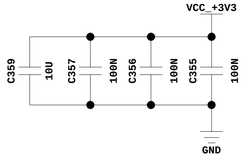


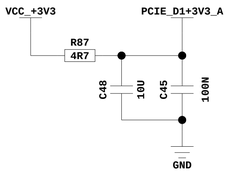








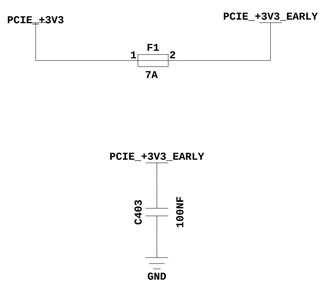


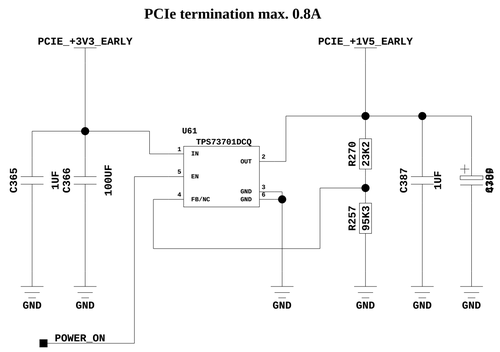


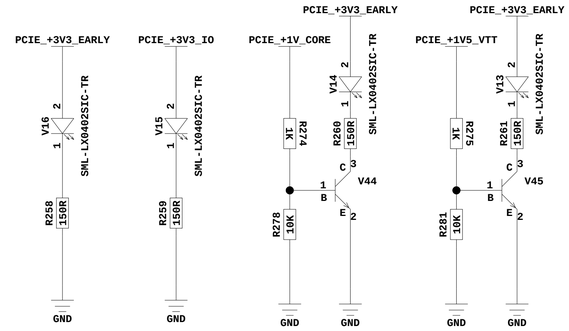
Capacitors on AMC modules

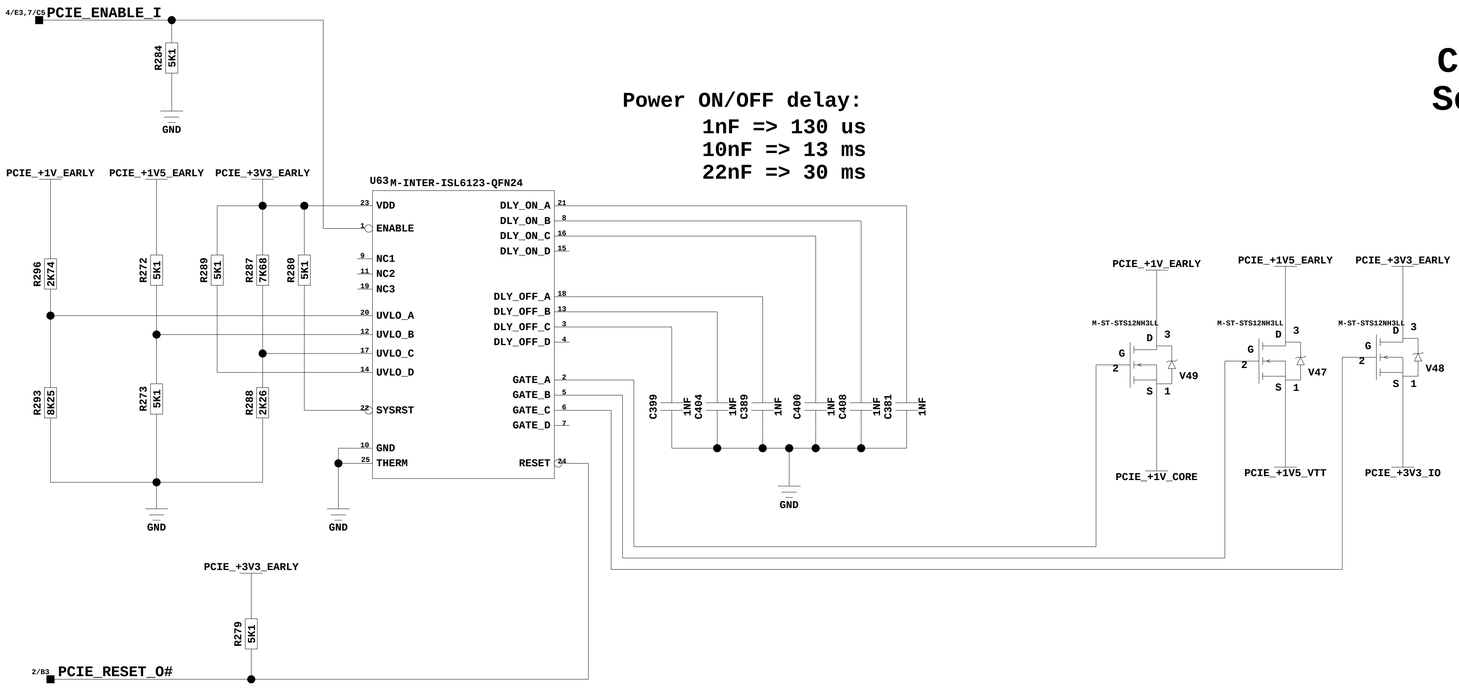
Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 5 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE REFERENCE CLOCK		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

PCIe switch power supply and power sequencer







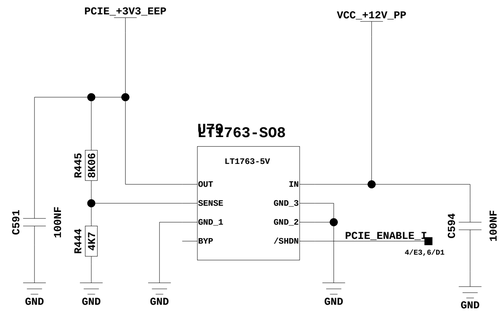


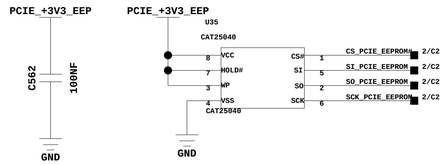
Power supply consumprion:

IO supply current (3V3) : max. 0.001 A
Core supply current (1V): max. 6 A (typical 5 A)
SerDes termination supply current (1V5): max. 0.84

Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 6 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE POWER SEQUENCER AND POWER SUPPLY #2		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

Configuration EEPROM for PCIe switch, default Vcc=3V3





SPI configuration EEPROM 256 kb (7.8MHz@3V3), 5mA@5V or config + extra ROM SPI EEPROM 512 kb

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 7 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE CONFIGURATION EEPROM		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

To DO

Bus betweem FPGA (spartan)

Improve package of PowerConverter and its caps (pads)

Connect LEDS

Tune and improve PCIe nets

Caps for PEX8532

Use termination resistors R=100R +/- 10% when all ports are not implemented, Rx1-Rx3

ALL PCIe receivers must be AC coupled on the receiver chip (100nF 1%)

PCIe signals on port 0

Remarks for VCS3312:

Input and Output Signals Invertion supported, simplifies PCB

Support for Loss of Signal on inputs

VDDio = 2V5/3V3, Vcore = 2V5

Requirements for PCIe routing:

Match signals in a single lane up to 5mil (carrier and AMC)

Maximum length of PCIe trace is 381mm on carrier and 76mm on AMC

Main logic and Xilinx IO/3.3V power supply 10A/3V3

configuration EEPROM 256 kb (7.8MHz@3V3), 5mA@5V

config + extra ROM SPI EEPROM 512 kb

lk variations +/- 300 ppm

SSC must be turn on/off

e matched within 15" (whole board, point-to-point)

r on planes or traces wider than 100 mils

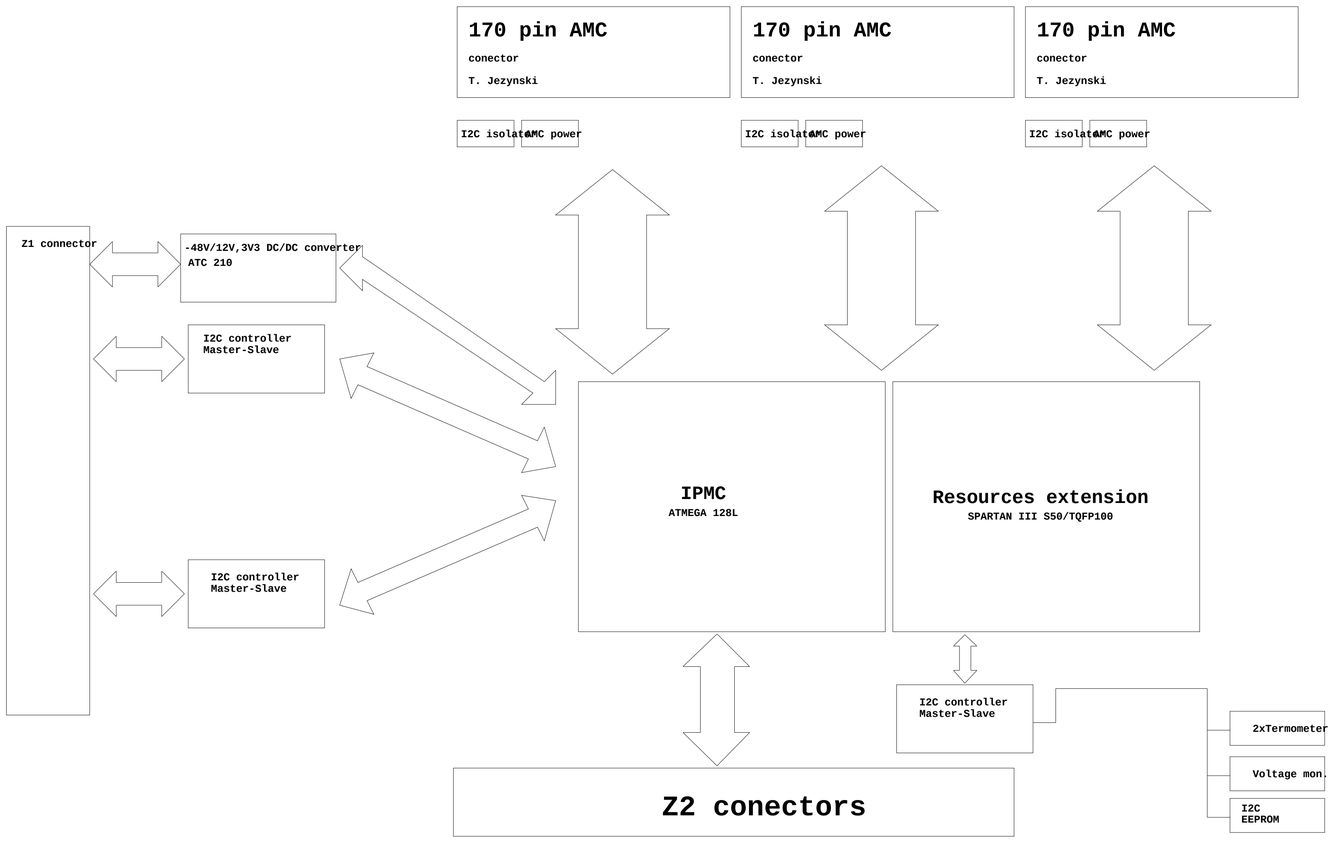
-parallel termination at the clk source

rs 0402 no TxD lane as close as possible on single lane

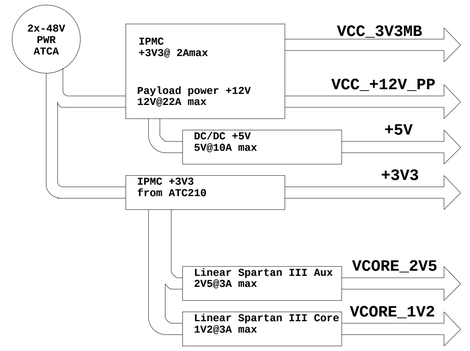
to connector (TxD lane), or receiver chip (RxD) (chip-to-chip lane) - always simulate

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 8 of 8	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE PCB ROUTING NOTES		
Changed by: DARIUSZ MAKOWSKI			
Date changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

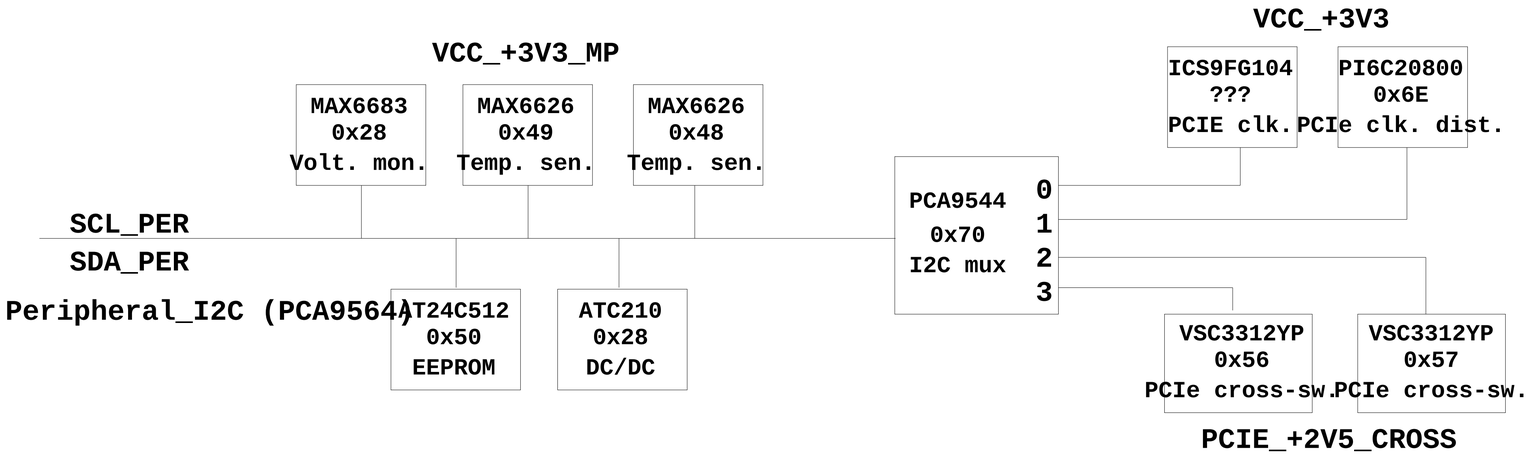
IPMC block diagram



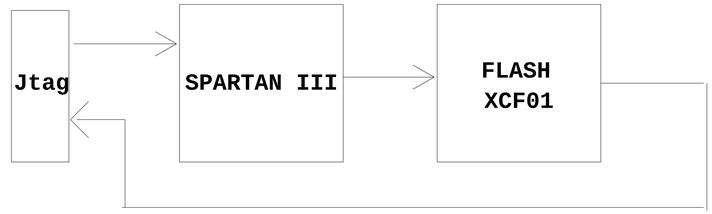
Power Supply



Map of devices on I2C peripheral bus



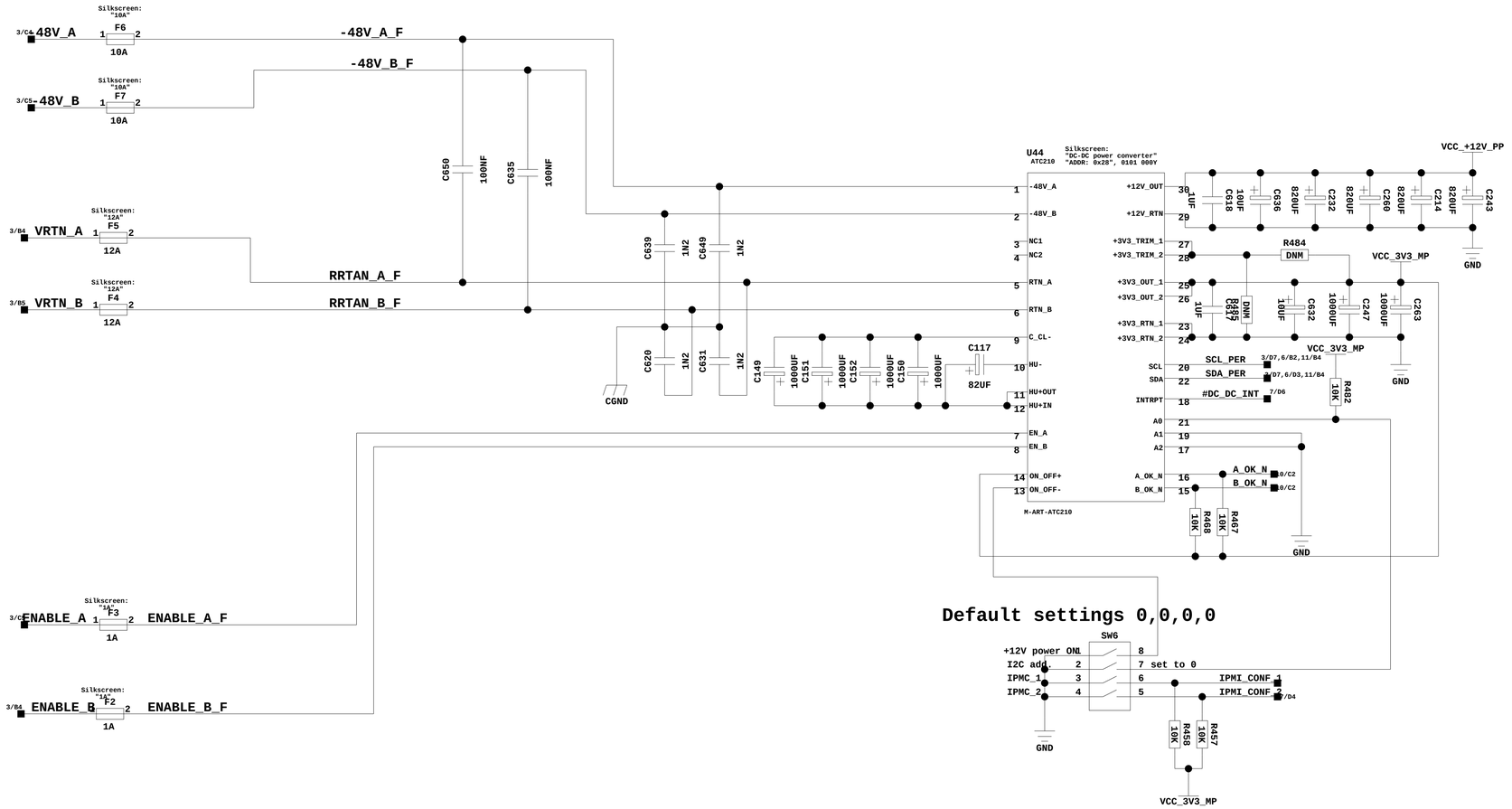
Jtag chain for IPMC FPGA



Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: IPMC BLOCK DIAGRAM		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

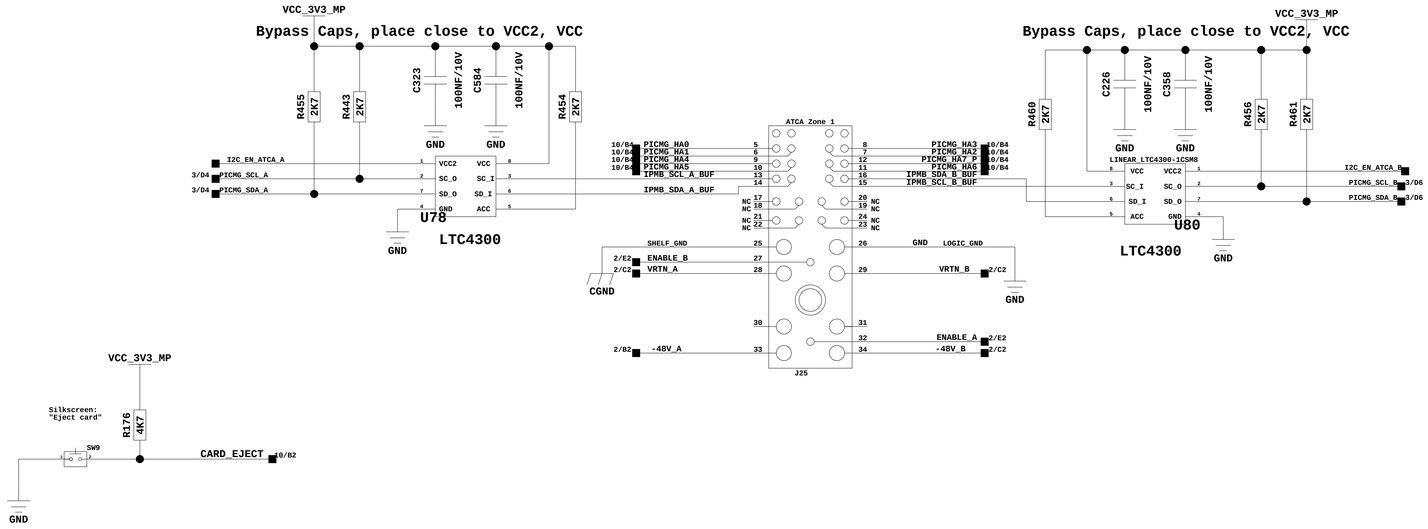
Main power converter DC/DC -48V/VCC_12V_PP VCC_3V3_MP

,superflink,451,Nanofuse,7/1A, RS: 843-453, 541-3388
MD,superflink,451,Nanofuse,10A, RS: 843-469

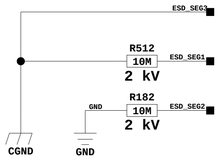


Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 2 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: MAIN POWER CONVERTER		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

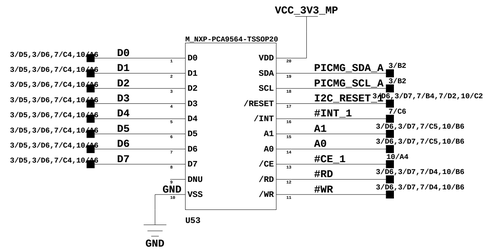
Z1 ATCA connector, 2x I2C



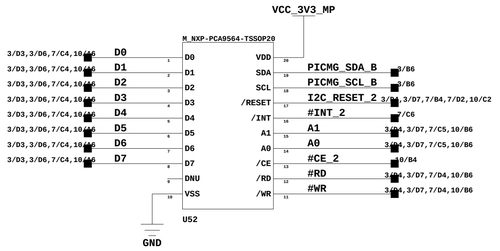
ESD discharge circuit



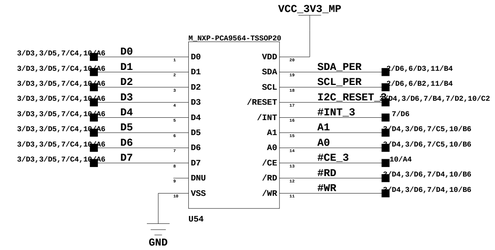
ATCA_I2C_#1



ATCA_I2C_#2



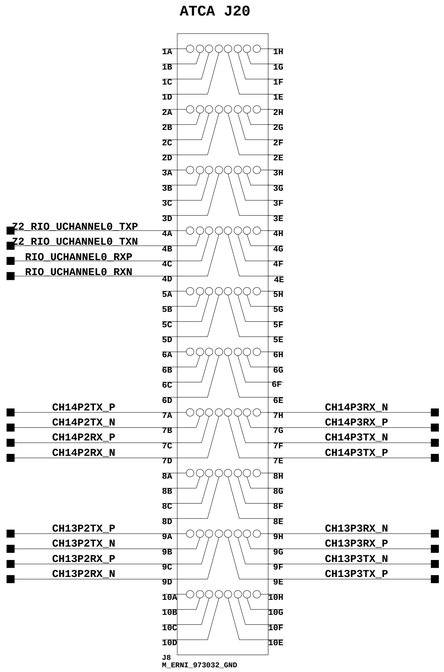
Peripheral_I2C

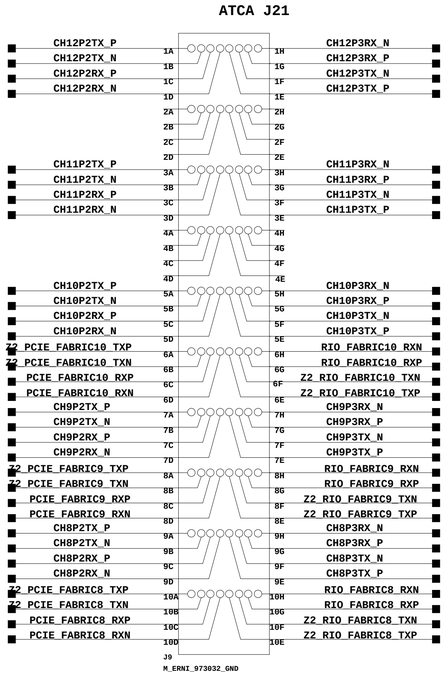


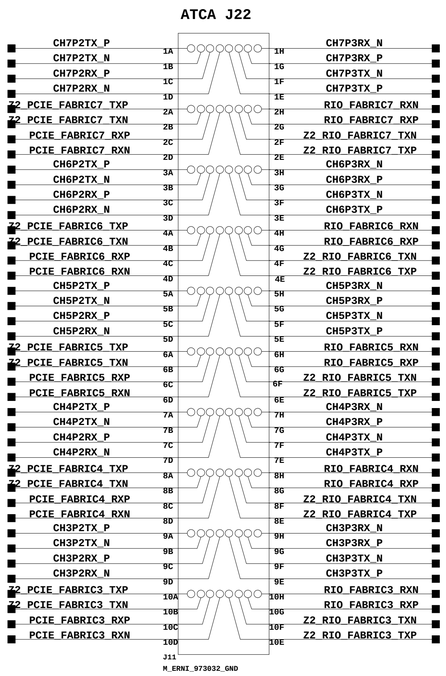
Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 3 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: ATCA ZONE 1 CONNECOR AND I2C EXP. Zone 1 connector		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

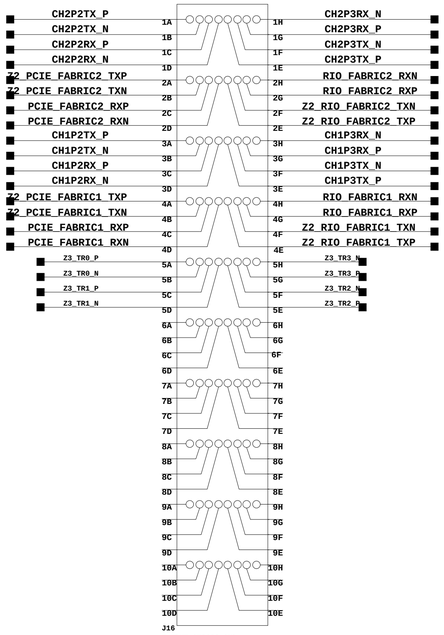
Zone 2 connectors

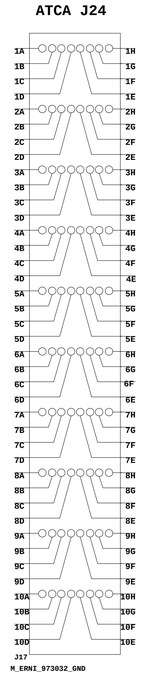
Port 2	Port 3	Row n
Port 0 PCIe (Tx/Rx)	Port 1 RIO (Tx/Rx)	Row n+1
ab	cd	ef











Use termination resistors R=100R +/- 10% when all ports are not implemented, Rx1-Rx3

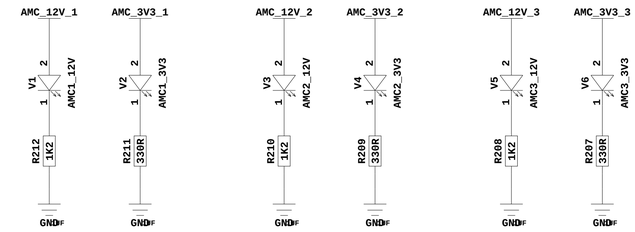
ALL PCIe receivers must be AC coupled on the receiver (transmitter) chip (100nF 1%)

PCIe signals on port 0 / RIO on port 1 and JP20.4

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 4 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: ZONE 2 CONNECTORS		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

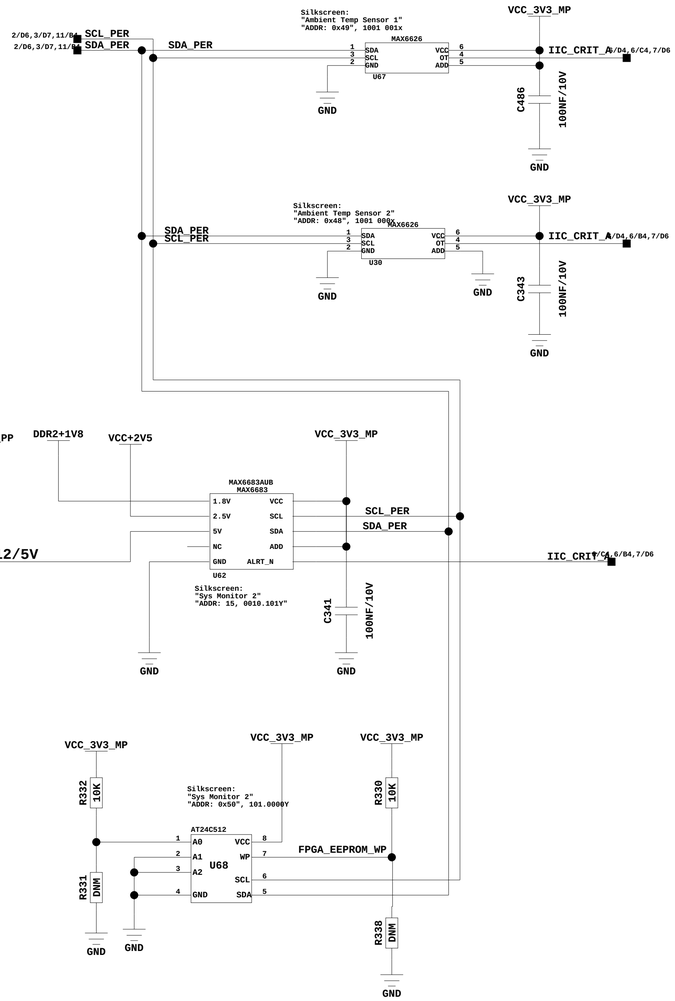
Power management for AMC modules

Route 6 mR resistor with 4 Kelvin connectors



Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 5 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: AMC POWER SUPPLY		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

IPMI monitoring



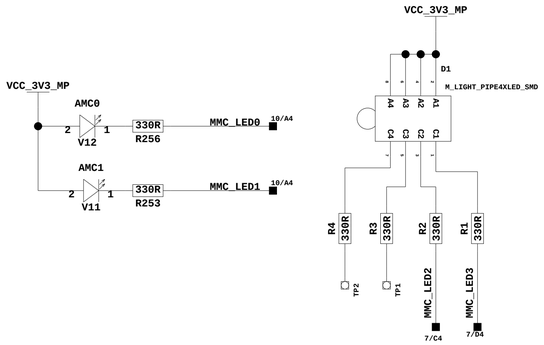
Map of I2C devices

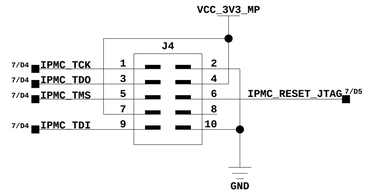
IC	REF	DESCRIPTION	IIC Bus ADDR
ATC210	U30	DC/DC power converter	0x28
MAX6626	U45	Ambient Temp 1	0x49
MAX6626	U44	Ambient Temp 2	0x48
MAX6683	U43	System Monitor (VCC+2V5, 5V, VCC_3V3_MP)	0x15
AT24C512	U42	512 kB EEPROM memory	0x50
ICS9FG104	U60	PCIe clock generator	0x..
PI6C20800SAE	U59	PCIe clock distributor	0x6E
VSC3312YP	U78	PCIe Cross-switch	0x57
VSC3312YP	U80	RIO Cross-switch	0x56

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 6 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: IPMC ELECTRICAL PARAMETERS MONITORING		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

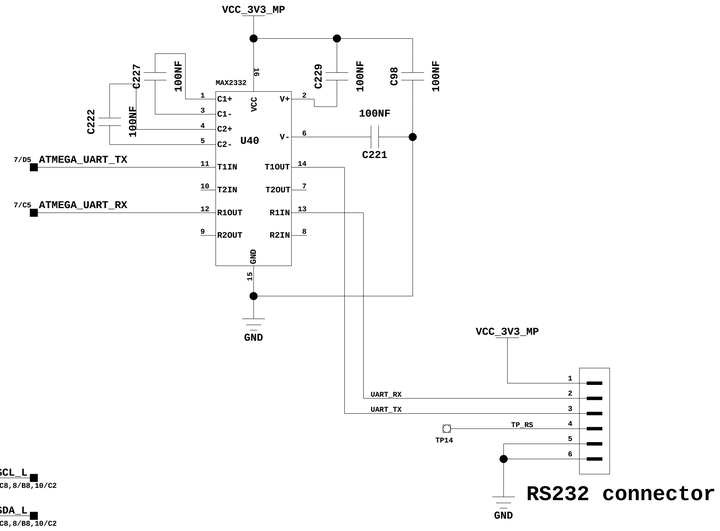
ATCA carrier board management controller IPMC

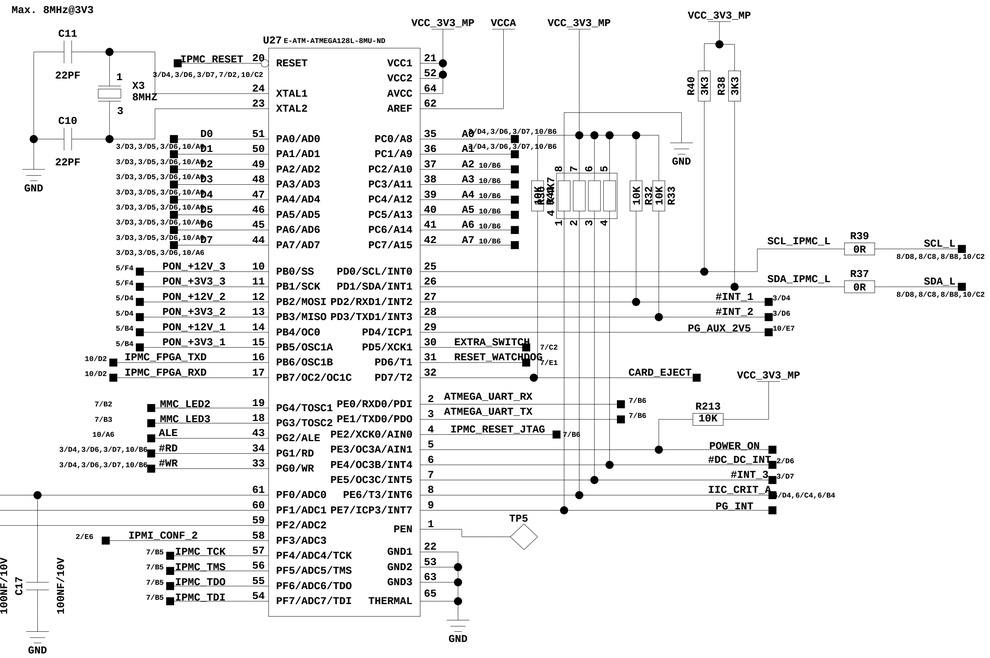
ATCA LEDs





EIA RS232





Watch-dog timeout = 2.5s

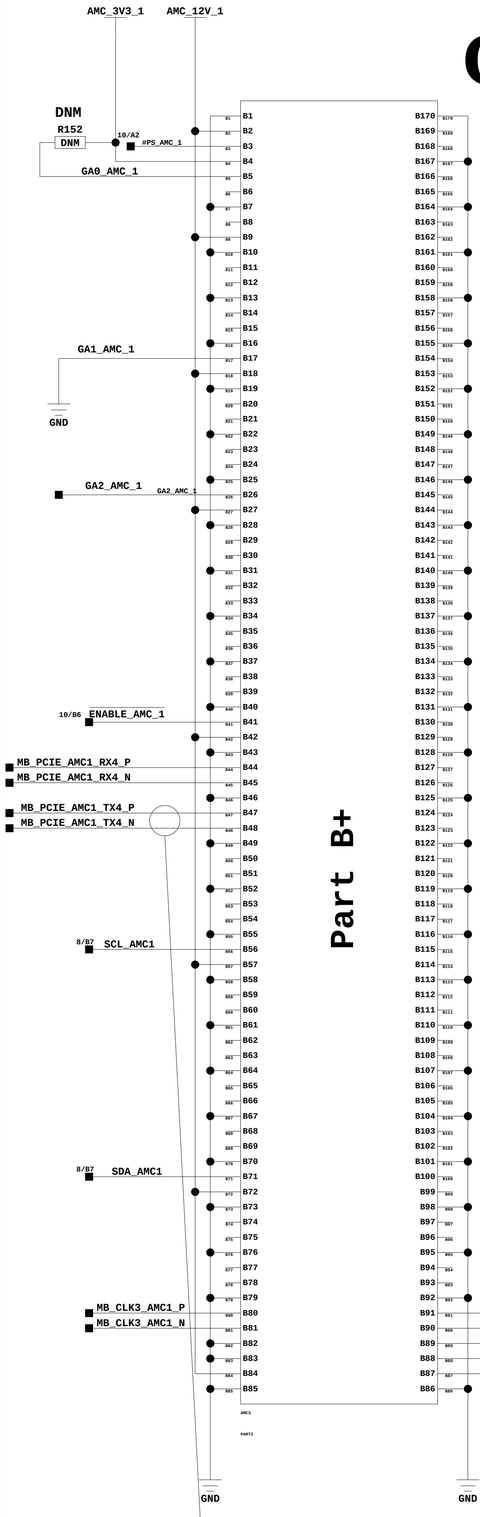
Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 7 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: IPMC CONTROLLER		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

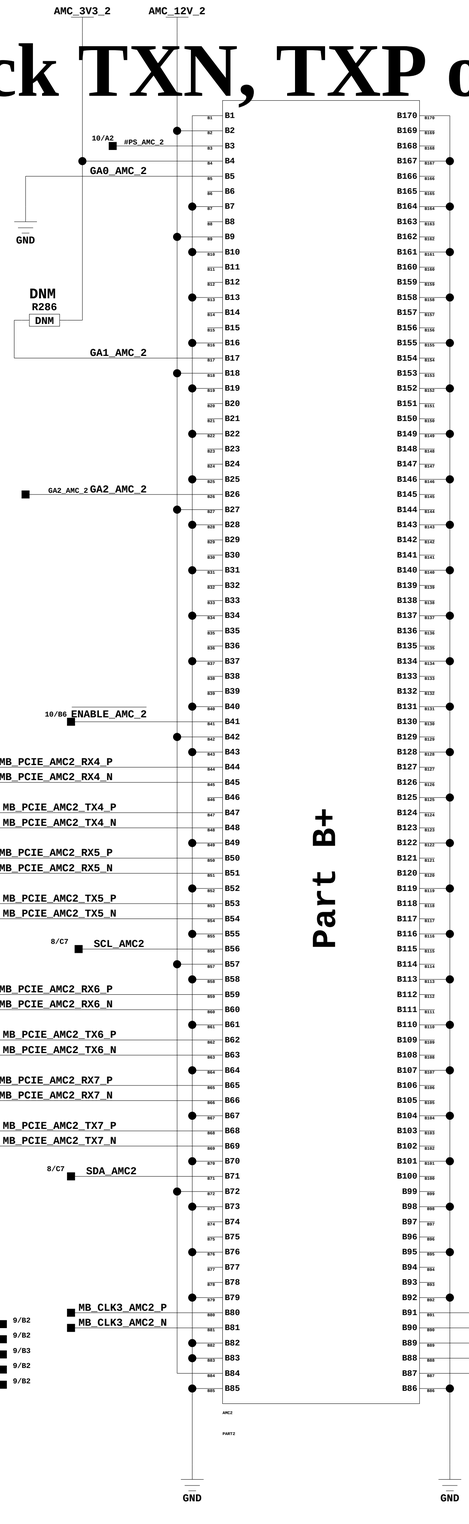
AMC 1, BA: UGU, ga2..ga0

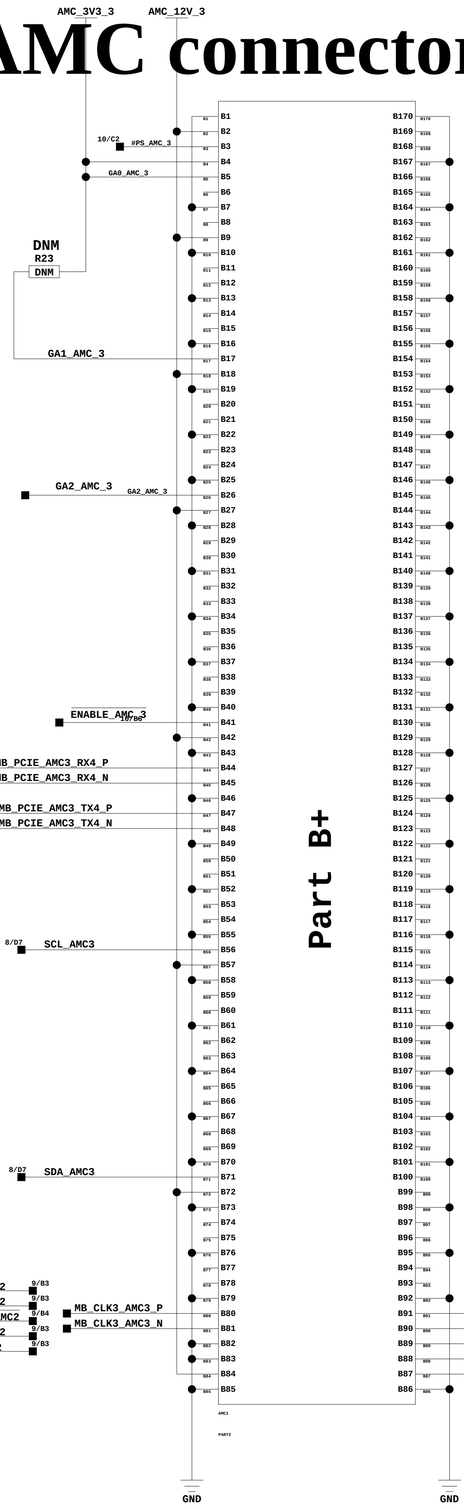
AMC 2, BA: UUG

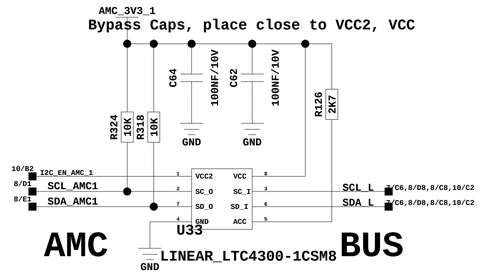
AMC 3, BA: UUP

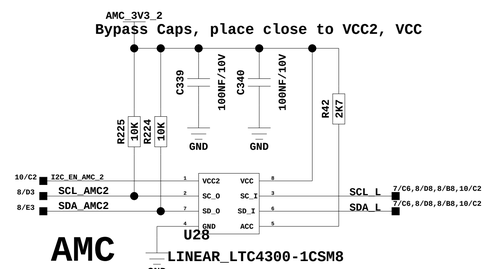
Check TXN, TXP of AMC connectors .....

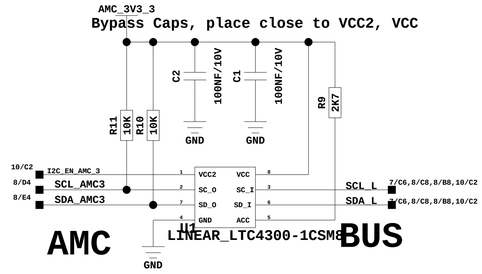








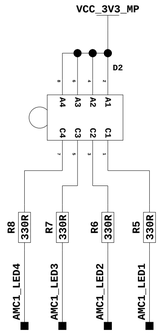


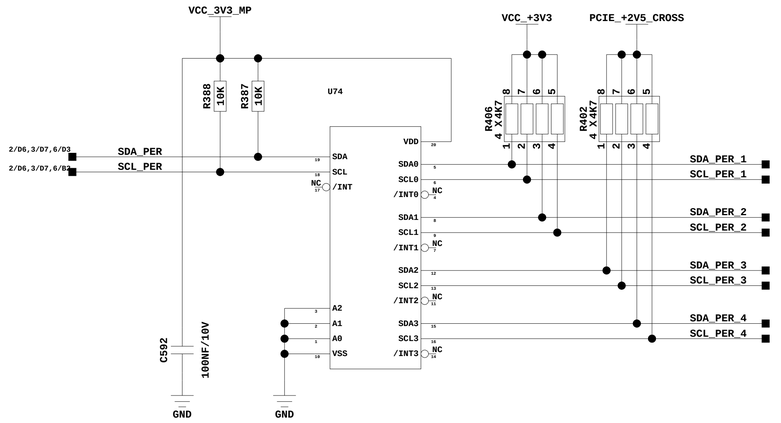


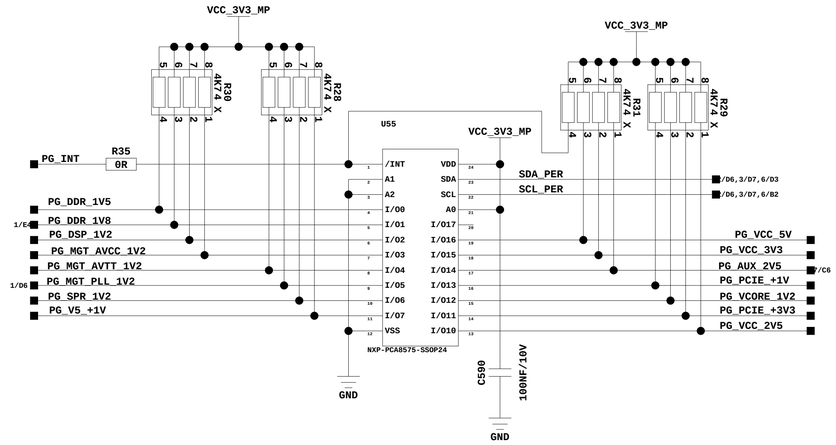
Route differential lines with Z=100R +/-10%

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 8 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: AMC CONNECTORS AND I2C BUFFERS		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

AMC 1 leds

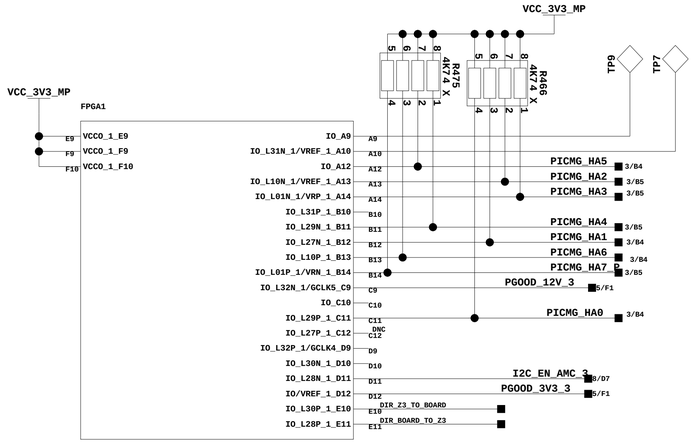


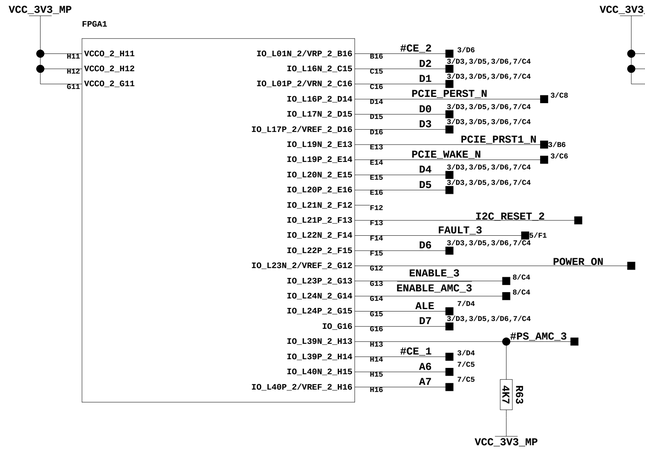


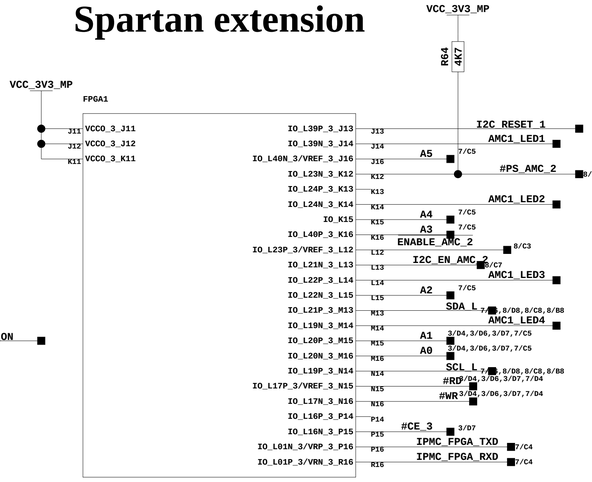


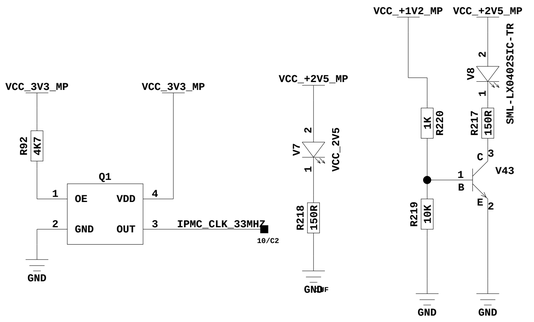
Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 9 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: DIAGNOSTICS LEDS, I2C-BUS EXPANDER		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

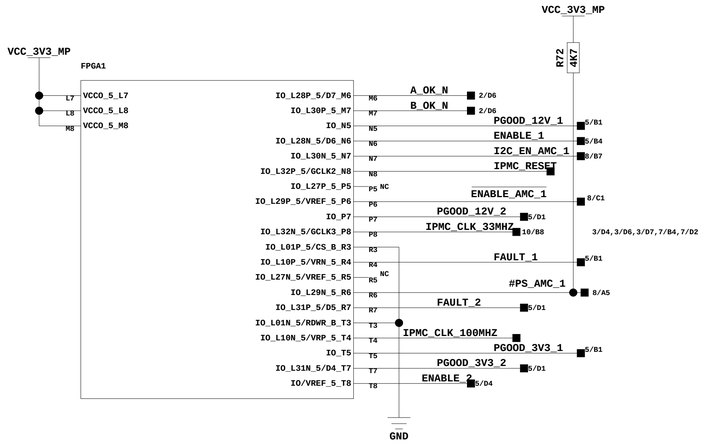
Spartan extension

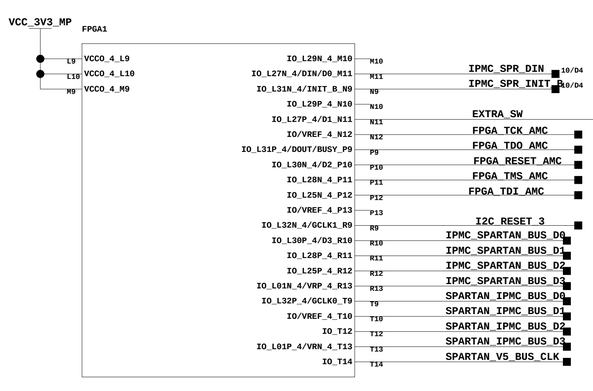


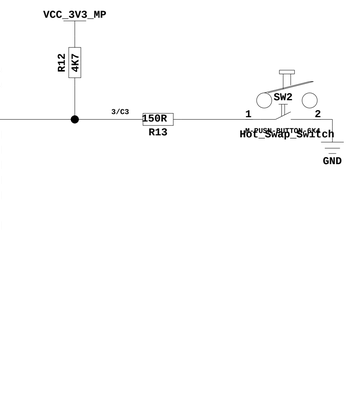


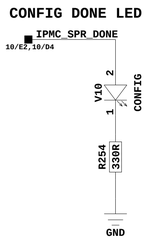


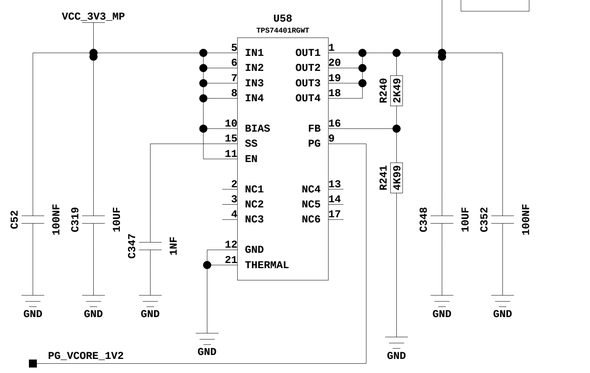




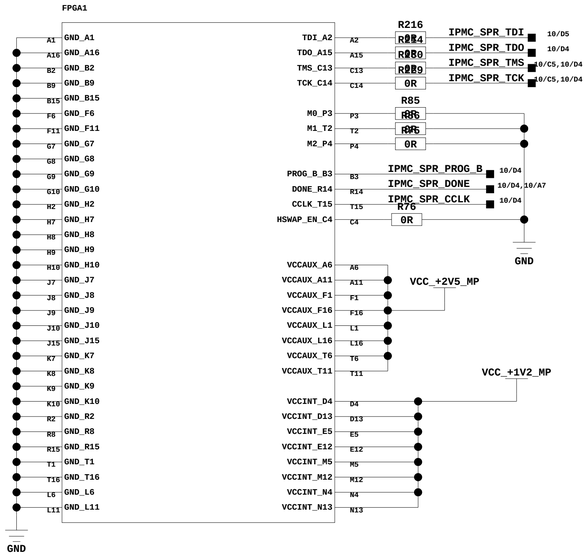


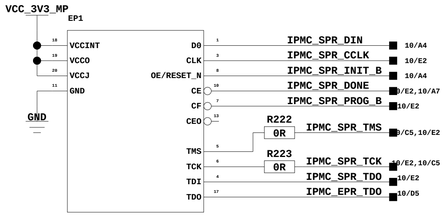


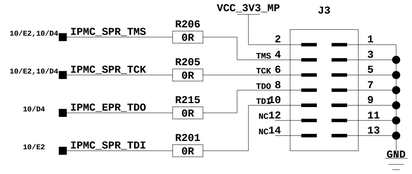




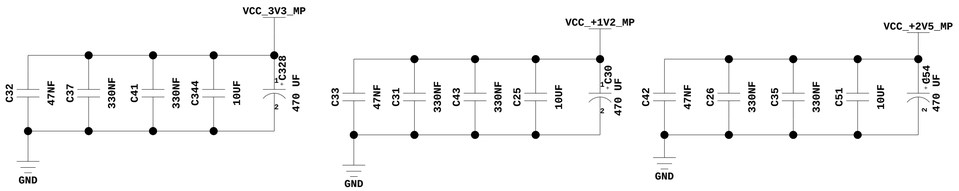
Spartan-3 configuration part

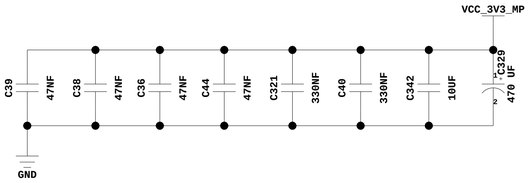


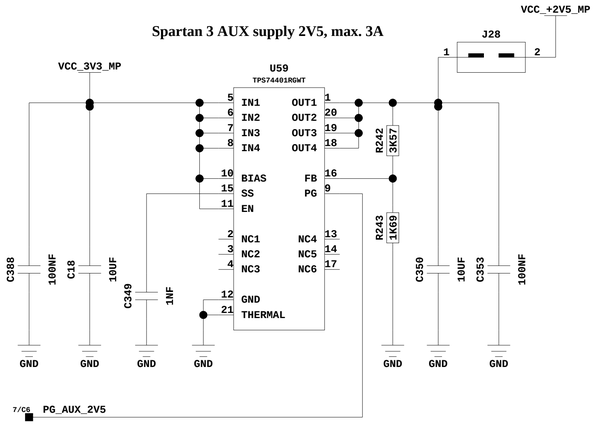




Caps for spartan







Caps for spartan

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet 10 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: IPMC EXPANDER		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

QUESTIONS

These signals are already connected from my side

Still not connected

IPMC_V5_BUS_D0
IPMC_V5_BUS_D1
IPMC_V5_BUS_D2
IPMC_V5_BUS_D3
V5_IPMC_BUS_D0
V5_IPMC_BUS_D1
V5_IPMC_BUS_D2
V5_IPMC_BUS_D3
IPMC_V5_BUS_CLK

Main reset from IPMC

IPMC_RESET_JTAG 7/86

and maybe IPMC reset

IPMC_RESET

To Wojtek's SPARTAN FPGA

IPMC_TCK_AMC1
IPMC_TDO_AMC1
IPMC_TMS_AMC1
IPMC_TDI_AMC1

IPMC_TCK_AMC2
IPMC_TDO_AMC2
IPMC_TMS_AMC2
IPMC_TDI_AMC2

IPMC_TCK_AMC3
IPMC_TDO_AMC3
IPMC_TMS_AMC3
IPMC_TDI_AMC3

FPGA_TCK_AMC
FPGA_TDO_AMC
FPGA_RESET_AMC
FPGA_TMS_AMC
FPGA_TDI_AMC

Jtag connectors from IPMI modules

Check-out list

Check if Wojtec connected PCIe bus to V5

Check if Wojtec connected RIO bus to V5

Check PowerSupply for MGT of V5 (RIO and PCIe)

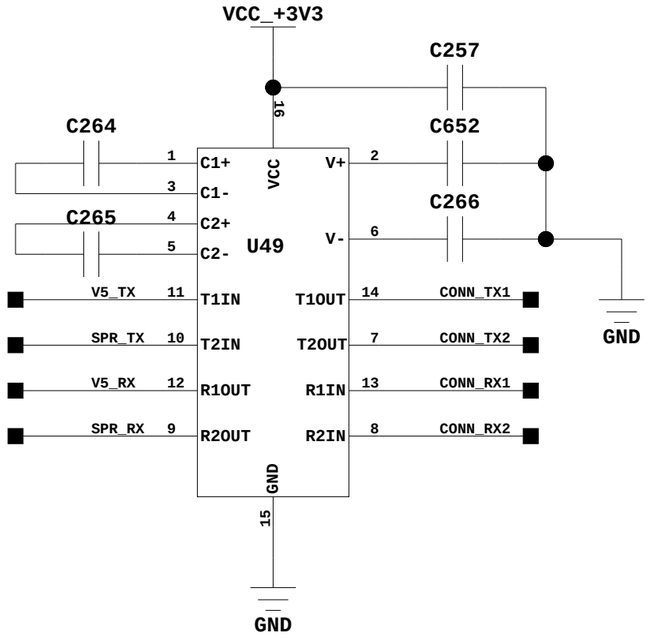
Check PCIe and RIO clk signals for V5

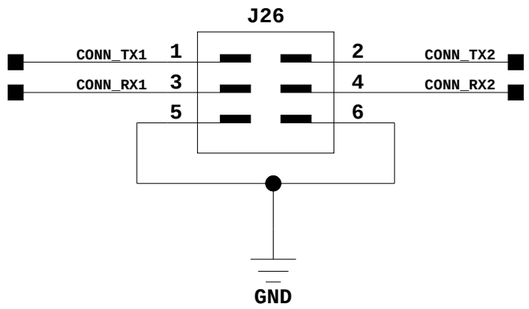
Check PowerSupply converter U88 +2V5

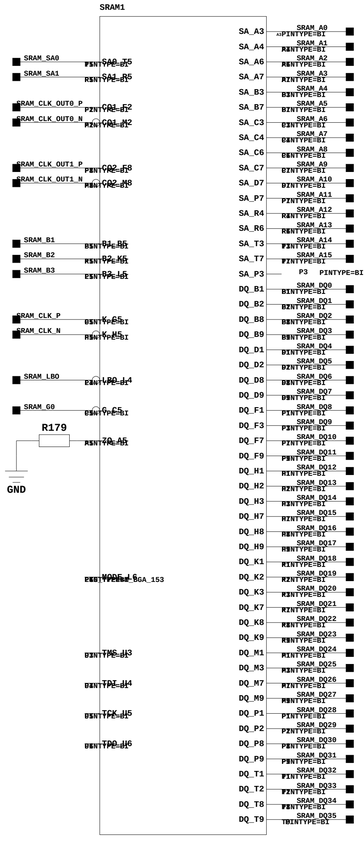
Check JTAG connection to AMC and universal bus to V5

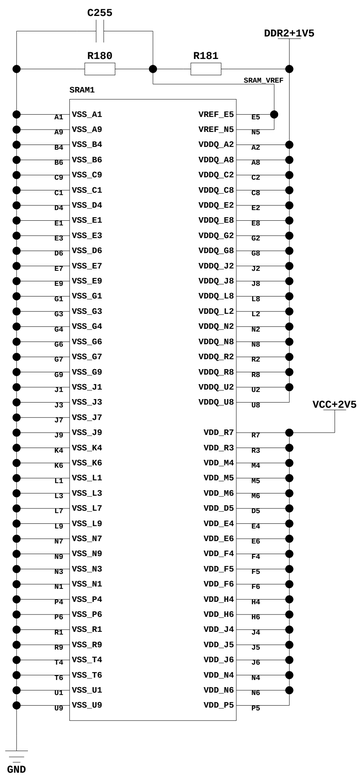
Check JTAG connection to AMC and universal bus to V5

Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet 11 of 11	
Drawn by: DARIUSZ MAKOWSKI	Title: TRASHCAN		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	


VCC_+3V3
C257
C264
C652
C265
C266
U49
VCC
GND
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
V5_TX
SPR_TX
V5_RX
SPR_RX
CONN_TX1
CONN_TX2
CONN_RX1
CONN_RX2
GND


J26
CONN_TX1
CONN_RX1
CONN_TX2
CONN_RX2
GND

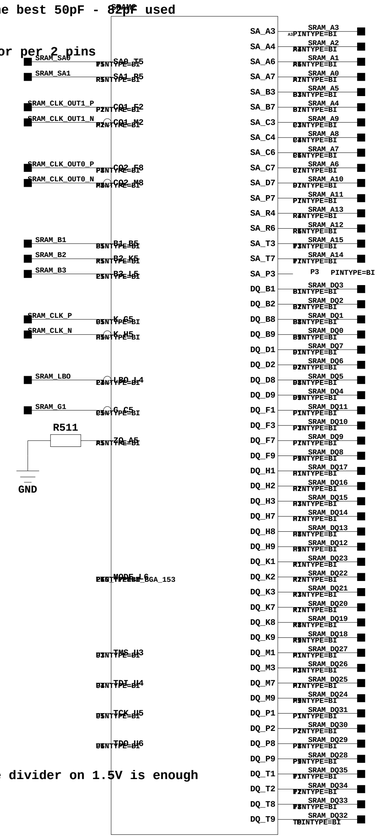


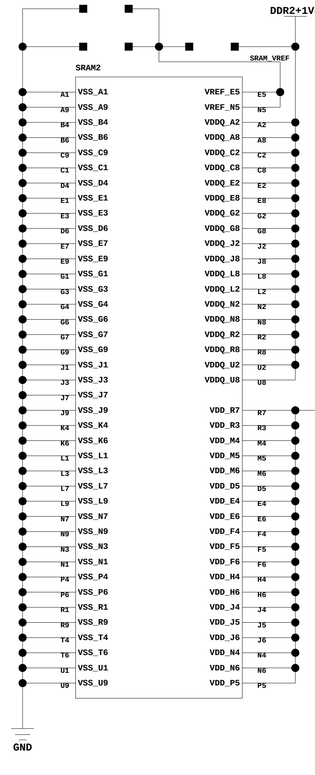


- 50 Ohm ressistors on VRN and VRP pins for that bank

Decoupling capacitors - for around 300MHz - the best 50pF - 22pF used

Number of Capacitors was reduced - one capacitor per 2 pins



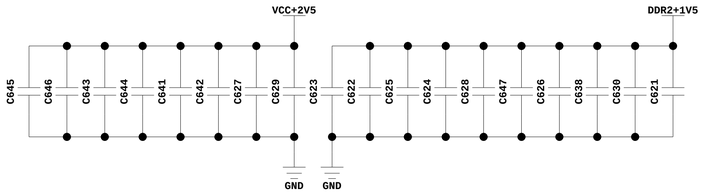


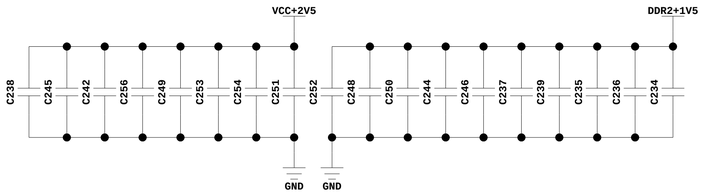
Notes on SRAM:

All ports are HSTL. I requires:

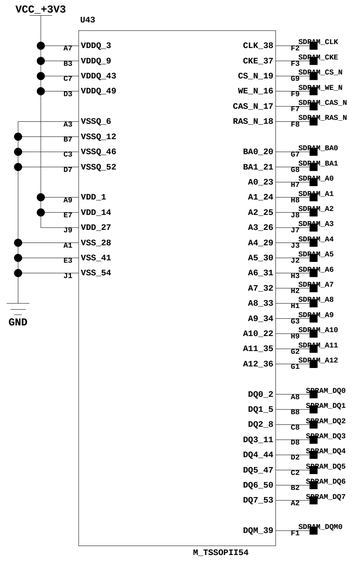
- 0.75 reference voltage on SRAM and Virtex - 10uA so simple divider on 1.5V is enough

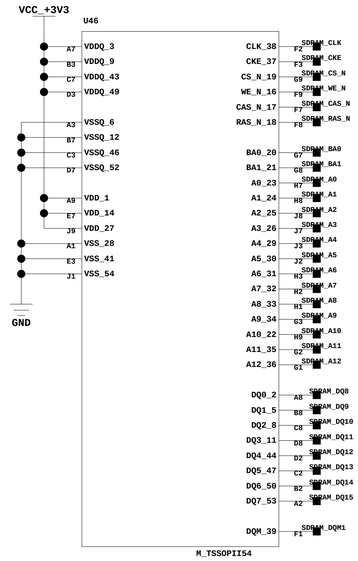
- 1.5 for VCCO on Virtex for that bank

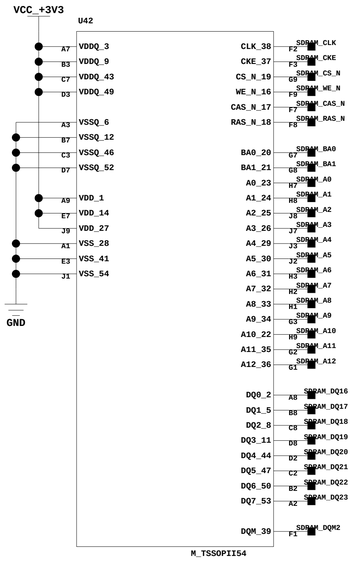


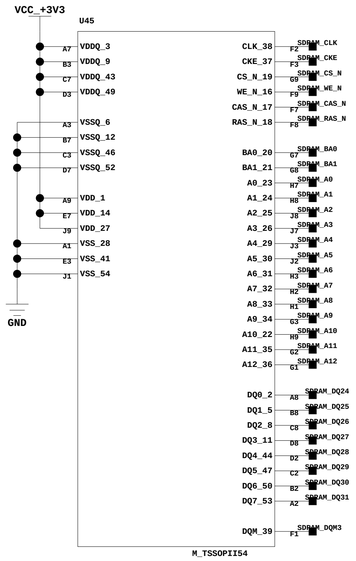


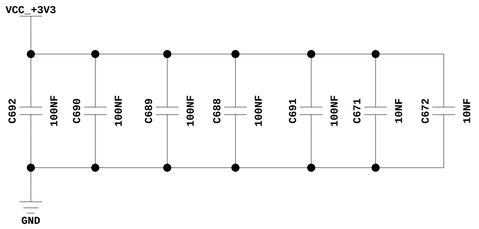
Engineer: WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: QDR SRAM MEMORY		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

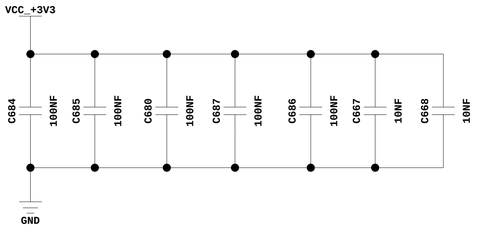


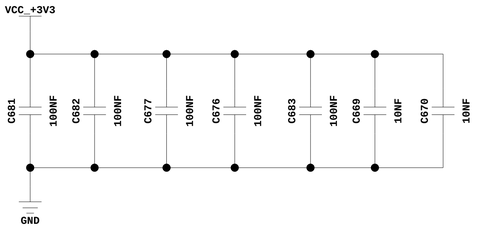


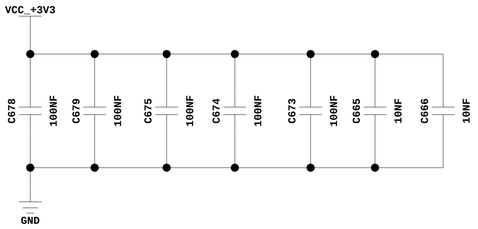




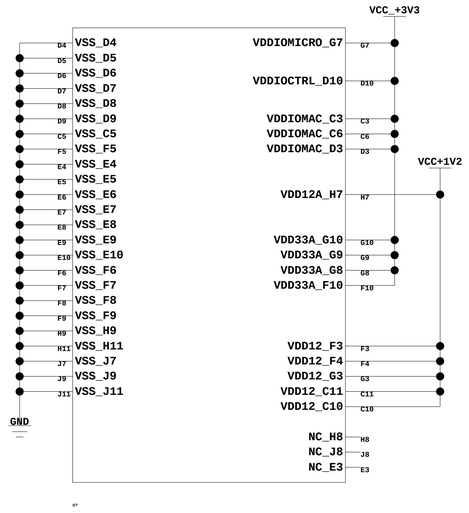


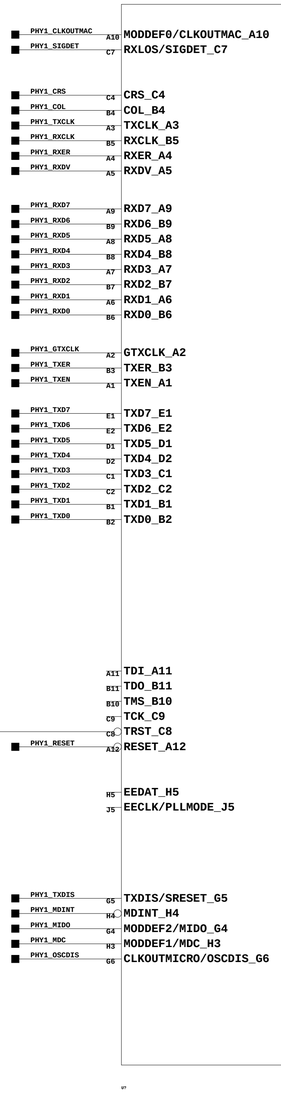


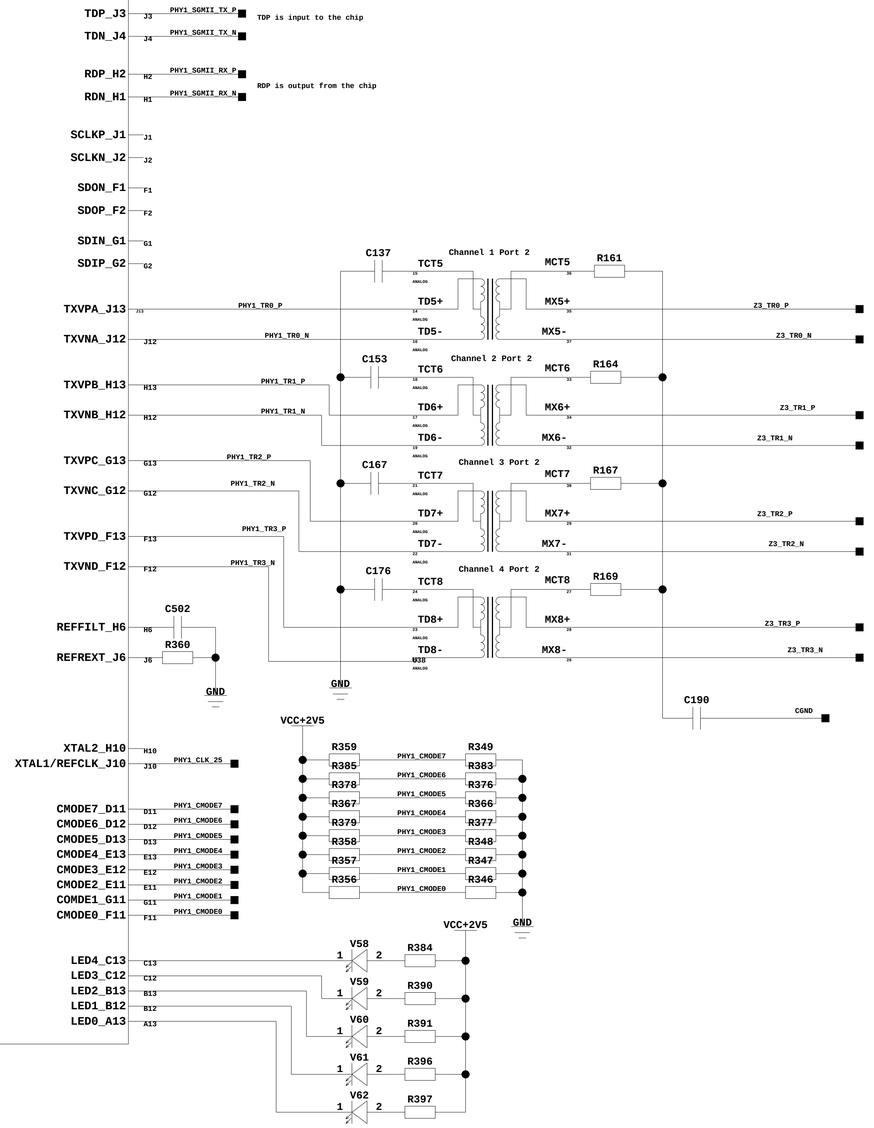


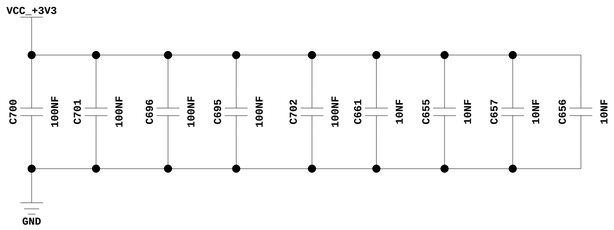


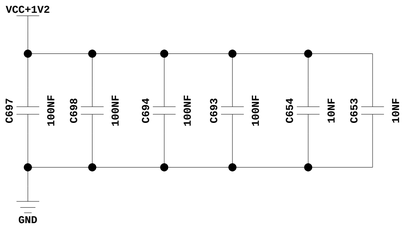
Engineer: WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: SDRAM MEMORY FOR EMBEDDED SYSTEM		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	



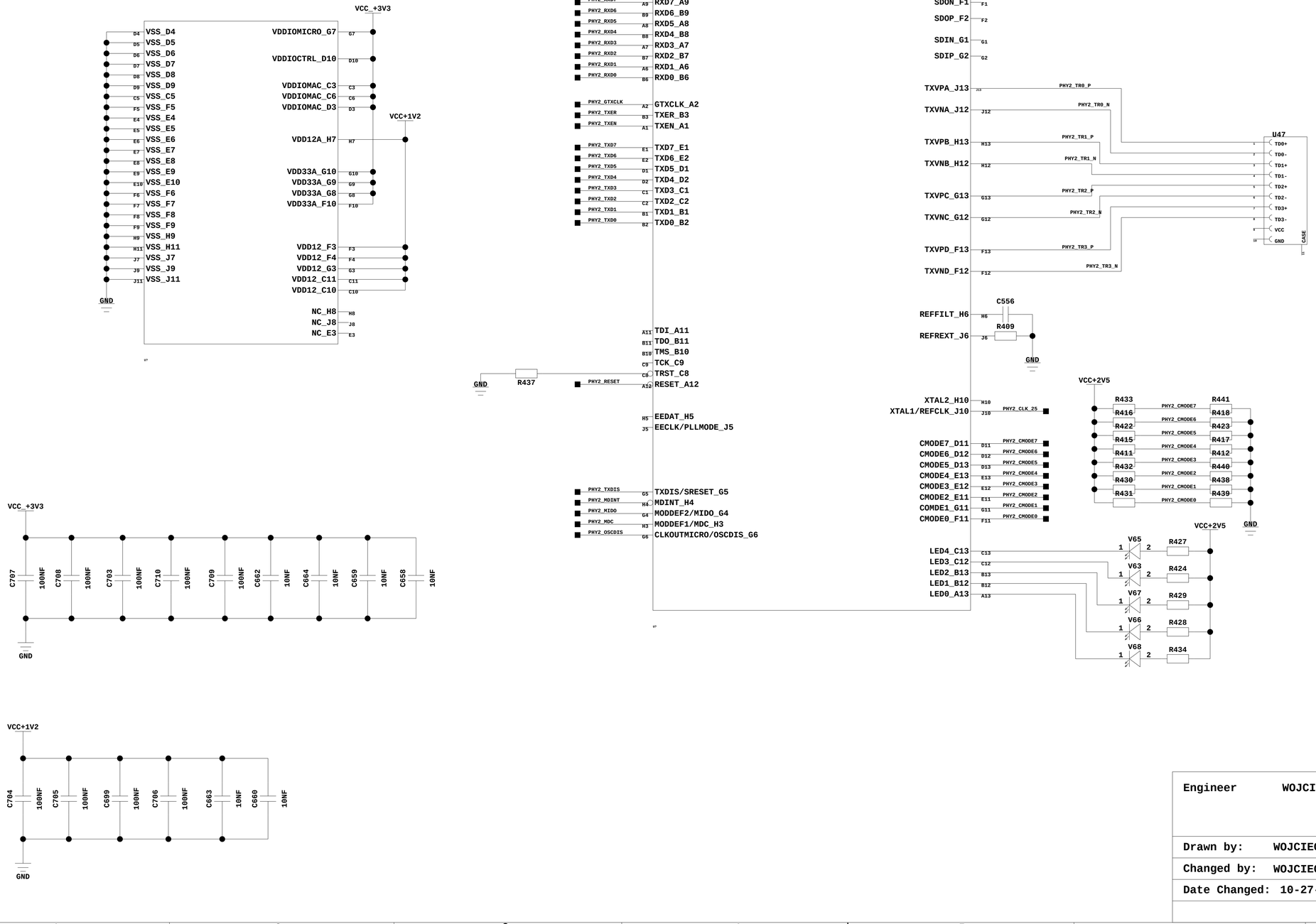








Engineer: WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: QDR SRAM MEMORY		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	



Engineer WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: QDR SRAM MEMORY		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

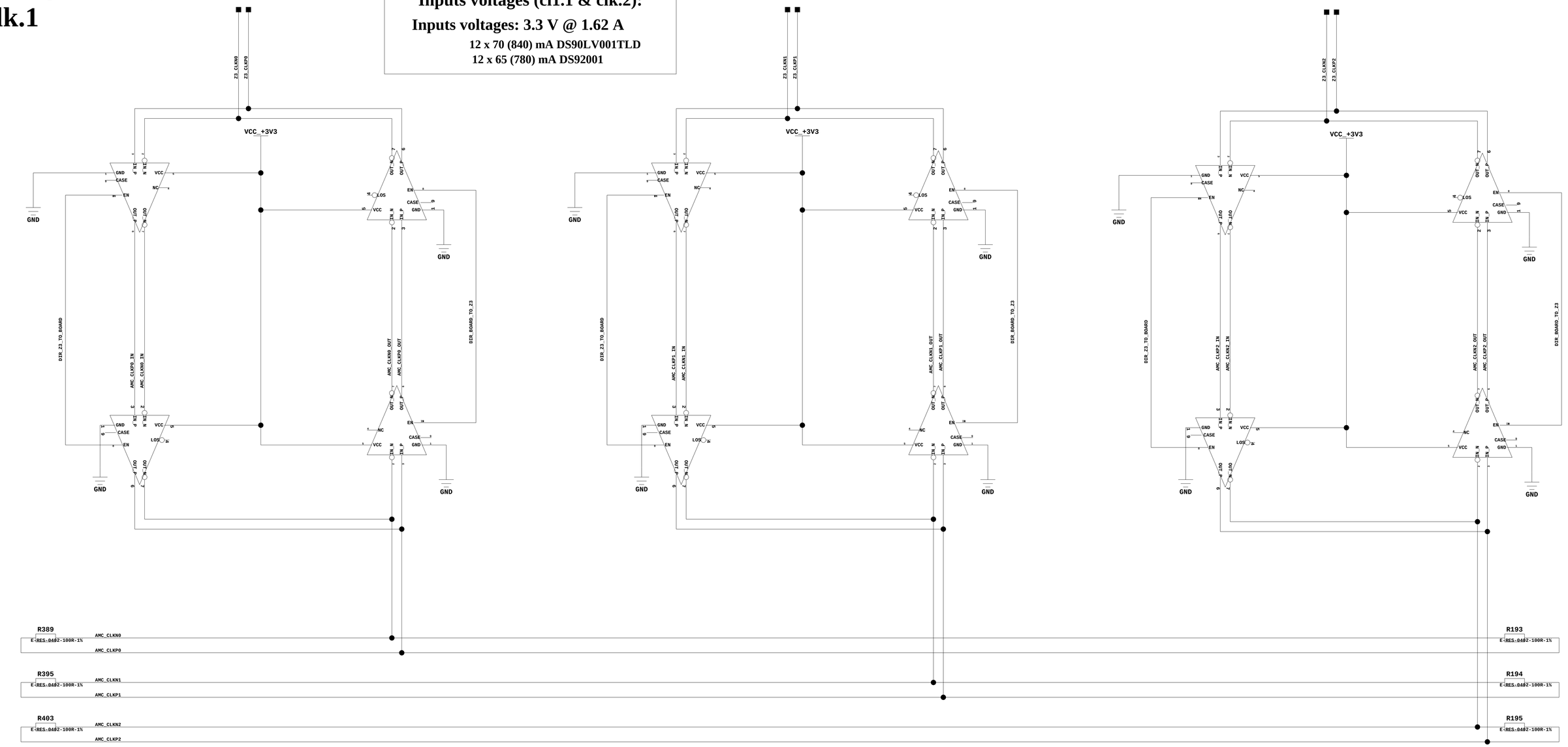
Clock signals (ZONE 3)

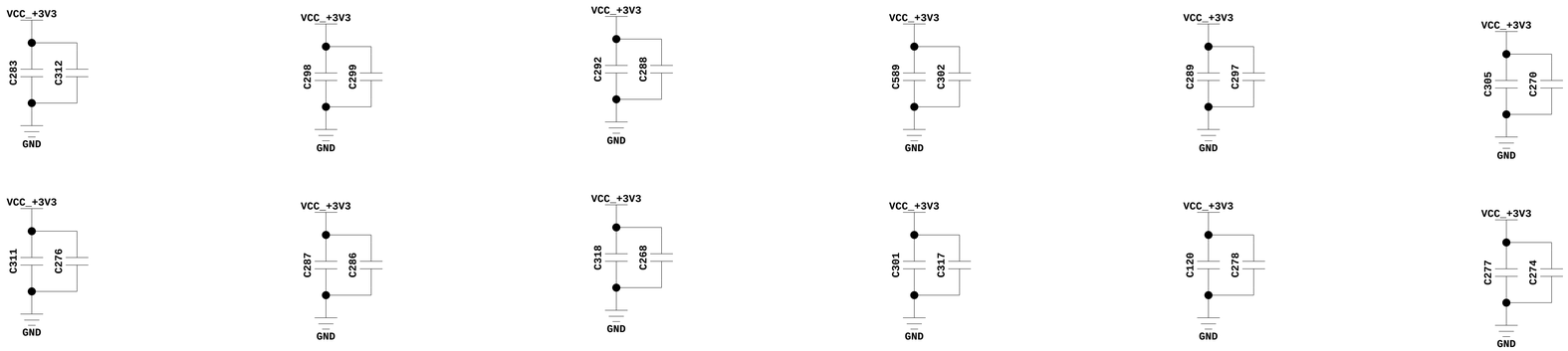
clk.1

Inputs voltages (cl1.1 & clk.2):

Inputs voltages: 3.3 V @ 1.62 A

12 x 70 (840) mA DS90LV001TLD
12 x 65 (780) mA DS92001





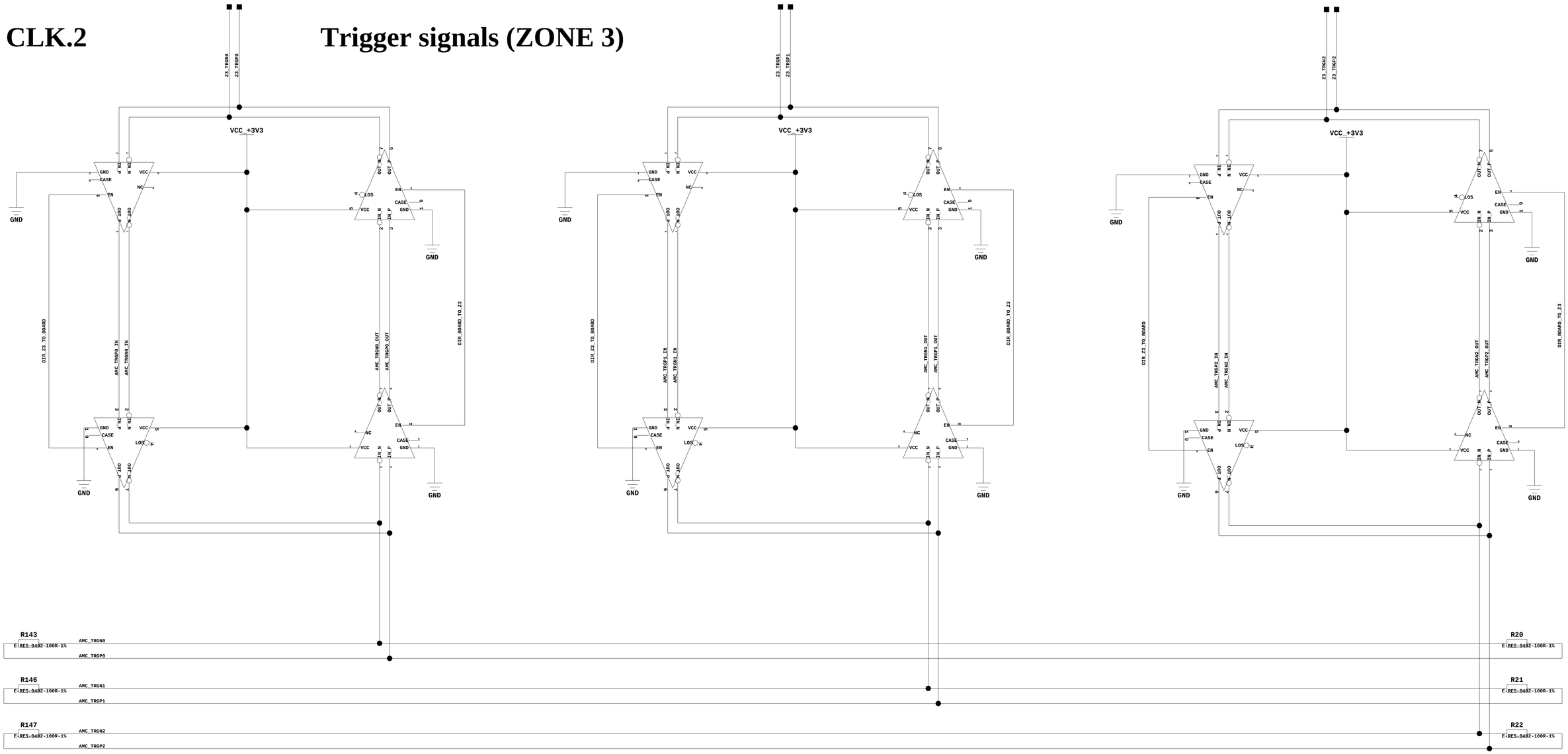
from IPMI or Spartan

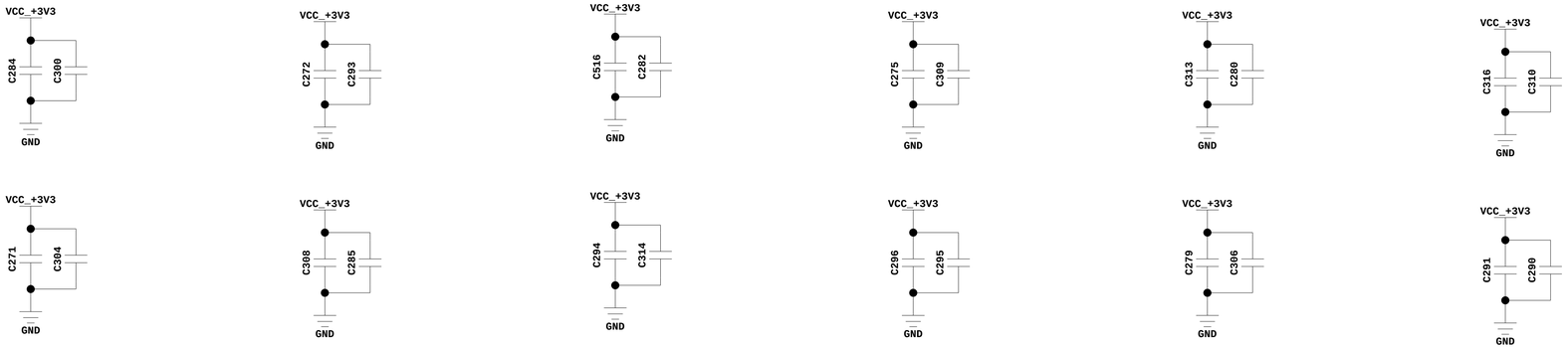
DIR_Z3_TO_BOARD
DIR_BOARD_TO_Z3

Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

CLK.2

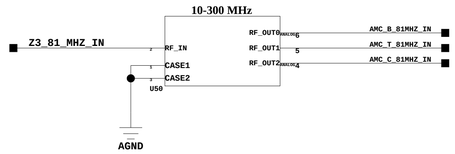
Trigger signals (ZONE 3)

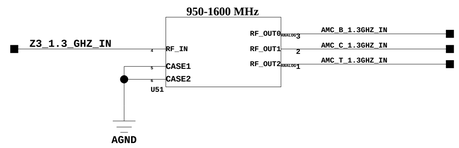




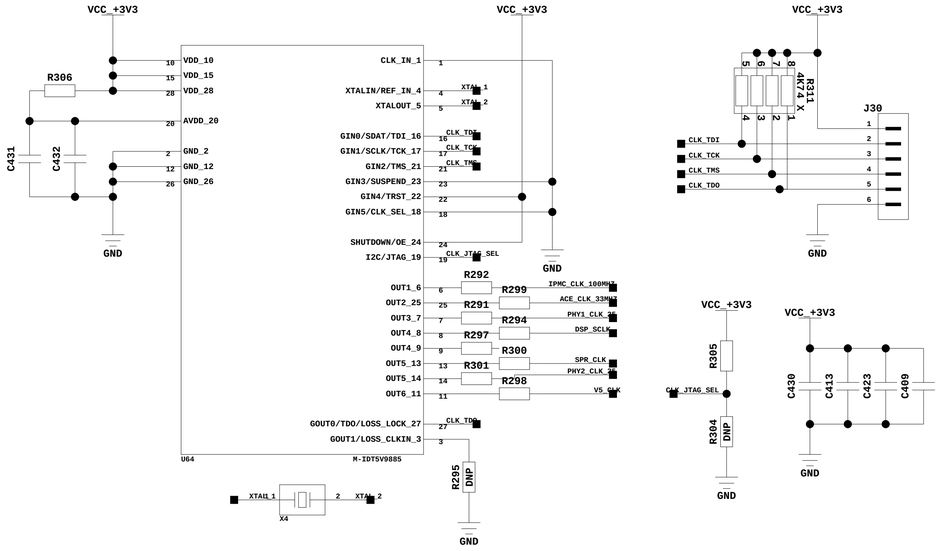
Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

clk.3





Engineer <YOUR NAME HERE>	DESY-<GROUP> Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 1	
Drawn by: <DRAWN BY>	Title: <NAME>		
Changed by: <CHANGED BY>			
Date Changed: 8-21-2006_14:53	Board Nr: <NR>	Drawing Nr: <NR>	

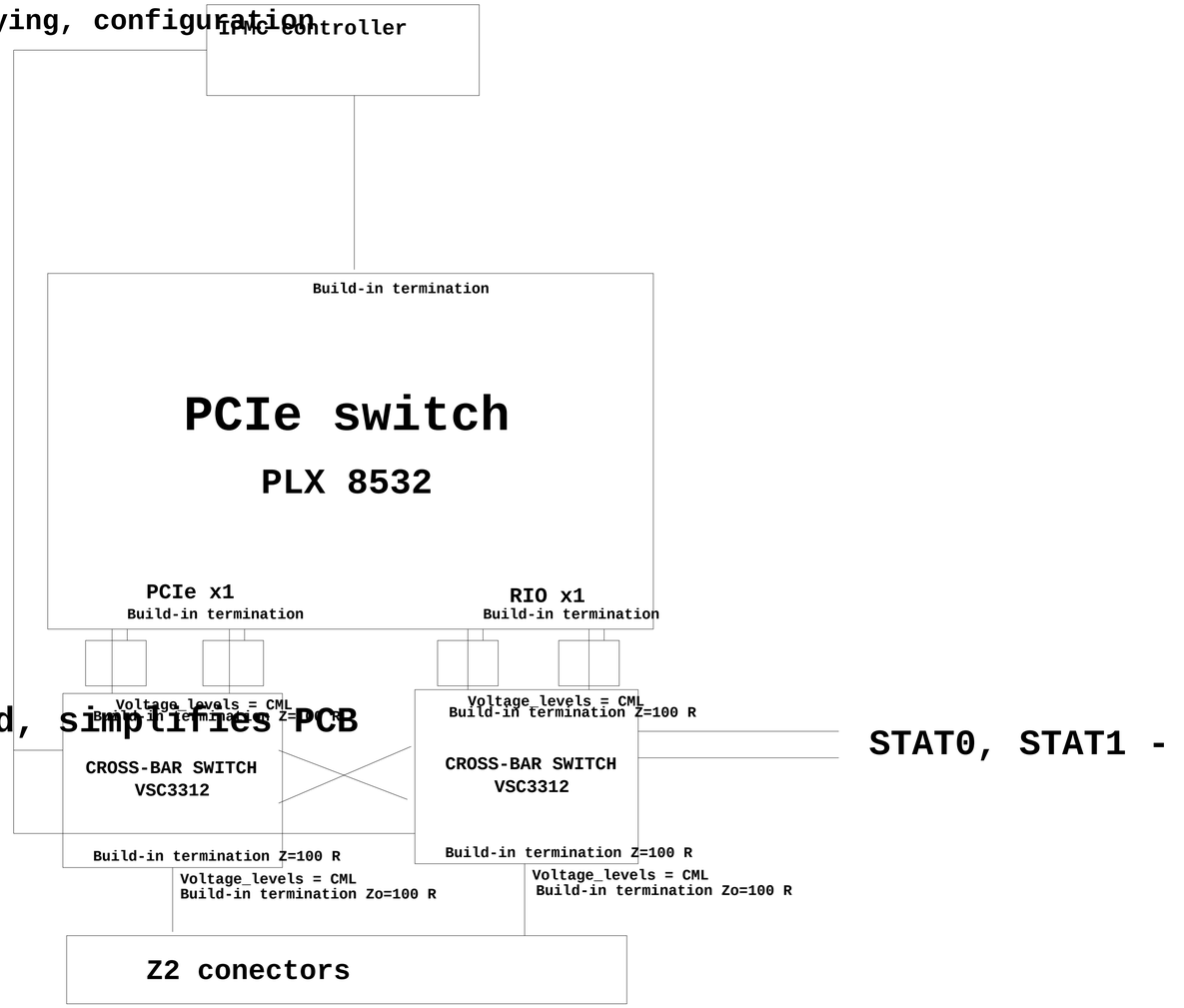


Engineer: WOJCIECH JALMUZNA	DESY-MSK Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 1
		Sheet: 1 of 1	
Drawn by: WOJCIECH JALMUZNA	Title: DIGITAL CLOCK DISTRIBUTION		
Changed by: WOJCIECH JALMUZNA			
Date Changed: 10-27-2008_20:43	Board Nr: <NR>	Drawing Nr: <NR>	

PCIe transmission according to PICMG 3.4, option 1 (x1)

PCIe signals on FAT pipe region ports 4-7, AMC.1 types 1 or 4

I2C bus - e-keying, configuration



STAT0, STAT1 - status pins

Remarks for VCS3312:

Input and Output Signals Invertion supported, simplifies PCB

Support for Loss of Signal on inputs

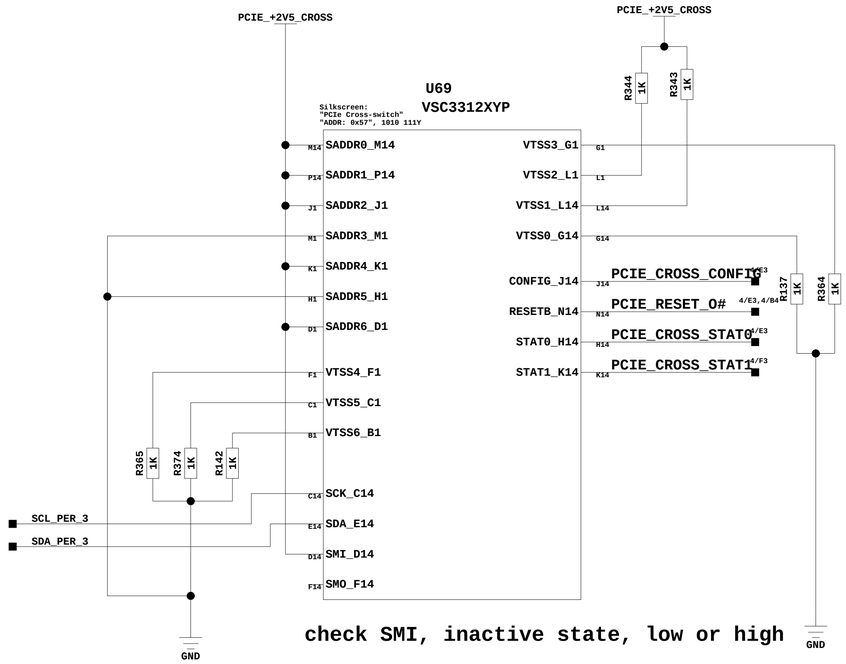
VDDio = 2V5/3V3, Vcore = 2V5

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 5	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE AND RIO CROSS-SWITCHES BLOCK DIAGRAM		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

Power consumption:

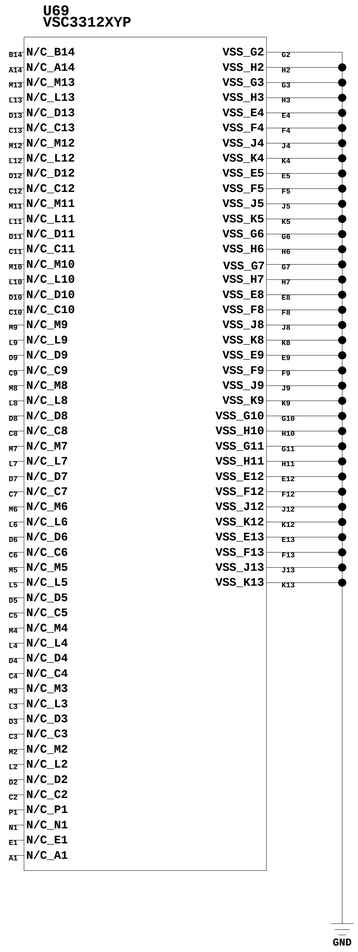
Pmax = 1.9W @ 2V5, Pmax = 3.9W @ 3V3 (12x in, 12x out)

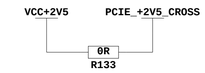
Pmax = 0.7W @ 2V5, Pmax = 1.3W @ 3V3 (4x in, 4x out)



check SMI, inactive state, low or high

check VOLTAGE LEVELS, MAYBE CONVERTER

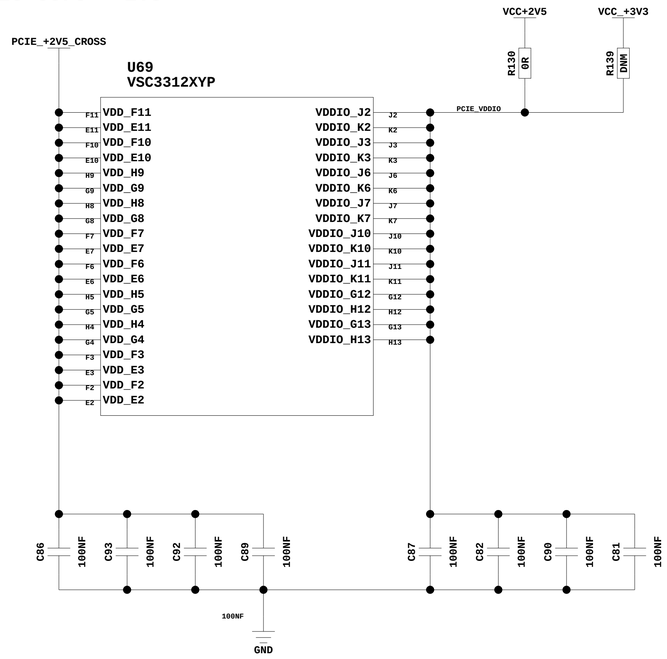




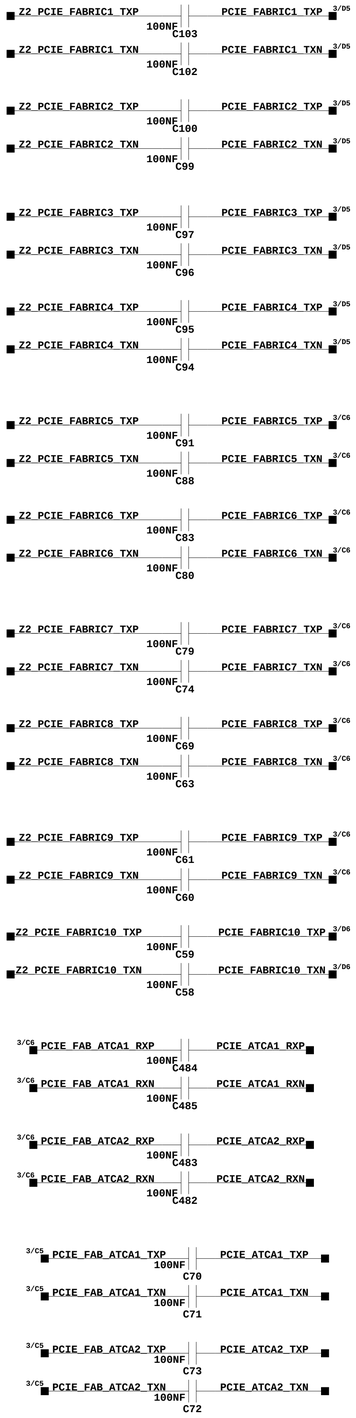
IO Supply voltage 2V5 or 3V3

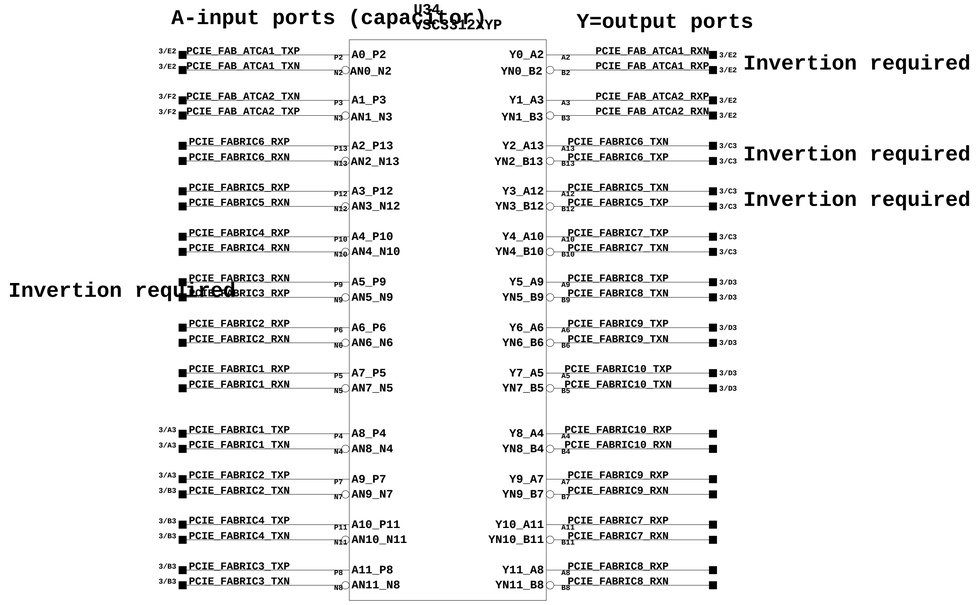
3V3 olny for 1300 mV diff swin

IO Core = 2V5

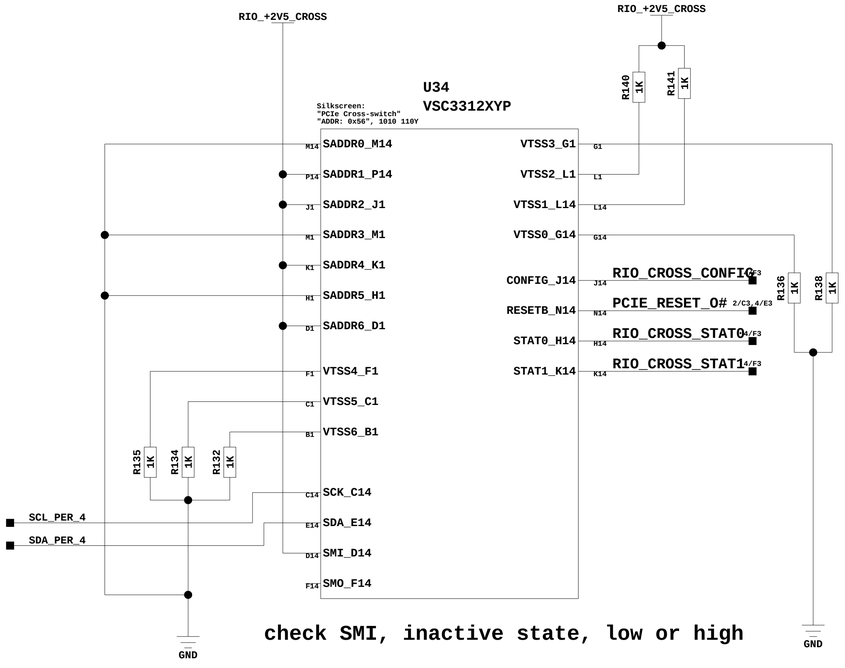


Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 2 of 5	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE CROSS-POINT SWITCH FOR ATCA BACKPLANE		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	



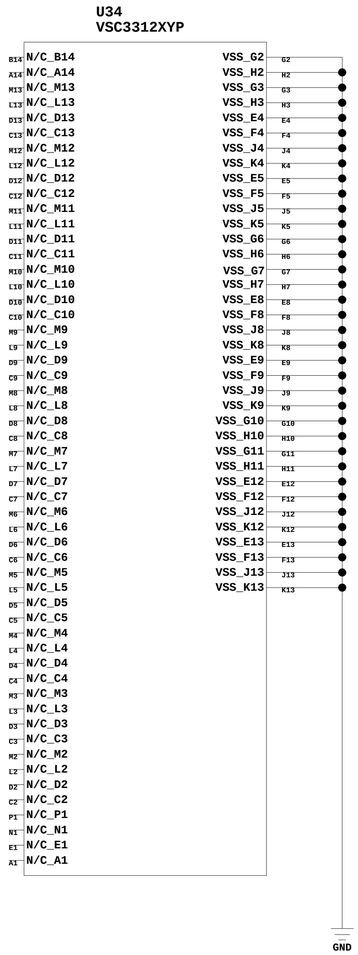


Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 3 of 5	
Drawn by: DARIUSZ MAKOWSKI	Title: PCIE CROSS-POINT SWITCH FOR ATCA PART 2		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	



check SMI, inactive state, low or high

check VOLTAGE LEVELS, MAYBE CONVERTER



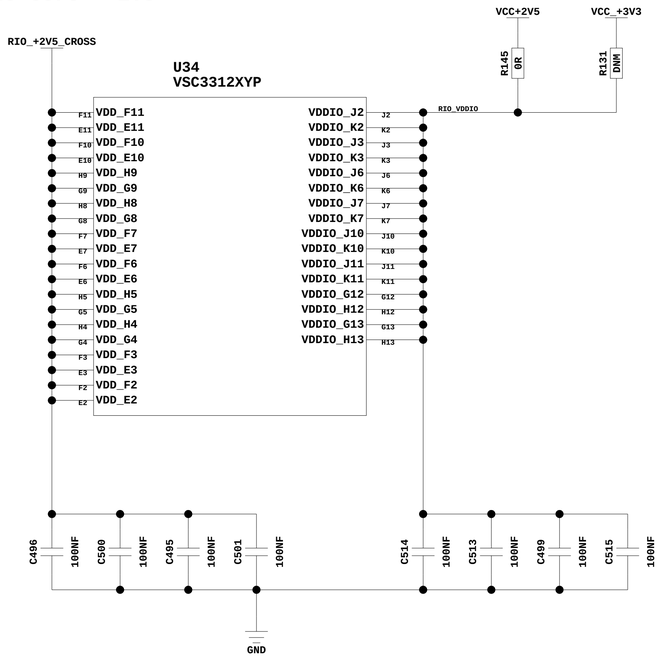
Power consumption:

Pmax = 1.9W @ 2V5, Pmax = 3.9W @ 3V3 (12x in, 12x out)

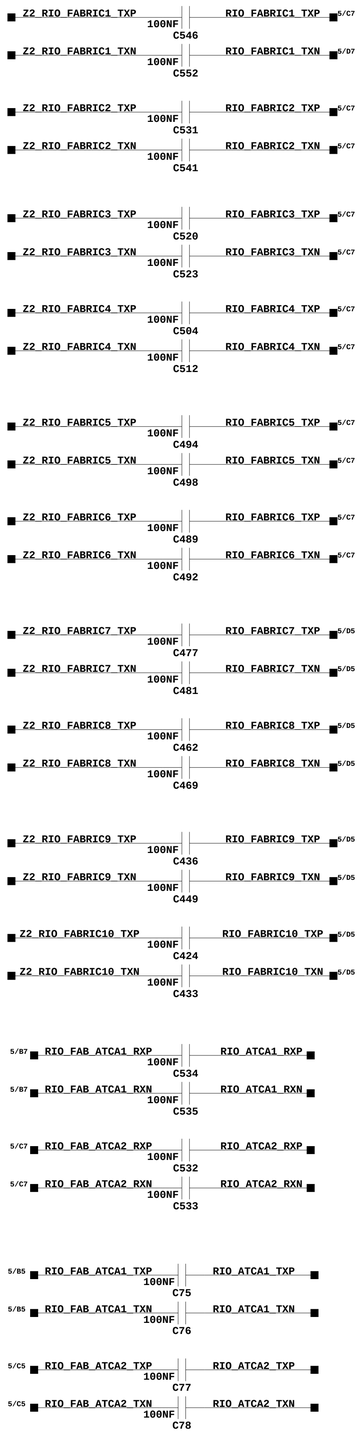
Pmax = 0.7W @ 2V5, Pmax = 1.3W @ 3V3 (4x in, 4x out)

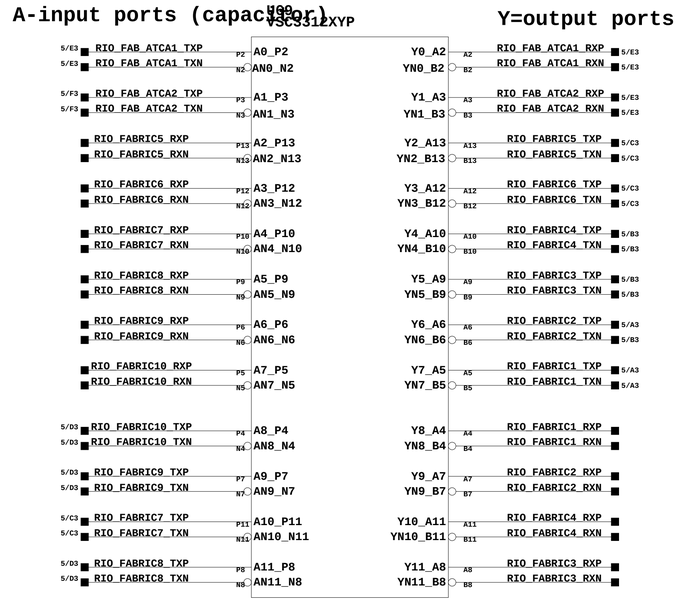
IO Core = 2V5

IO Supply voltage 2V5 or 3V3
3V3 olny for 1300 mV diff swin

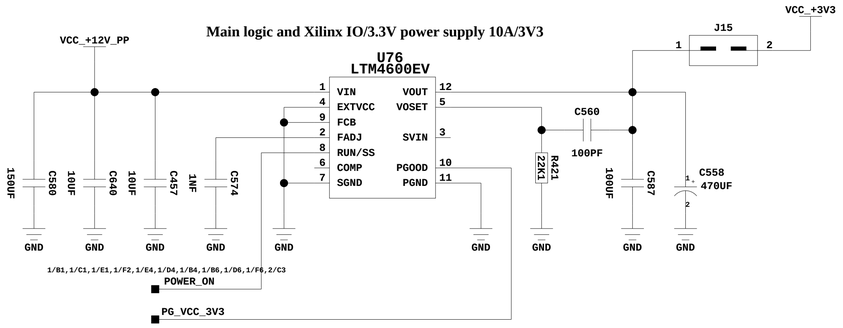


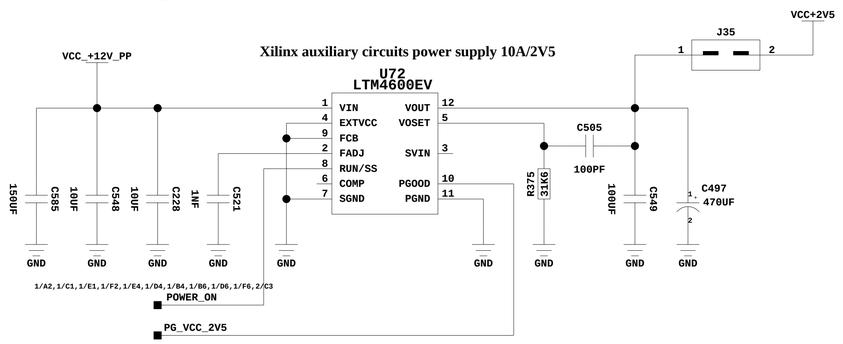
Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 4 of 5	
Drawn by: DARIUSZ MAKOWSKI	Title: RIO CROSS-POINT SWITCH FOR ATCA BACKPLANE		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

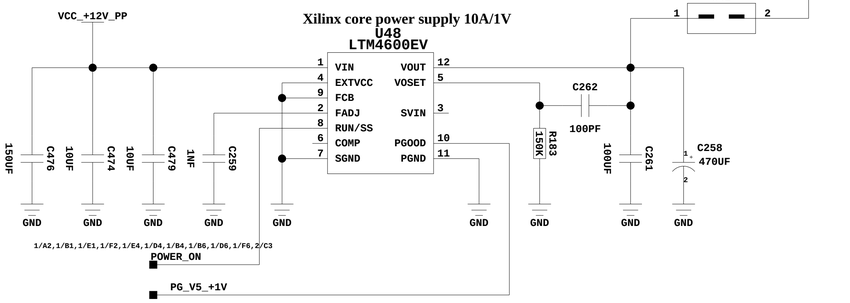


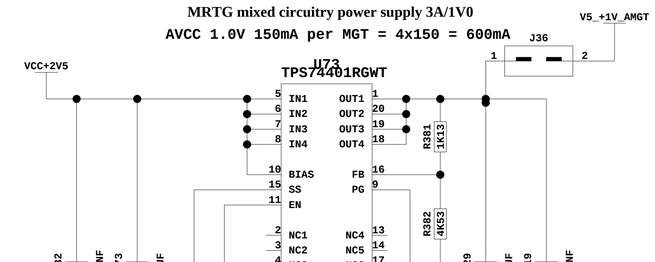


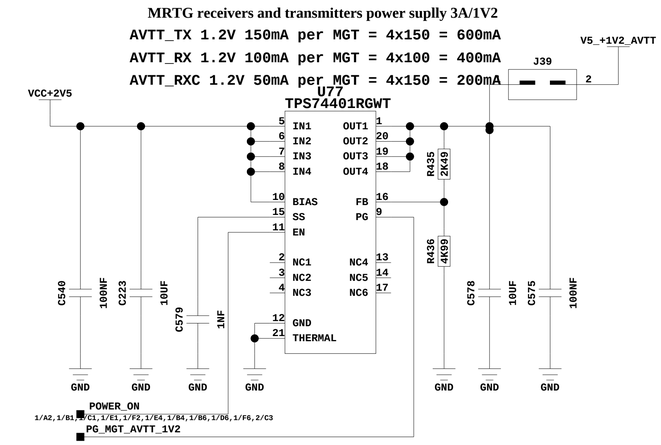
Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 5 of 5	
Drawn by: DARIUSZ MAKOWSKI	Title: RIO CROSS-POINT SWITCH FOR ATCA PART 2		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

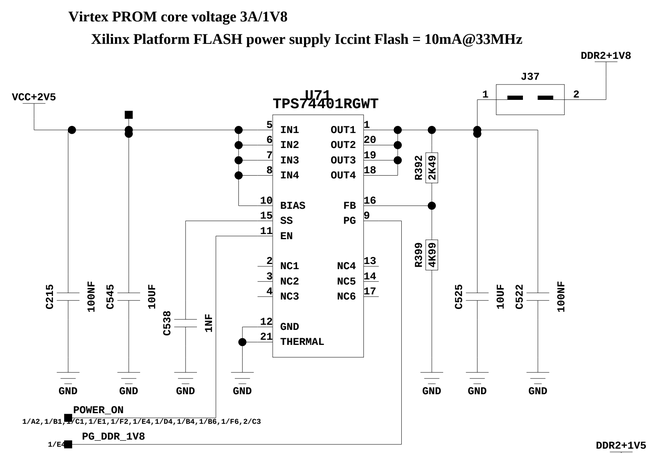




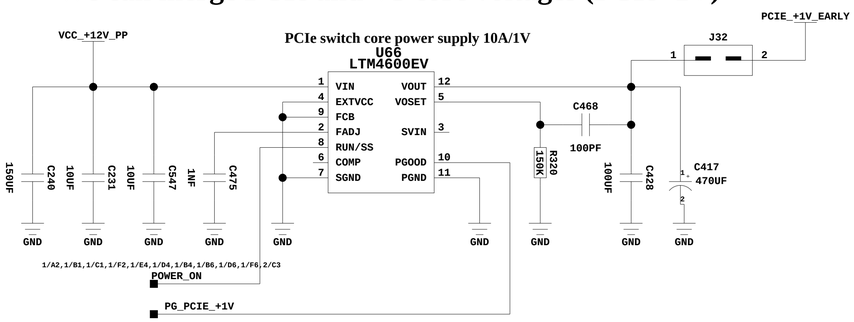


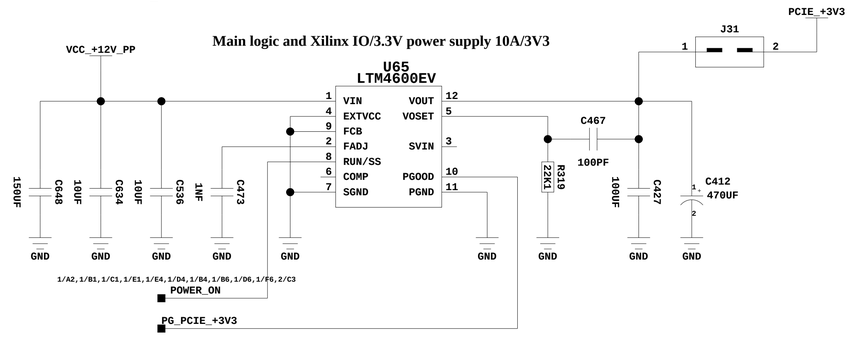


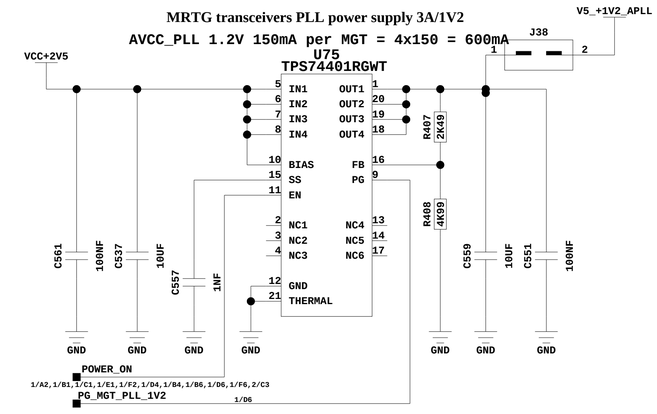


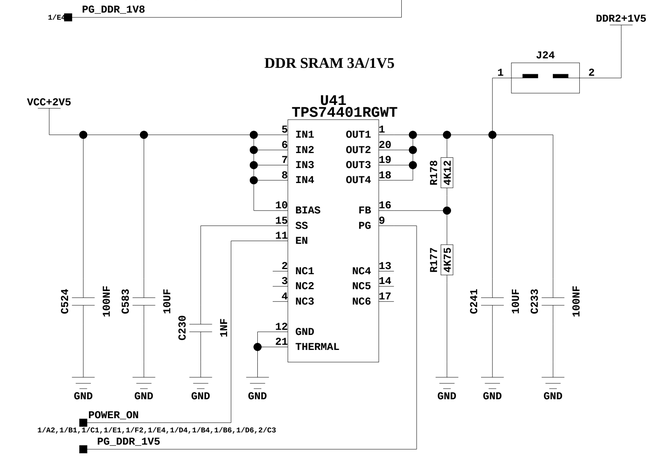


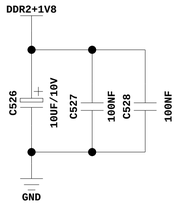
We can merge PCIe and V5 core voltages (PCIe>1V)



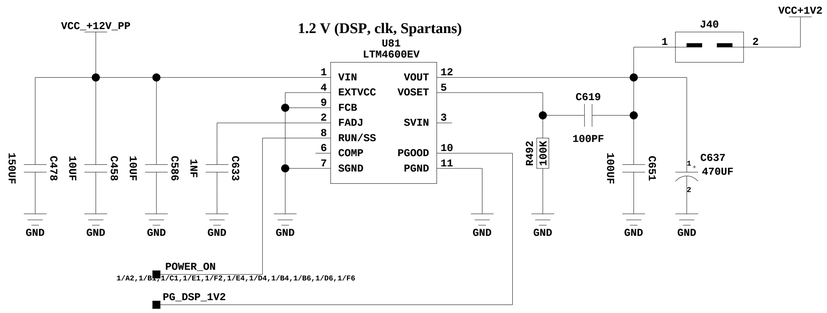




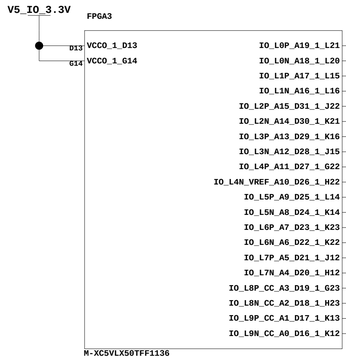


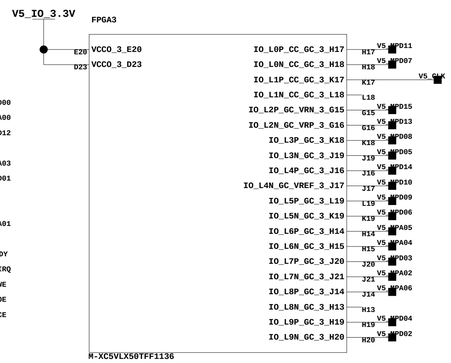


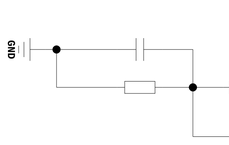
Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 1 of 2	
Drawn by: DARIUSZ MAKOWSKI	Title: MAIN POWER SUPPLY UNIT #1		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

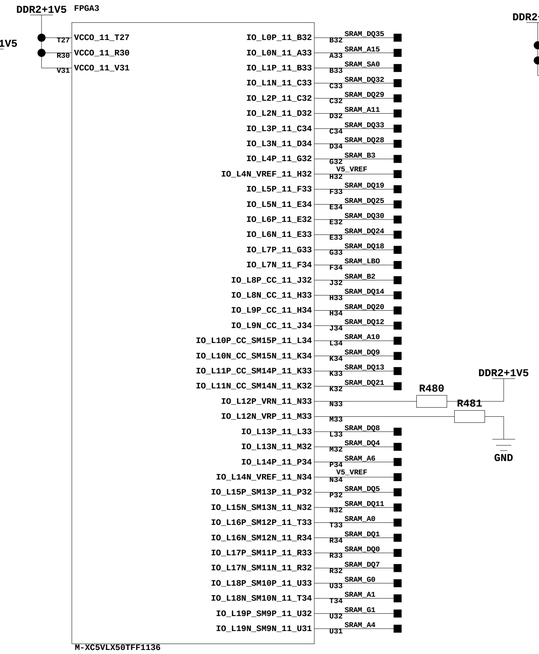


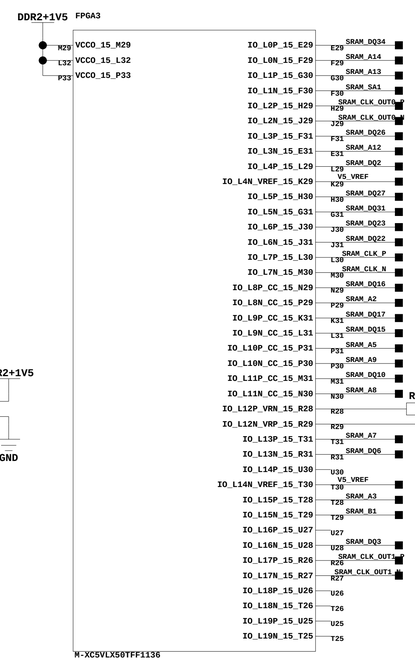
Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 2 of 2	
Drawn by: DARIUSZ MAKOWSKI	Title: MAIN POWER SUPPLY UNIT #2		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

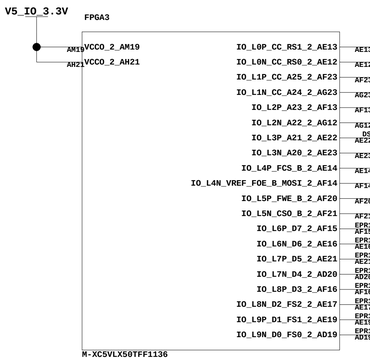


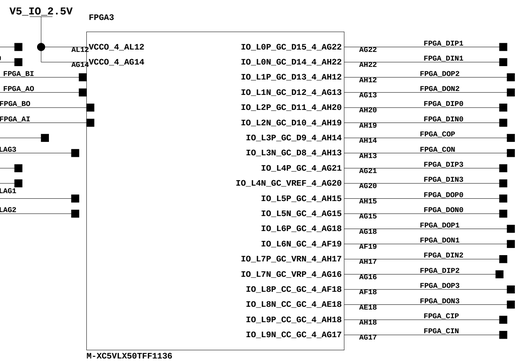


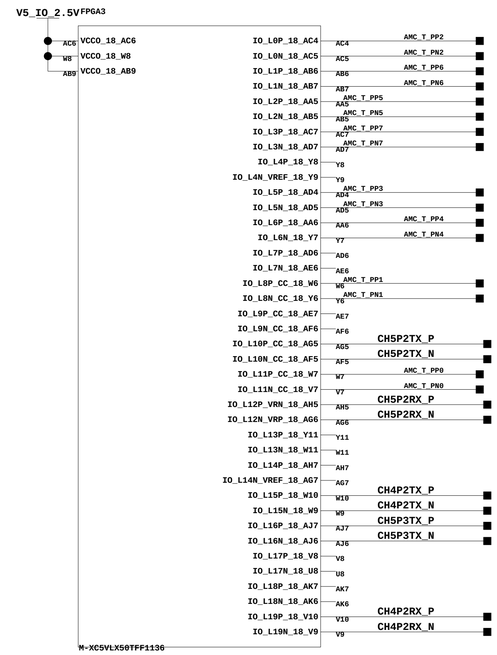


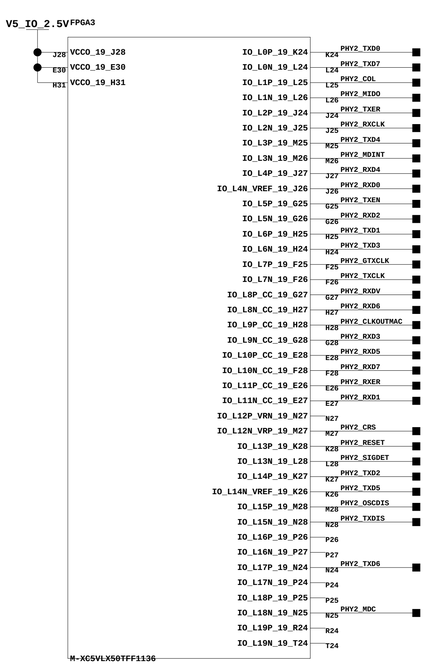


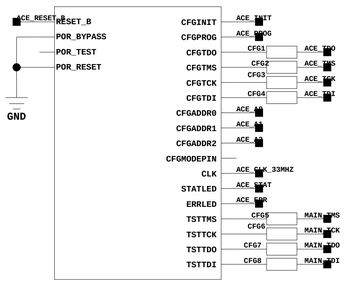


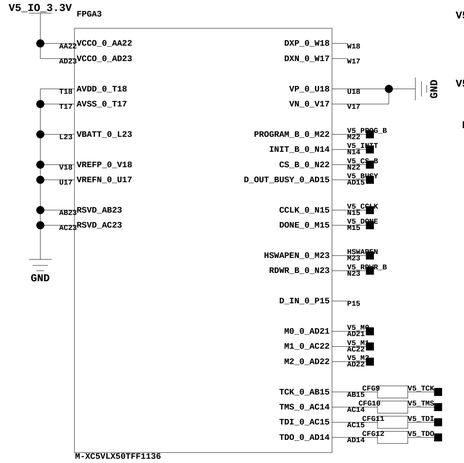


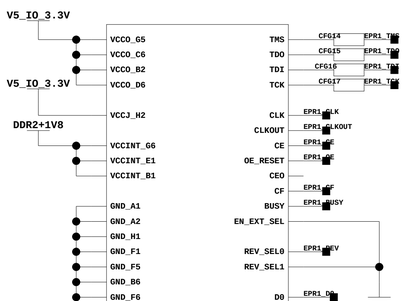


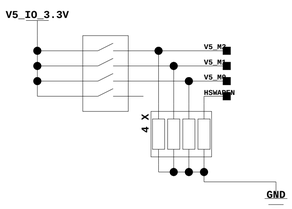


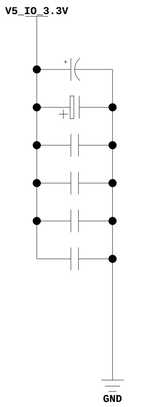


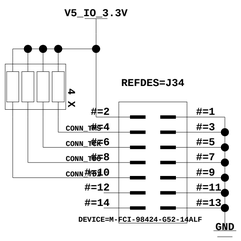


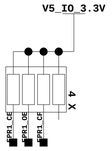


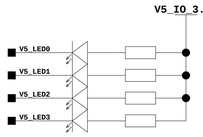




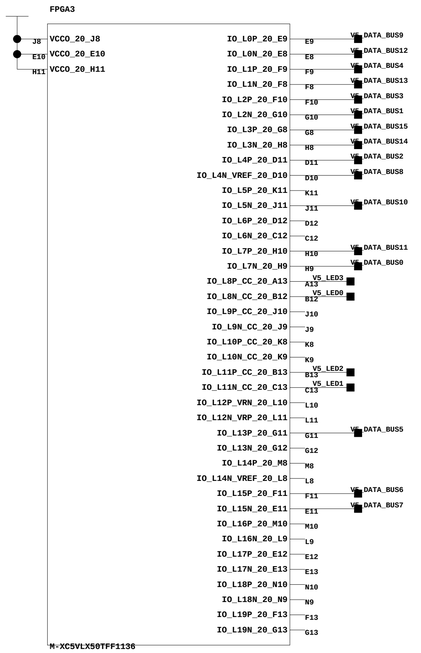


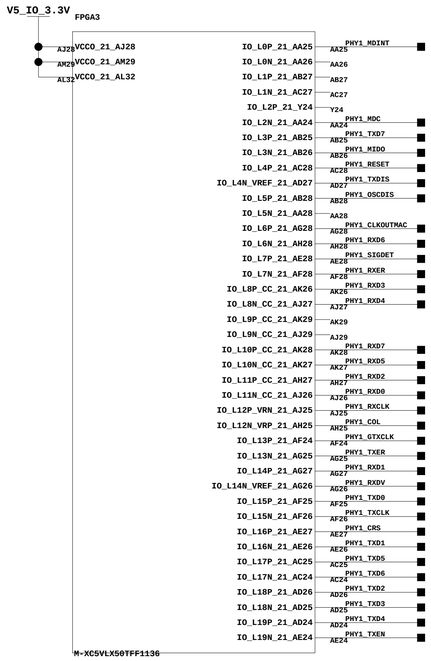


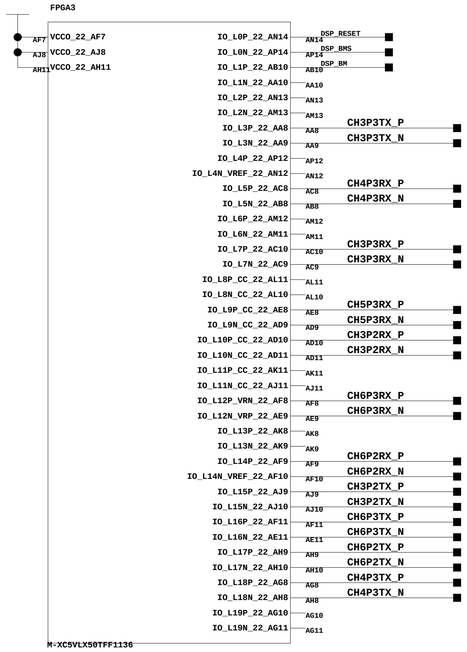


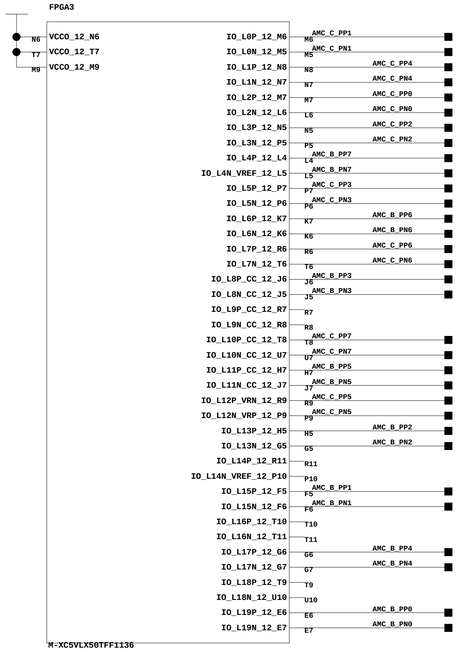


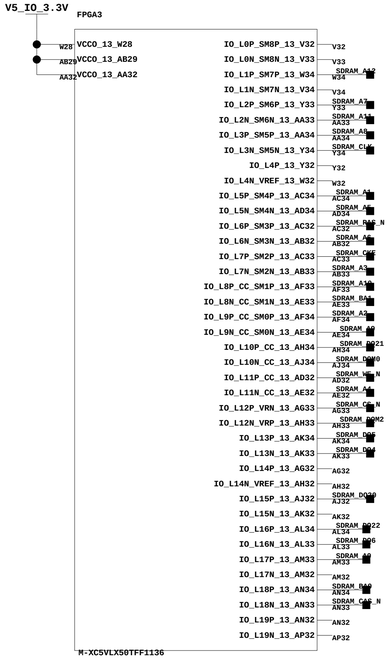
Engineer	DESY- Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev:
		Sheet: 1 of 1	
Drawn by:	Title:		
Changed by:			
Date Changed:	Board Nr: <NR>	Drawing Nr: <NR>	

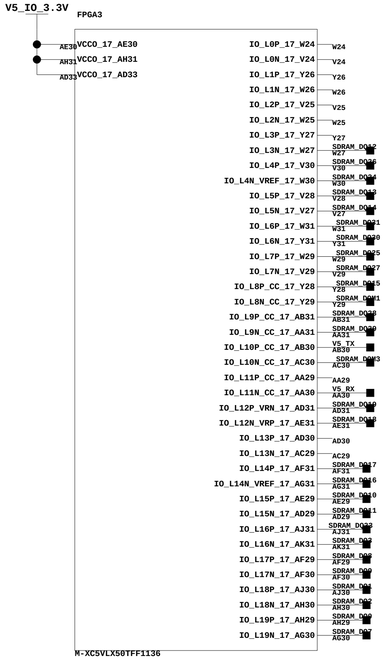




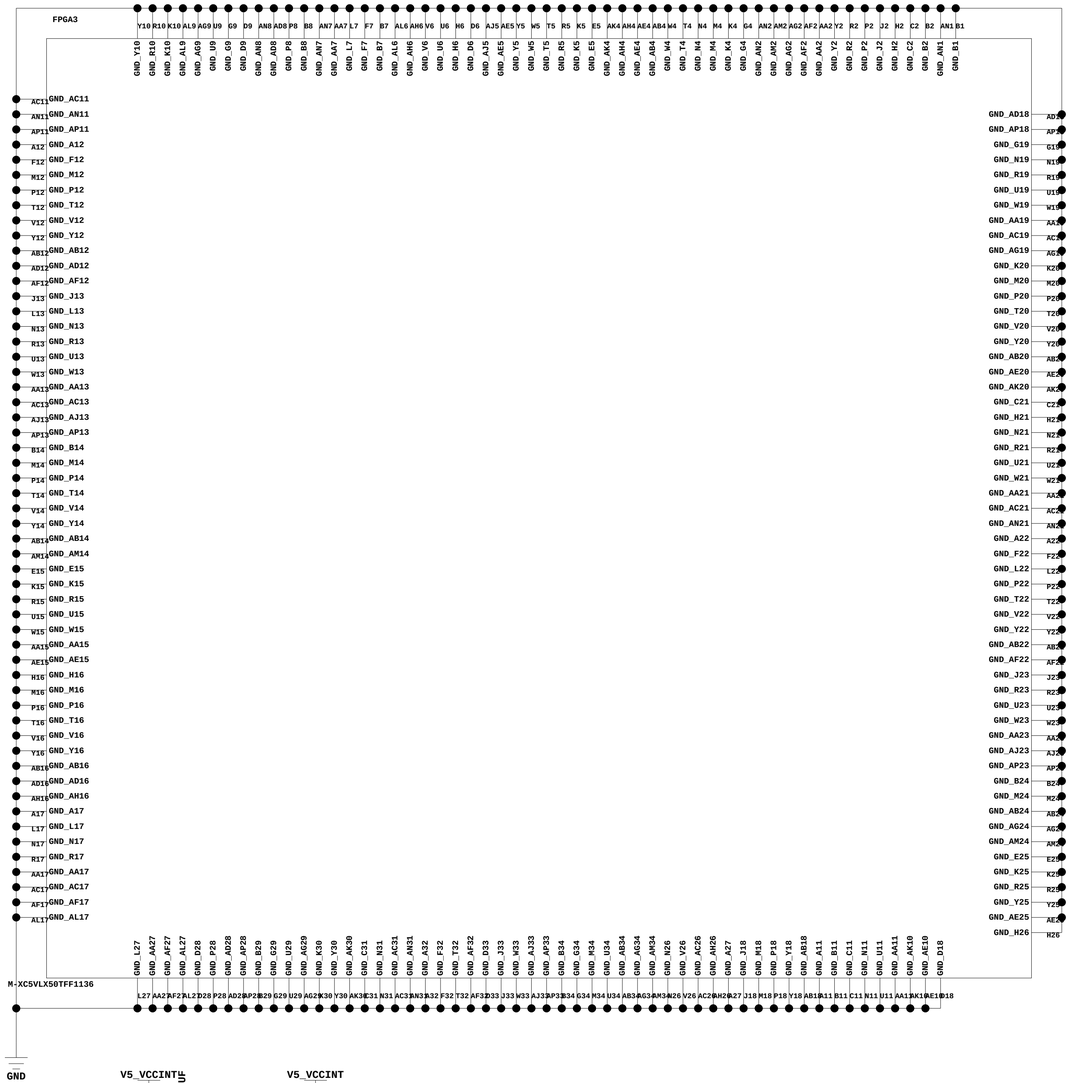


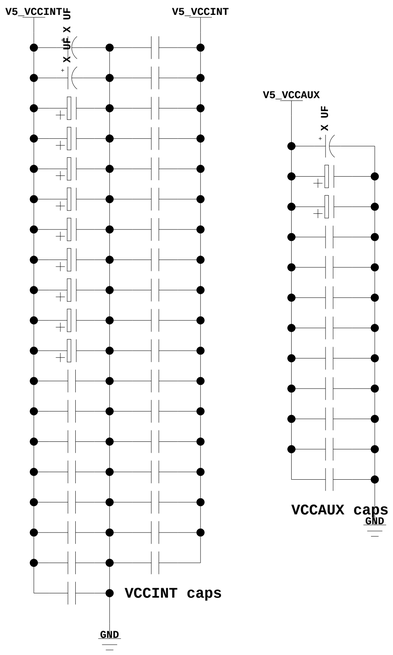


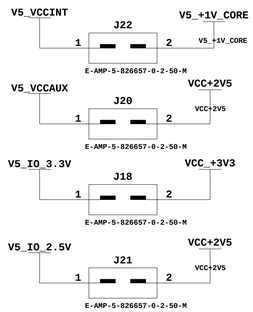


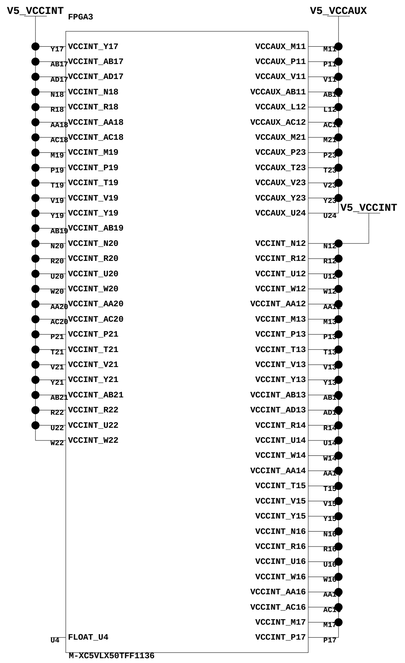


Engineer	DESY- Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev:
		Sheet: 1 of 1	
Drawn by:	Title:		
Changed by:			
Date Changed:	Board Nr: <NR>	Drawing Nr: <NR>	



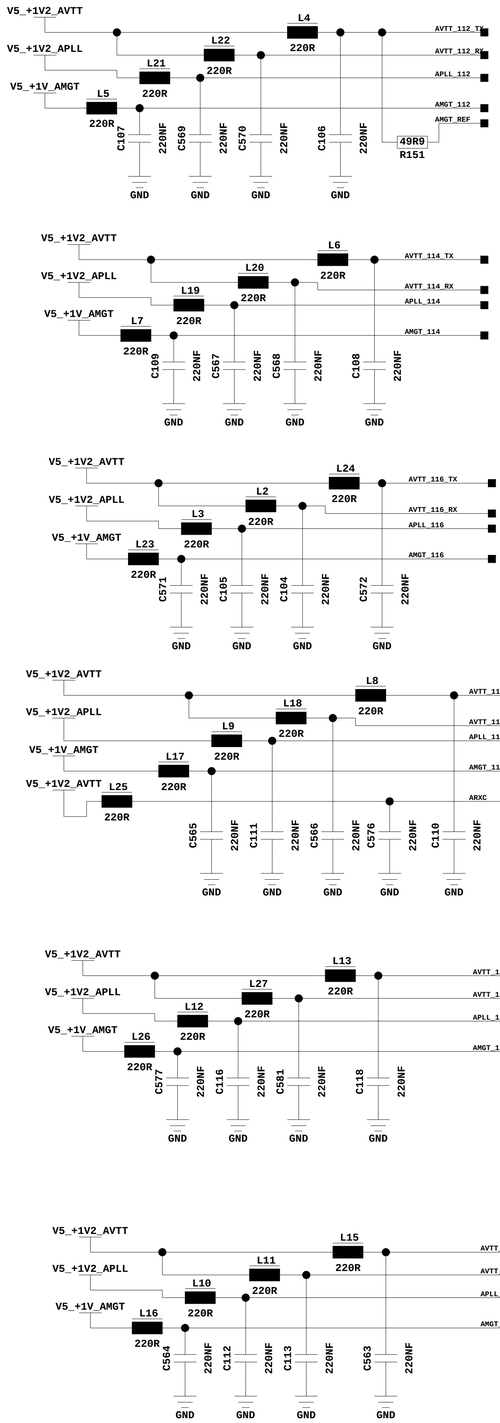


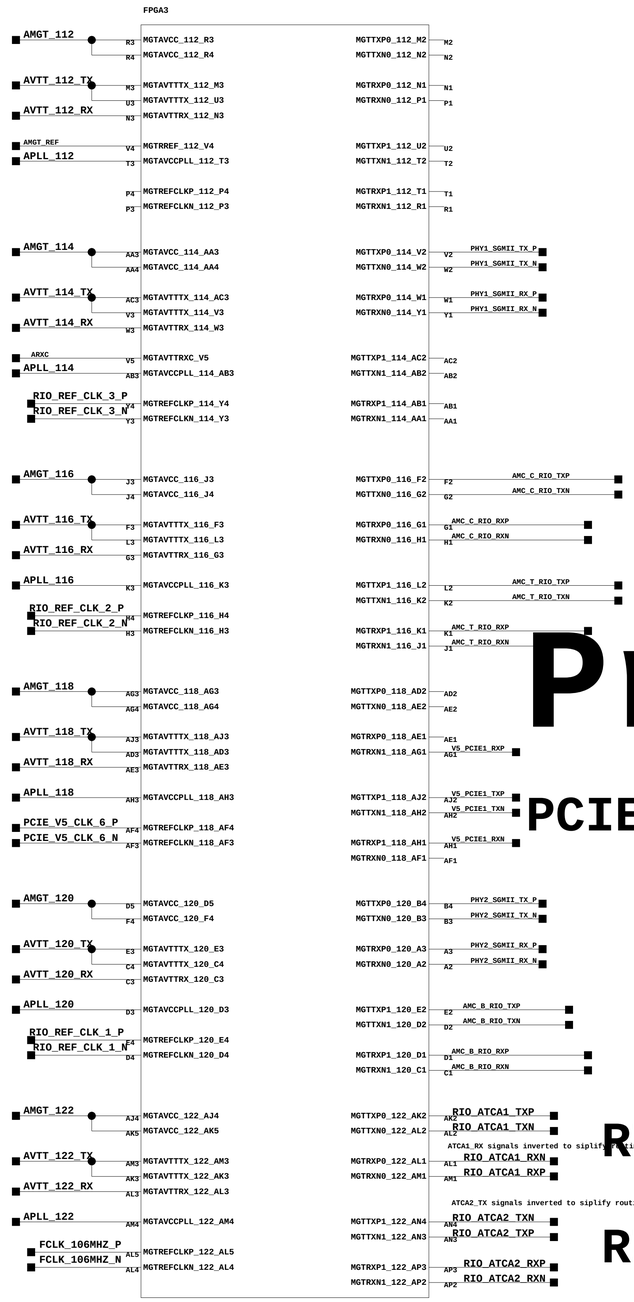




Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 3 of 1	
Drawn by: DM/WJ	Title: VIRTEX V5 MGT AND POWER SUPPLIES		
Changed by: DM/WJ			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

Change TX/RXPOLARITY0 for lanes possible (ug196.pdf)





PCIE x1

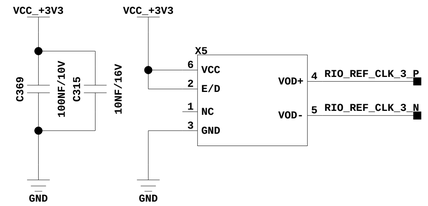
RIO x1

RIO x1

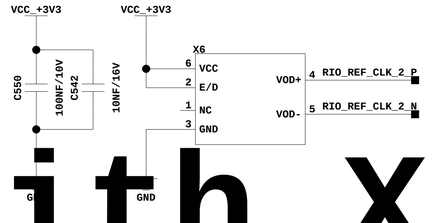
ATCA1_RX signals inverted to siplify routing

ATCA2_TX signals inverted to siplify routing

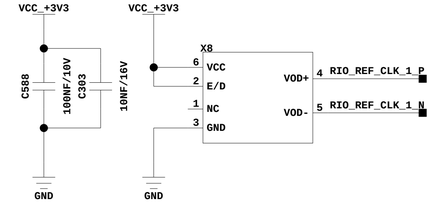
ARXC



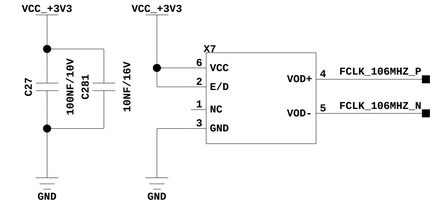
Rocket IO clock



Rocket IO clock



Rocket IO clock



Problem with Xil

Engineer: DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 4 of 1	
Drawn by: DM/WJ	Title: VIRTEX V5 MGT AND POWER SUPPLIES		
Changed by: DM/WJ			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	

Engineer DARIUSZ MAKOWSKI	DESY-MSK/DMCS Notkestrasse 85 D-22607 Hamburg	Size: A3	Rev: 0
		Sheet: 5 of 1	
Drawn by: DARIUSZ MAKOWSKI	Title: VIRTEX V5 MGT POWER SUPPLY		
Changed by: DARIUSZ MAKOWSKI			
Date Changed: 10-27-2008_20:43	Board Nr: CARRIER V2	Drawing Nr: <NR>	