

AMC - DESY

SPECIFICATION

**Advanced Mezzanine Card
AMC.1 Extension**

MSK Group

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Version 1.3**

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Revision History

Date	revision	Change	Signature
15.02.2007	0.0	Created	Tomasz Jezynski
01.03.2007	1.0	First published version	
13.04.2007	1.1	Interlock signals added	
09.08.2007	1.2	AMC Extension	
03.12.2007	1.3	RF inputs 81MHz & 1.3GHz	
05.03.2008	1.3	Updated Fig.4	

1. Introduction

At DESY a Low Level RF Control System is under development for FLASH and the proposed XFEL accelerator complex system. As one of the electronic standards for this control system the Advanced Telecommunications Computing Architecture (AdvancedTCA or ATCA) is under consideration. AdvancedTCA incorporates the latest trends in high speed and low latency interconnection technologies, and improved reliability, availability and serviceability. The Advanced Mezzanine Card (AMC) base specification¹ and its a subsidiary specification AMC.1² define the base-level requirements for a wide range of high speed mezzanine cards optimized for but not limited to AdvancedTCA Carriers³ and μ TCA.

For the low level RF system it is required to avoid front panel connections, what means that all specific signals for the LLRF system must be available on edge connectors of the AMC card. The consequence of mentioned above requirement is need to modify classical AMC connector, but it must be still possible to connect a standard AMC module to modified connector.

2. Description

The AMC-DESY connector is used to transfer all signals to the AMC module which are described in the AMC.1 specification.

In addition it is specified to transfer:

1. specific analog signals characteristic for LLRF systems to and from the AMC bay , like the probe signal representing the accelerating field in the cavity, the RF reference signal of the master oscillator and the vector modulator (VM) output signal driving the high power klystron,
2. digital signals such as clock signals for the ADCs as well as trigger signals,
3. multi bit data with high speed and low latency between the AMC module and the carrier board in parallel to the standard PCIExpress link
4. data between FPGAs and DSPs located on AMC modules and a carrier cards or vice versa.

3. Requirements

The following signals, in addition to signals defined win AMC1. spec, must be available for AMC modules:

- 10 lines for analog signals of up to 1.3GHz and 0dBm (8 x probe signals, 1 x RF reference signals, 1 x RFout

¹ Reference to PICMG AMC base specification

² Reference to AMC.1 specifications

³ Reference to ATCA Specification PICMG 3.0

- 1 x differential line for coded clock signals (2.6 GHz, 0dBm)
- 3 x clock signals, differential LVDS, bus
- 3x trigger signals, differential LVDS bus
- 10 x lines for low latency protocol, up to 3.5Gbps for a DSP TigerSHARC (according to Analog Device spec).

The AMC connector must support DESY modules, made according to that specification, as well as the standard AMC modules full and half high size.

A mechanical problem must

4. Specification

Specification presented below covers following aspects:

- signals description
- connector type
- pin assignments
- mechanical construction of AMC module

4.1 Signals description

Common issues:

Isolation: RF reference (1300MHz) and LO at IF < 50 dBm

RF crosstalk: better than -45 dB between any two RF channels

Operating temperature range: -10 deg. C to +70 deg. C

Humidity: max 95 % none condensing

Analog signals

- 10 x differential line, 100 Ohm, dedicated for probe signals – 10MHz – 1.3 GHz, 0dBm
8 lines devoted to probe signal , or forward or reflected power
2 line for monitoring or spare
- 1 x RF reference, differential lines 100 Ohm – 1.3 GHz, 0dBm
- 2 x RF output, differential line, 100 Ohm – 1.3 GHz, 0dBm,
alternative usage: any other RF signal

Digital signals

- 3 x clock, frequency 100 kHz -100 MHz, LVDS bus, stability 5 ps rms
- 3 x trigger, frequency 1Hz -100 MHz, LVDS bus, stability 500 ps rms

- 1 x coded clock, differential line, 100 Ohm, 0dBm,
alternative usage: second RF reference
- 10 x differential line for low latency protocol, LVDS, 100 Ohm, up to 3.5Gbps.5Gbps
- line for DSP link (according to Analog Device spec)
 - 4 x LVDS line for data transferred from AMC module
 - 4 x LVDS line for data transferred to AMC module
 - 2 x LVDS line for clock
 - 4 x single-ended LVCMOS (2.5V) for handshake

4.2 Connector type

The A+B+ connector has been chosen for an AMC-DESY slot. Its B+ part fulfils the AMC.1 specification, while the A+ part of the connector is deviating from the AMC.1 standard and can only be used for signals required to operate the FLASH/XFEL-LLRF system. The A+B+ connector is shown in Figure 1a, and in Figure 1b the B+ connector is shown. Both presented connectors support the full high AMC module.

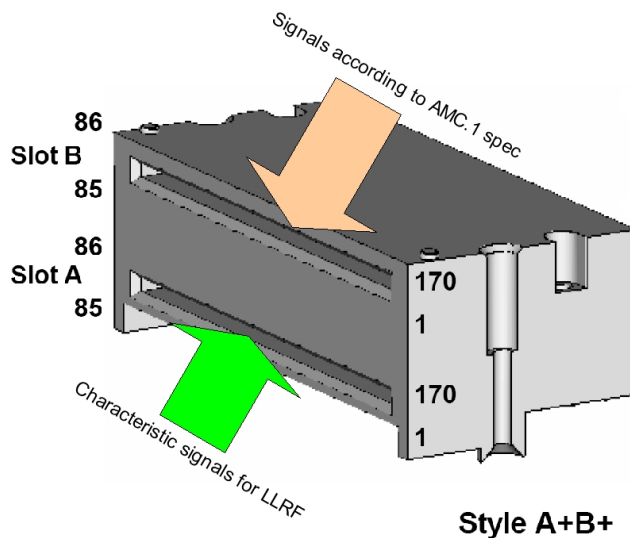


Fig. 1a. The standard A+B+ connector and its usage in LLRF system

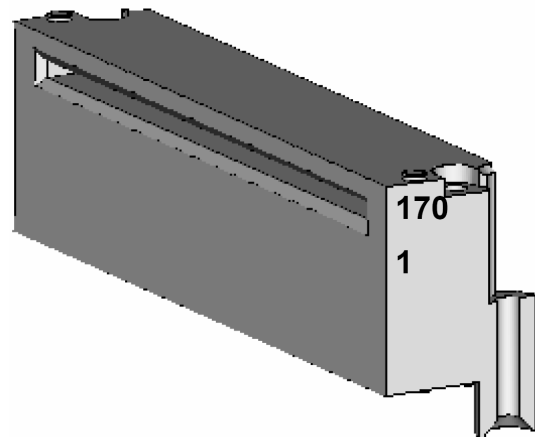


Fig. 1b. The standard B+ connector

The CN074-340-0001 connector from Yamaichi has been chosen. The CN074 series connectors are designed for use with high-speed interfaces up to 12.5 Gbit/s and all connectors from these series are designed for $100\ \Omega \pm 10\ \Omega$ controlled impedance. Its outline dimension is shown in Figure 2 and PCB layout is shown in Figure 3. In this type connector there are only mounting holes. Particular pins of the CN074 are connected directly to pads on PCB (see Figure 3)

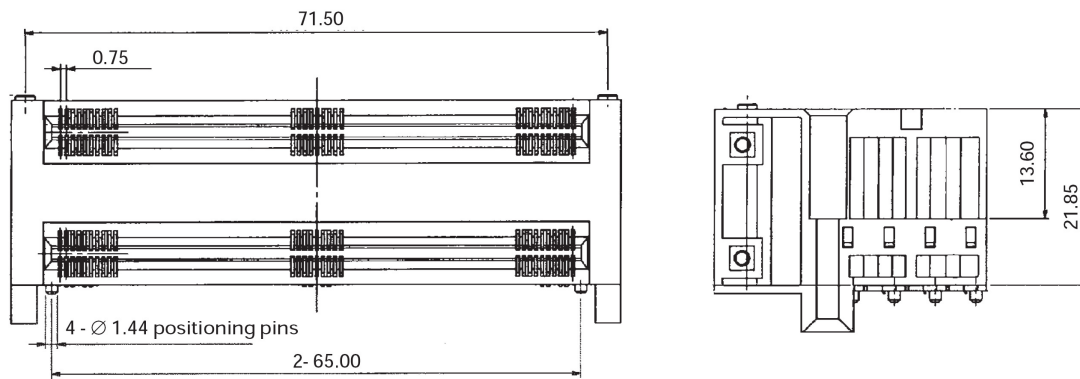


Fig. 2. Outline Connector Dimensions CN074-340-0001

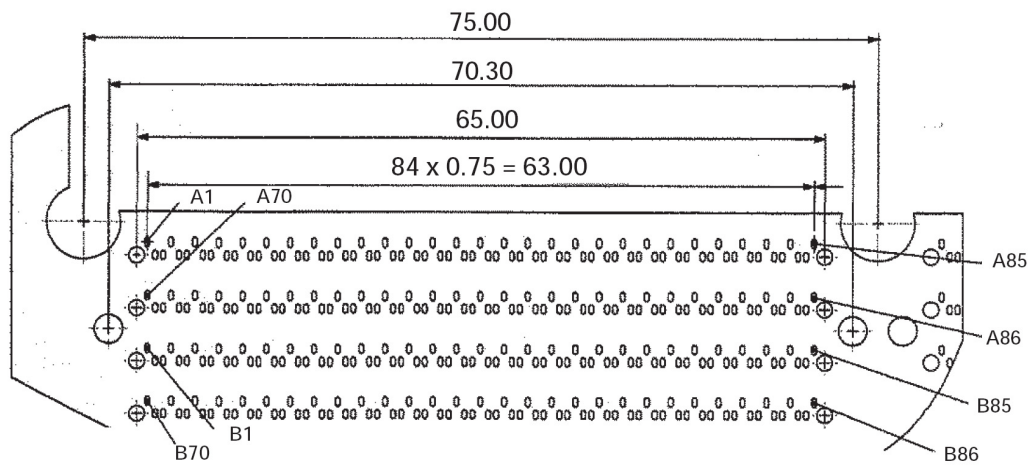


Fig. 3. PCB Layout CN074-340-0001

Signals distribution on A+B+ connector is shown in Figure 3 and description is given in Table 1.

A n p 0 0	A n p 2 2	A n p 4 4	A n p 6 6	A n p 8 8	C C n p 0 0	R F n p 0 0	In t1	A A l O	D D ln lp 1 1	D D ln lp 2 2	D D ln lp 3 3	D D ln lp 4 4	C C ln lp	C C n p 1 1	C C n p 2 2	C C n p 3 3	P P n p 0 0	P P n p 2 2	P P n p 4 4	P P n p 6 6	P P n p 8 8
A n p 1 1	A n p 3 3	A n p 5 5	A n p 7 7	A n p 9 9	C C 2n 2n p 0 0	R F n p 1 1	In t3	B B O l	D D n p 1 1	D D O n p 2 2	D D O n p 3 3	D D O n p 4 4	C C O n p	T T n p 1 1	T T n p 2 2	T T n p 3 3	P P n p 1 1	P P n p 3 3	P P n p 5 5	P P n p 7 7	P P n p 9 9

Fig. 4 Signals on the AMC-DESY connector (lower row)

An0, Ap0-An9,An9 – inputs (negative and positive), analog signals IF or 1.3GHz, point-to-point Z3

1.3GHz+, 1.3GHz-: RF reference, 1.3 GHz, spare,
point-to-point (splitter) Z3

81MHz+, 81MHz-: RF reference, 81 MHz, spare,
point-to-point (splitter) Z3

RF_{pn1}, RF_{op1} – RF 1.3GHz output, point-to-point

RF_on2,RF_op2 – RF 1.3GHz output, spare, point-to-point Z3, alternative use possible

Cn1,Cp1 – Cn3,Cp3 – clock signals, LVDS bus

Tn1, Tp1 – Tn1, Tp1 – trigger signals, LVDS bus

Pn0, Pp0 – Pn9, Pp9 - own protocol, point-to-point, connected directly to the main FPGA on the carrier board

DIn1,DIp1 – DIn1,DIp1 – data in for DSP link

DOn1,DOp1- DOn1,DOp1 – data out for DSP link

CIn, Clp – clock input for DSP link

Con, Cop – clock out for DSP link

AO – ACKO for DSP link

AI - ACKI for DSP link

BI - BCMPI for DSP link

BO - BCMO for DSP link
Int1-Int4 – interlock signals

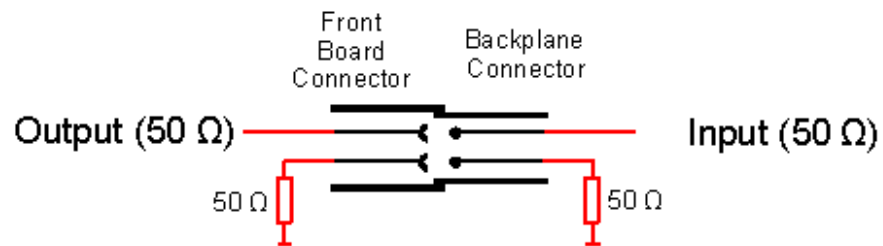
20	Cp2		151	Tp2
21	Cn2		150	TN2
22	GND		149	GND
23	Cp1		148	Tp1
24	Cn1		147	Tn1
25	GND		146	GND
26	Clp		145	COp
27	Cln		144	COn
28	GND		143	GND
29	Dlp4		142	DOp1
30	Dln4		141	Don1
31	GND		140	GND
32	Dlp3		139	DOp2
33	Dln3		138	DOn2
34	GND		137	GND
35	Dlp2		136	DOp3
36	Dln2		135	DOn3
37	GND		134	GND
38	Dlp1		133	DOp4
39	Dln1		132	DOn4
40	GND		131	GND
41	AO		130	BI
42	AI		129	BO
43	GND		128	GND
44	Int2		127	Int4
45	Int1		126	Int3
46	GND		125	GND
47	* RFop0		124	* RFop1
48	* RFon0		123	* RFon1
49	GND		122	GND
50	GND (Opp11)		121	GND (Opp12)
51	GND (Opn11)		120	GND (Opn12)
52	GND		119	GND
53	* 1.3GHz+		118	* 81MHz+
54	* 1.3GHz-		117	* 81MHz-
55	GND		116	GND
56	GND (Opp9)		115	GND (Opp10)
57	GND (Opn9)		114	GND (Opn10)
58	GND		113	GND
59	Ap9		112	Ap8
60	An9		111	An8
61	GND		110	GND
62	GND (Opp7)		109	GND (Opp8)
63	GND (Opn7)		108	GND (Opn8)
64	GND		107	GND
65	Ap7		106	Ap6
66	An7		105	An6
67	GND		104	GND
68	GND (Opp5)		103	GND (Opp6)
69	GND (Opn5)		102	GND (Opn6)
70	GND		101	GND
71	Ap5		100	Ap4
72	An5		99	An4
73	GND		98	GND

74	GND (Opp3)		97	GND (Opp4)
75	GND (Opn3)		96	GND (Opn4)
76	GND		95	GND
77	Ap3		94	Ap2
78	An3		93	An2
79	GND		92	GND
80	GND (Opp1)		91	GND (Opp2)
81	GND (Opn1)		90	GND (Opn2)
82	GND		89	GND
83	Ap1		88	Ap0
84	An1		87	Ap0
85	GND		86	GND

Table1. Assignment of pins in A+B+ connector – part A+ only.

* Remarks

Inputs and outputs signed with * mark are single-ended lines, but differential connector is used. To provide these signals following schema must be applied.



4.4 Mechanical construction of the AMC module

The standard, full high AMC module plugged to the AMC bay equipped with A+B+ connector is shown in 5. The same module can be connected to the AMC bay equipped with the B+ connector (only upper row of the A+B+ connector)

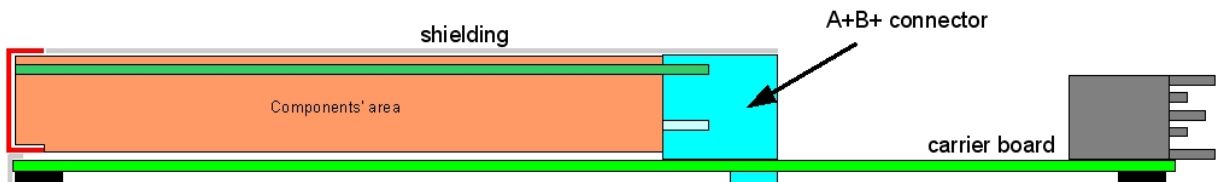


Fig. 5 Standard AMC full high module in AMC-DESY bay

Figure 6 shows the AMC DESY module connected to the A+B+ connector. The AMC DESY module consists of two boards – the main board and signal conditioning board. The main board is connected to the B+ (upper row) part of the A+B+ connector, while the signal conditioning board is connected to the A+ (lower row) part of the A+B+ connector.

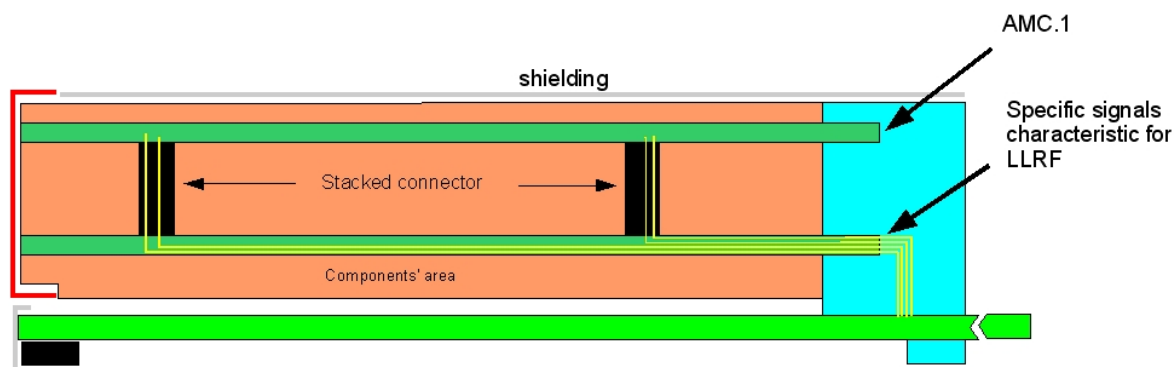


Fig. 6. Construction of the AMC DESY module.

Characteristic signals for LLRF system are provided to main board through the signal conditioning board and stacked connectors. Two connectors are used to reinforce the module mechanically, and in some cases increase isolation between signals (e.g. one connector may be devoted to analog signals, another one to digital signals). Required distance between boards is 13.5 mm. There is strong suggestion that all AMC boards, development at DESY should use the same type of connectors.

Presented solution allows to connect to the carrier board any standard AMC.1 module, full high or half high, and special AMC-DESY module. Figure 7a shows the carrier board equipped with A+B+ connector and the AMC-DESY module plugged into the AMC bay. Figures 7b shows the same carrier board but half high module is plugged to the AMC-DESYS bay.

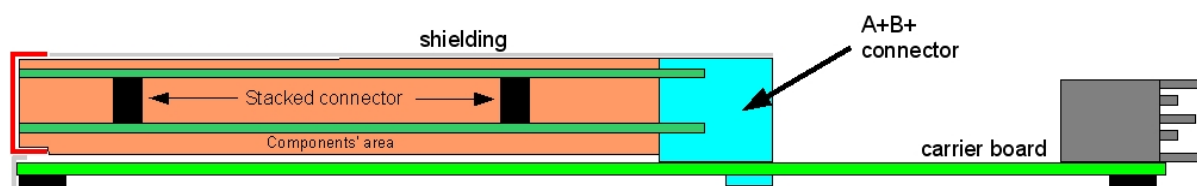


Fig. 7a DESY AMC module connected to ACM-DESY slot.

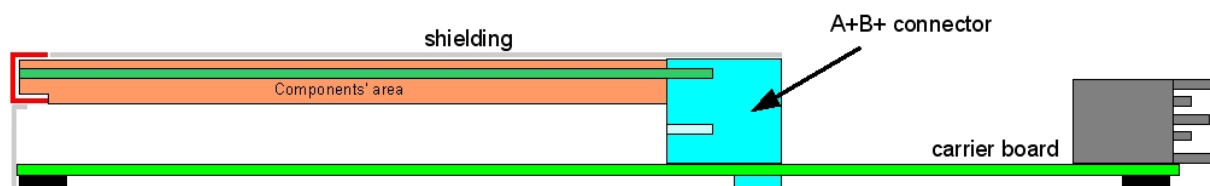


Fig. 7b. Standard AMC half high module in the AMC-DESY bay

4. Conclusion

A specialized AMC-DESY connector has been introduced. The first AMC card for the FLASH/XFEL LLRF control system, which fits this connector, is under construction as well as the appropriate ATCA carrier board designed to test its performance.

5. AMC-DESY Extension

It is possible to increase number of the point to point connections between ZONE3 and AMC connectors up to 22 channels per connector. These signals can be used as analog inputs or outputs. For this purpose, grounded signal pins (see Table.1) can be used. Optional pins are signed Op1 up Op12.