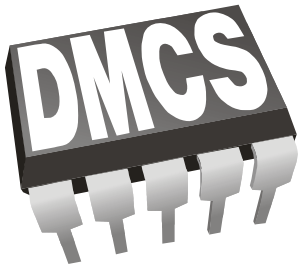
# FP7 - EuCARD

## LLRF at FLASH

S.Simrock, M.Grecki for the LLRF team

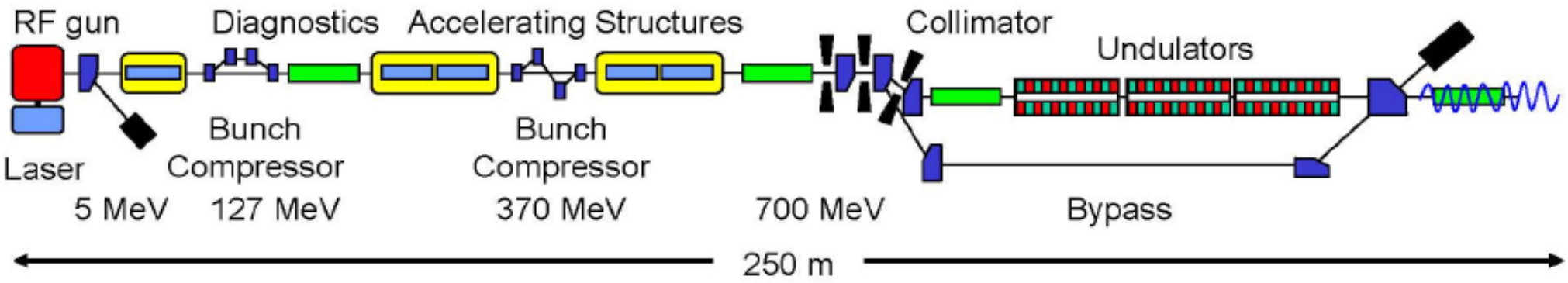


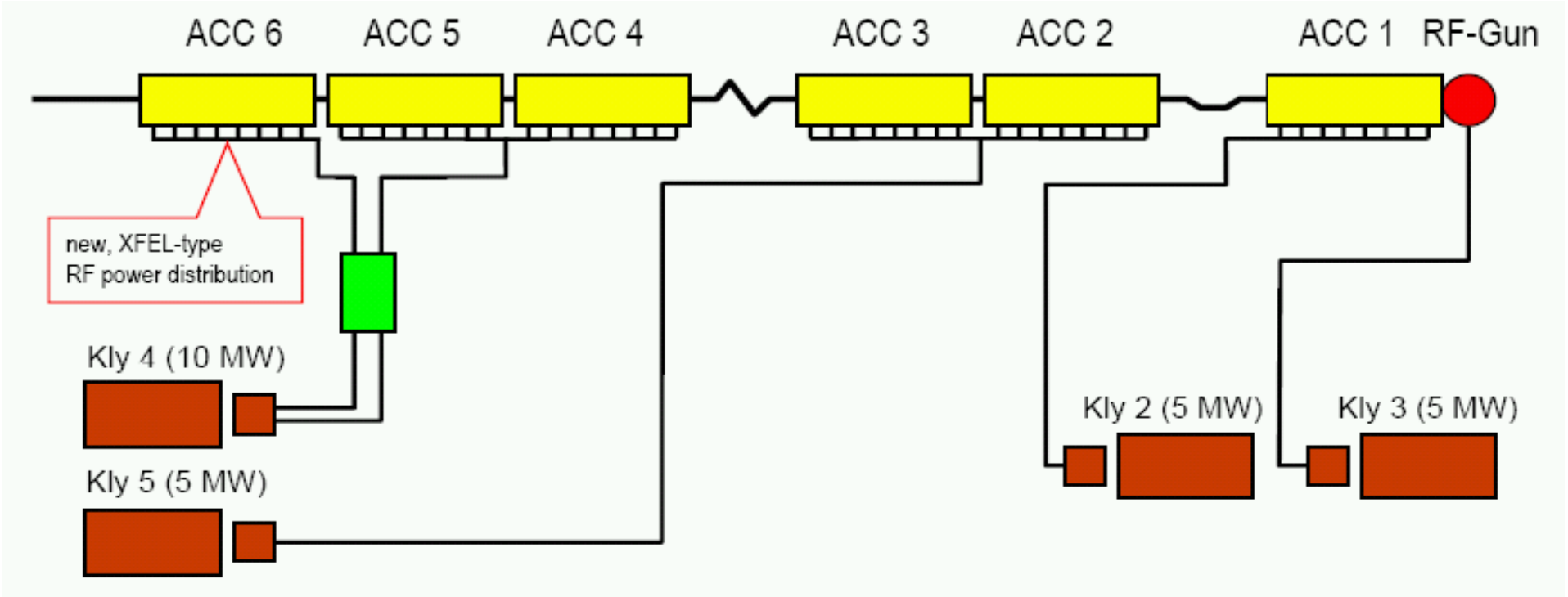
# Introduction

FLASH (Free-Electron LASer in Hamburg) is designed to produce SASE FEL radiation with a wavelength down to 6 nm with high brilliance

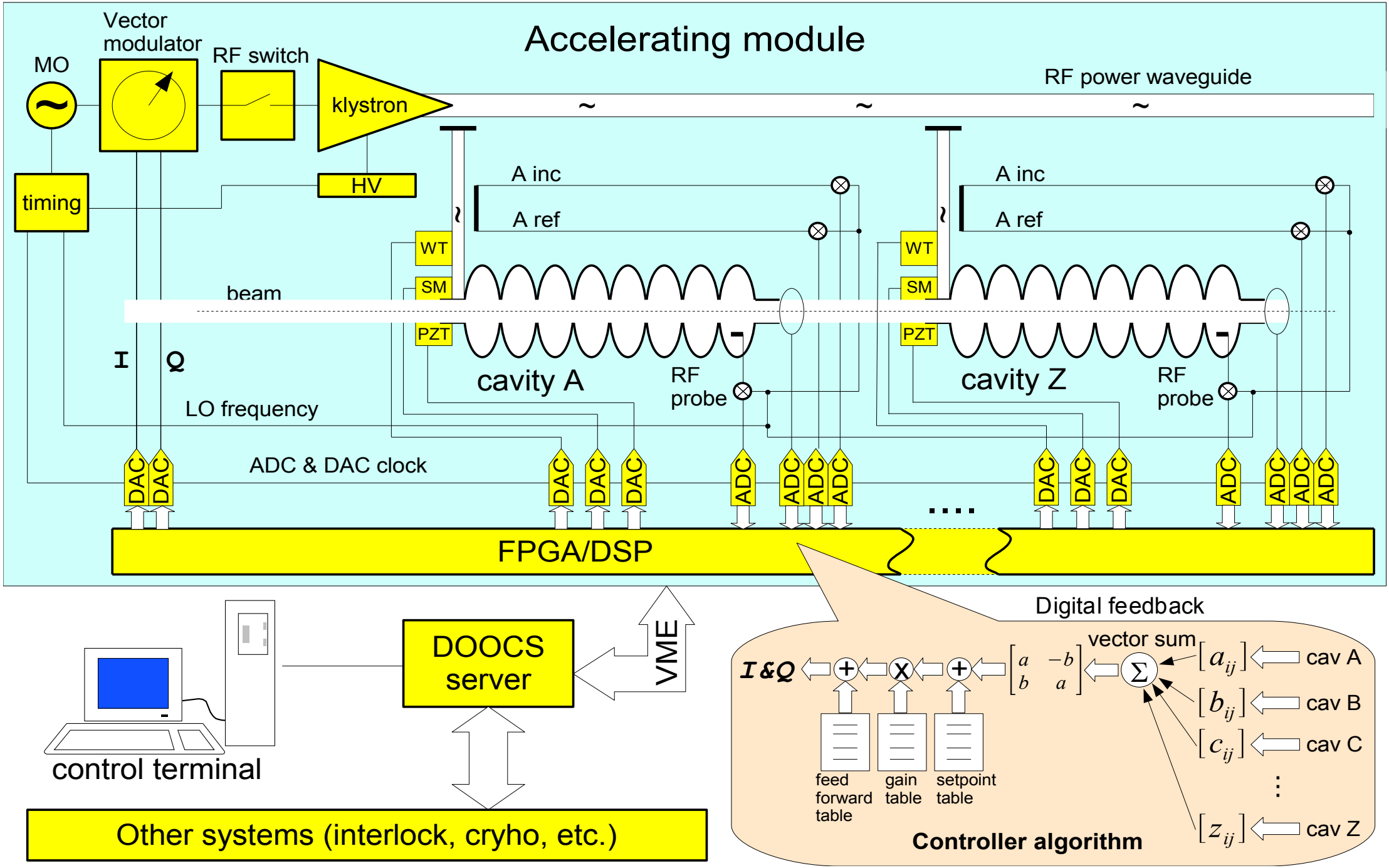
- 700MeV (12.5nm), after upgrade 1GeV (6nm)
- User experiments started in June 2005
- Test facility for technology development

# FLASH


RF gun
Diagnostics
Accelerating Structures
Collimator
Undulators
Laser
Bunch Compressor
Bunch Compressor
5 MeV
127 MeV
370 MeV
700 MeV
Bypass
250 m


ACC 6
ACC 5
ACC 4
ACC 3
ACC 2
ACC 1
RF-Gun
new, XFEL-type
RF power distribution
Kly 4 (10 MW)
Kly 5 (5 MW)
Kly 2 (5 MW)
Kly 3 (5 MW)

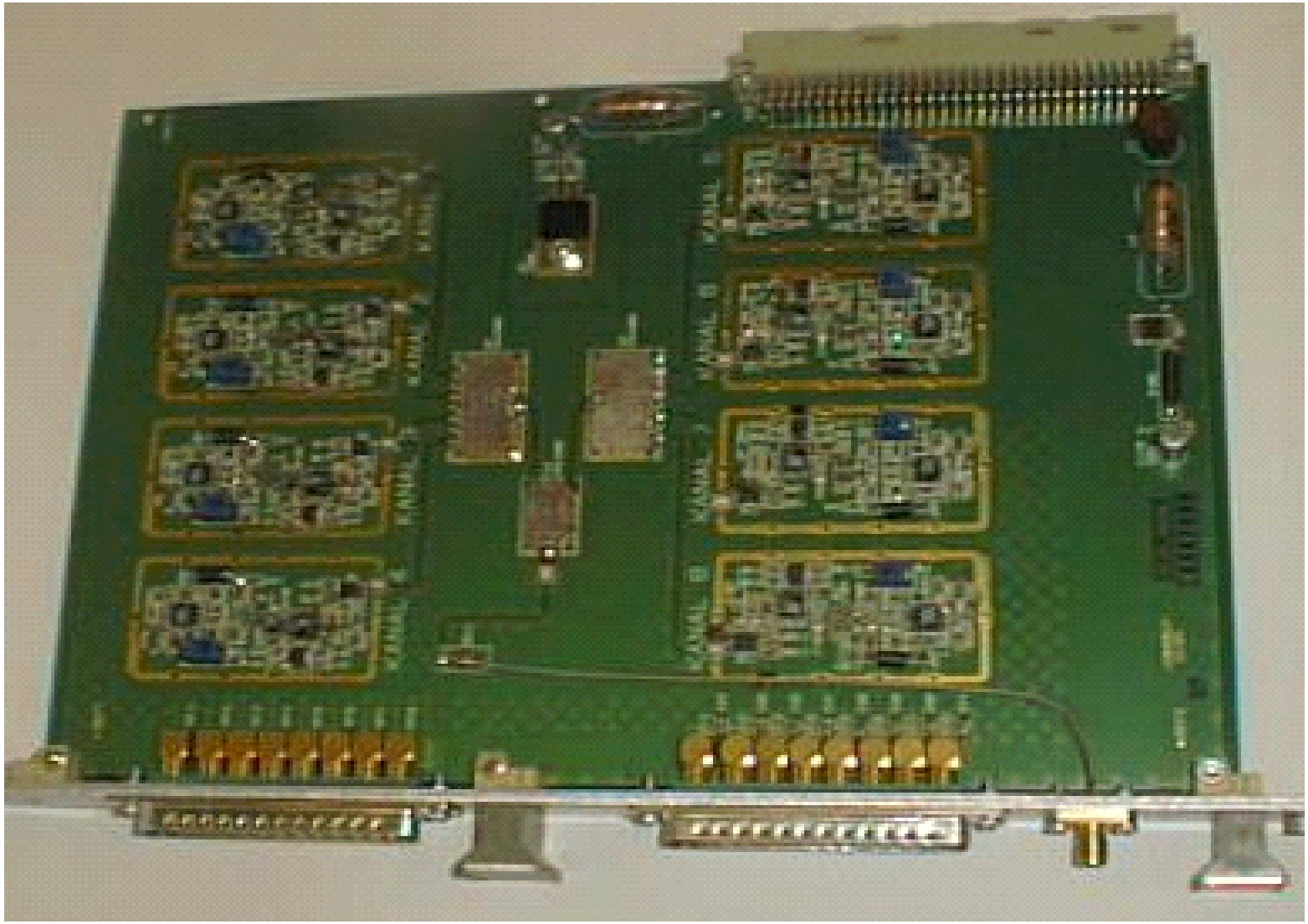
# LLRF system in FLASH



# FLASH LLRF station

- Several tens of analogue inputs 1.3 GHz, 0dBm
  - Down-conversion required
  - System latency < 1µs
  - Synchronized with MO
- RF drive output
- Low latency communication to other modules (500 µs)
  - Piezo driver
  - ...
- Communication to other systems
  - Waveguide tuners
  - ...
- System must be reliable, easy operable, robust...

# FLASH LLRF station (current state)

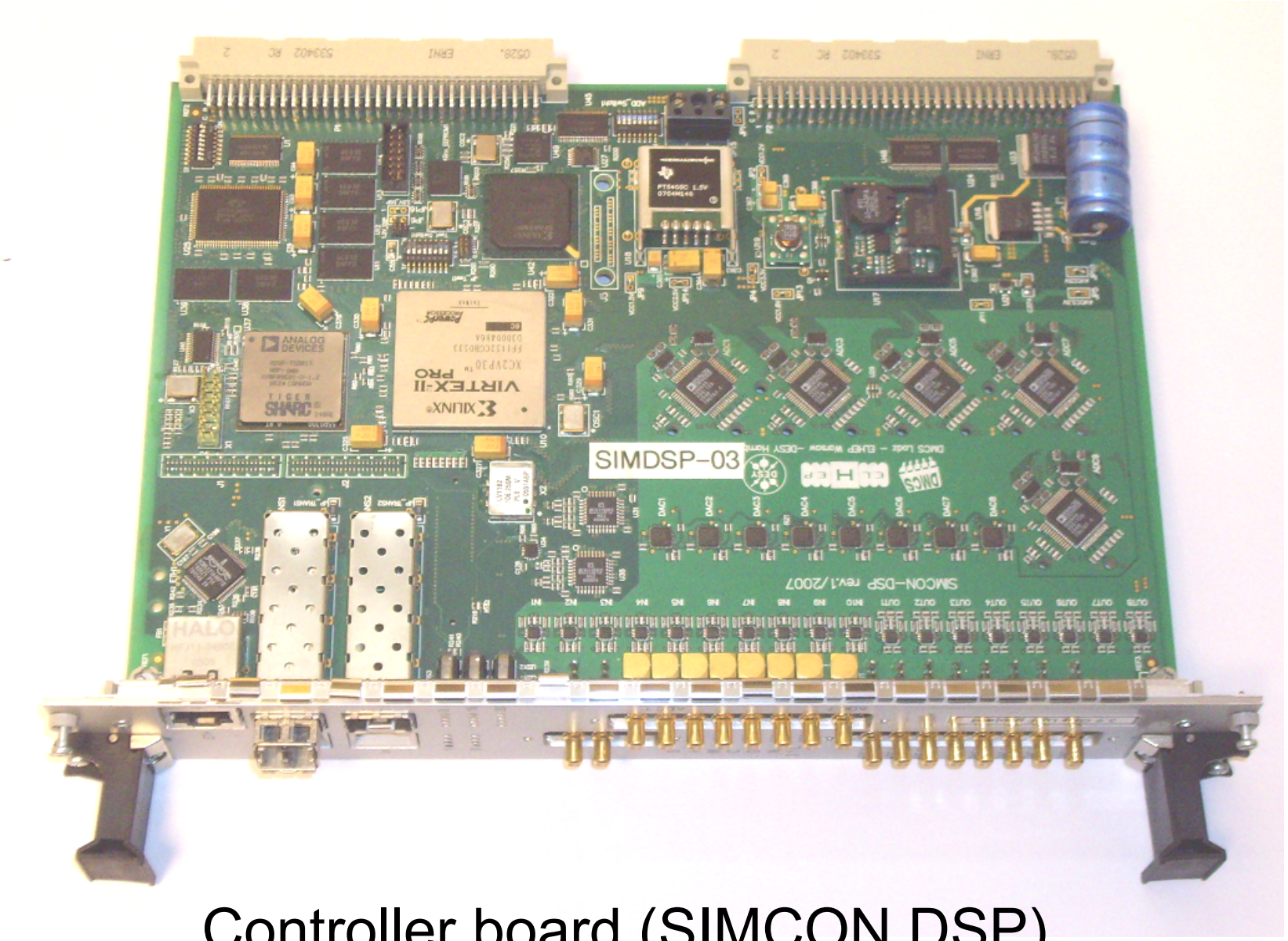


Downconverter board (IF=250kHz)

# FLASH LLRF station (current state)

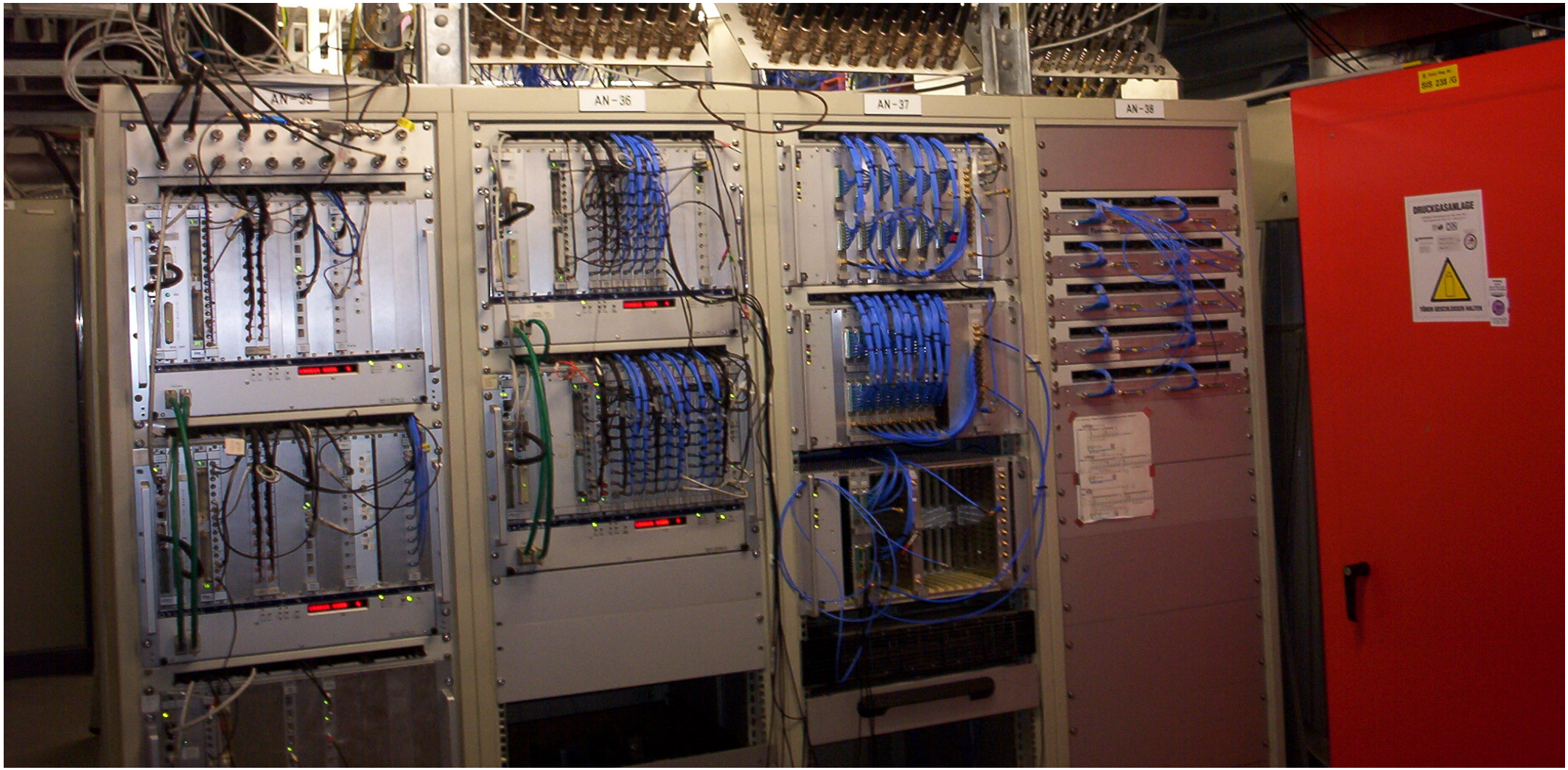
DSP C67 board

# FLASH LLRF station (current state)




Controller board (SIMCON DSP)

# FLASH LLRF station (current state)




System racks (VME)

# Why we need LLRF upgrade at FLASH (1)

The present LLRF control system at FLASH will satisfy user needs for the next 1-2 years but does not fulfill the long term (3-10 years) requirements in the following areas:

1. Field regulation

- The long term phase drifts especially in the injector section are to large (few ps/day). The proposed calibration scheme of the downconverters using the laser master oscillator will improve this stability by about one order of magnitude.
- The short term stability will also need some improvement (especially for the 3rd harmonics cavities) which can be achieved with a high IF/ clock scheme which is planned ot be implemented in the ATCA system. The present DSP systems clock rate is limited to 1 MHz.
- The vector sum calibration requires improvement which can be achieved with the combination of high IF/clock and power signal processing not available in the present DSP system.

# Why we need LLRF upgrade at FLASH (2)

2. Availability

- The ATCA concept is optimized for high availability.
- Significant diagnostics are required to support exception handling which will improve up-time. These algorithm cannot be implemented in the current DSP system
- Cables defects are one of the main problems. With the new ATCA concept with cabling from the rear side, a significant improvement is expected.

3. Maintenance

- The very limited resources require similar standards to be used for FLASH and XFEL. An ATCA based system will reduce resources required for maintenance.

4. Operability

- FLASH will require at higher degree of automation in the coming 2-3 years (~2010) to simplify changes in operating parameters (availability, performance, manpower) and guarantee high performance faster changing operational parameters. The ATCA based LLRF system can provide the necessary functionality which will be available at the XFEL after a few years of operation (~2015).

# Project history (shortly)

- Very ambitious first version, but...
- Budget reduction necessary
- Trials to cut down the required resources without significant scope reduction
- Limited scope of the project but not in scale with budget reduction
  - wide usage of students work supervised by experts

# Goal of FP7 LLRF for FLASH

The goal of the project is to advance RF Control Technology in the areas of hardware and software and to test developed solutions in FLASH accelerator:

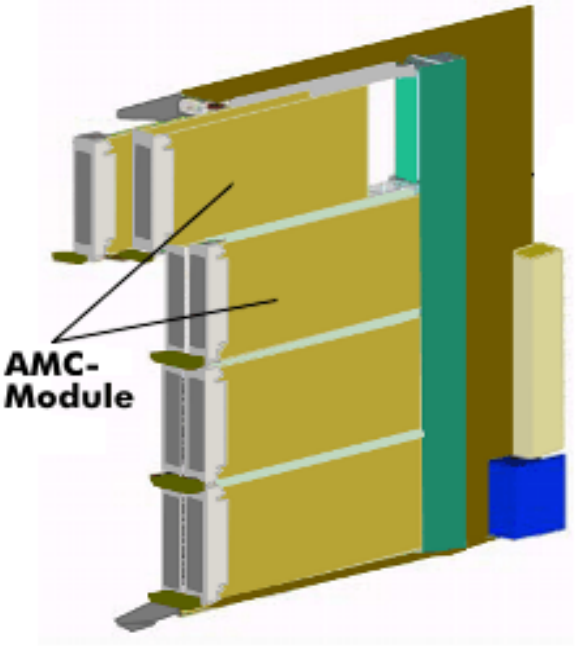
- develop LLRF implementation as HA ATCA System with required fast and ultra fast analogue and digital IO
- develop new frequency conversion and multi-channel ASIC version of downconverter
- develop radiation monitoring (based on customized ASIC and standard components)
- develop other necessary control systems (piezo, waveguide) and integrate them with ATCA based LLRF system
- improve technical performance
- optimize reliability availability
- reduce cost

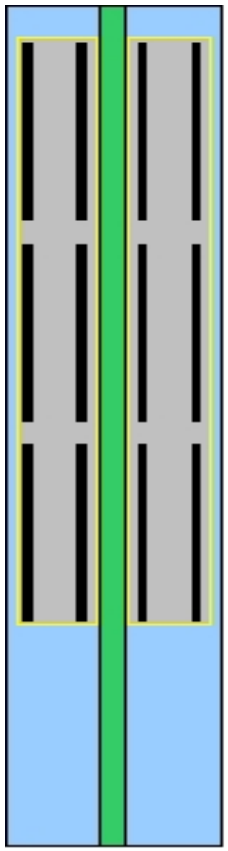
AdvancedTCA®

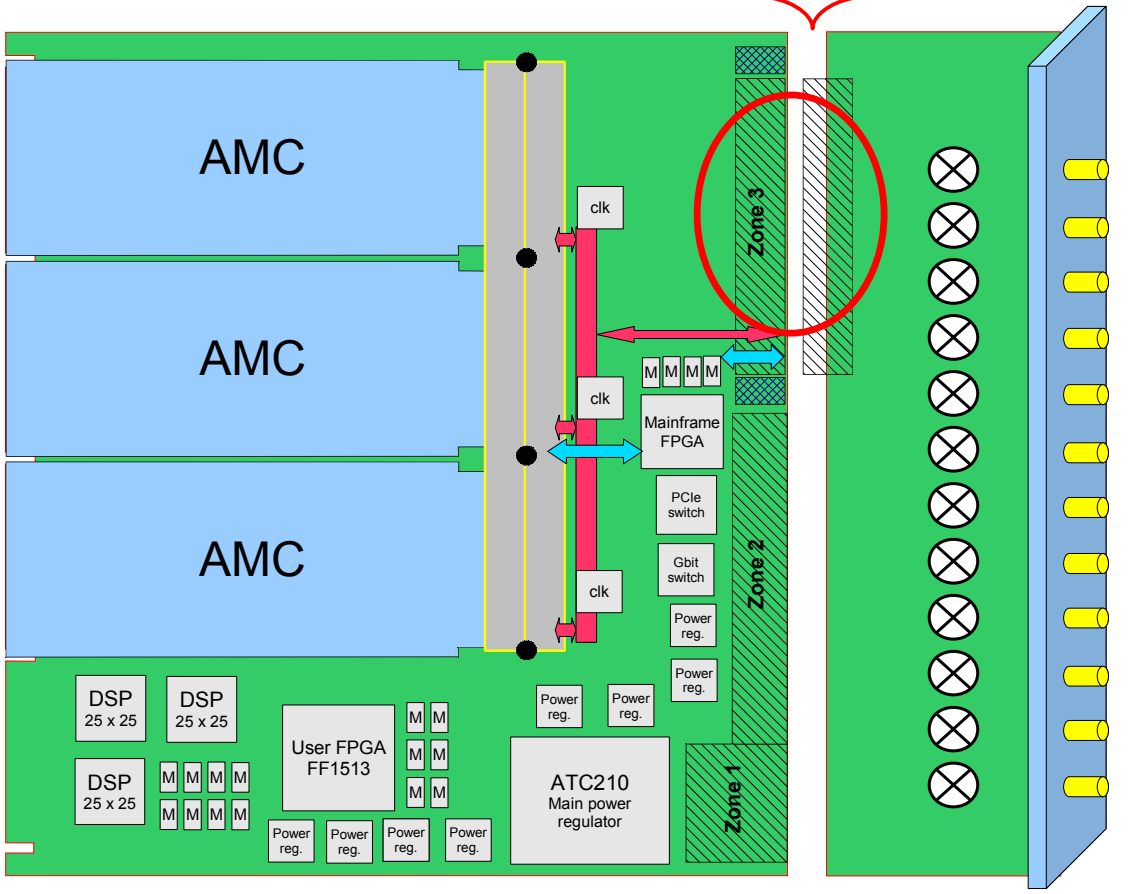
# Task 1 Development of ATCA carrier boards with FPGA, DSP

- Carries customized AMC modules
- Provides processing power and communication between system components
- Carries RF analogue signals
- Distributes timing and frequency reference signals

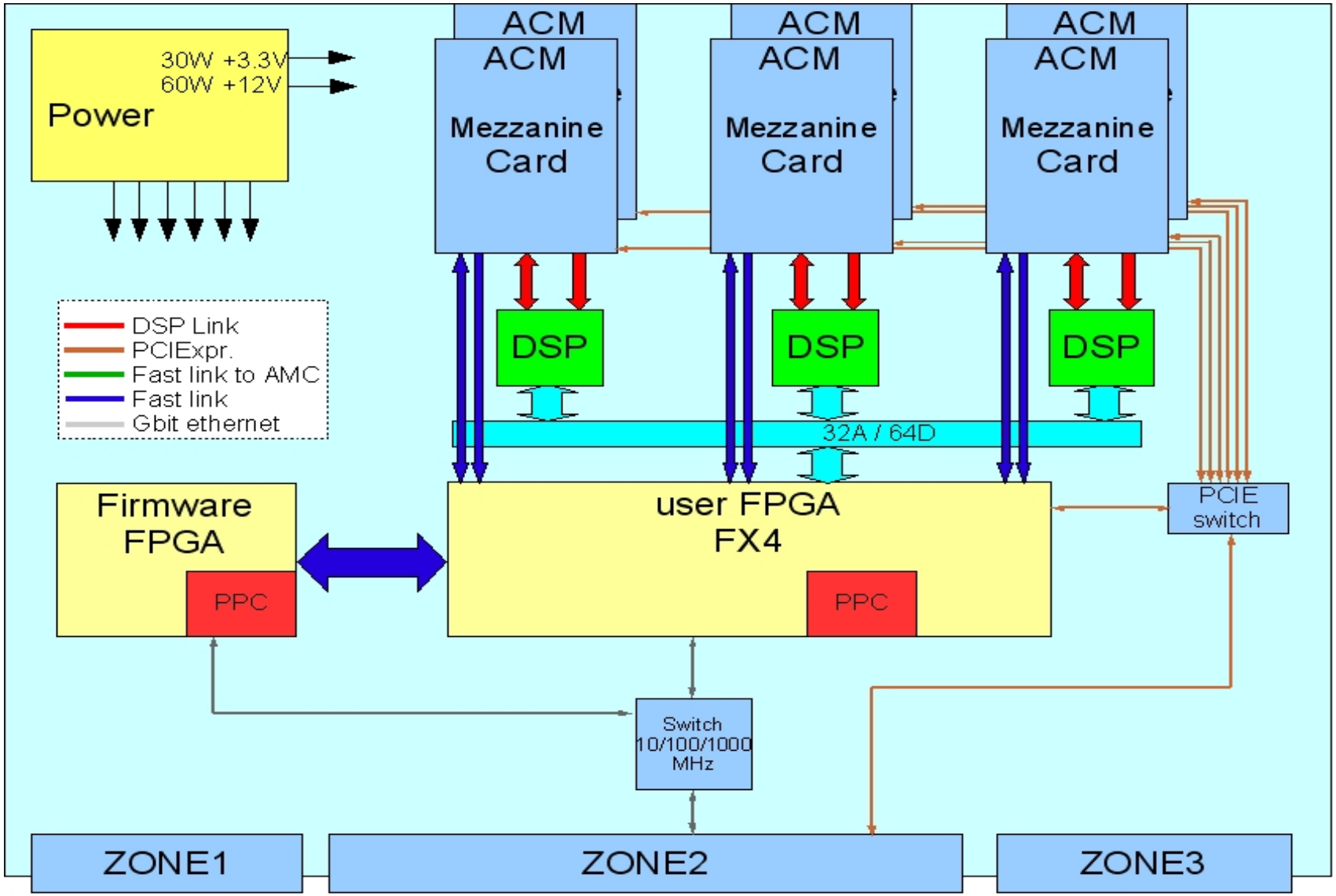
# Task 1 Development of ATCA carrier boards with FPGA, DSP

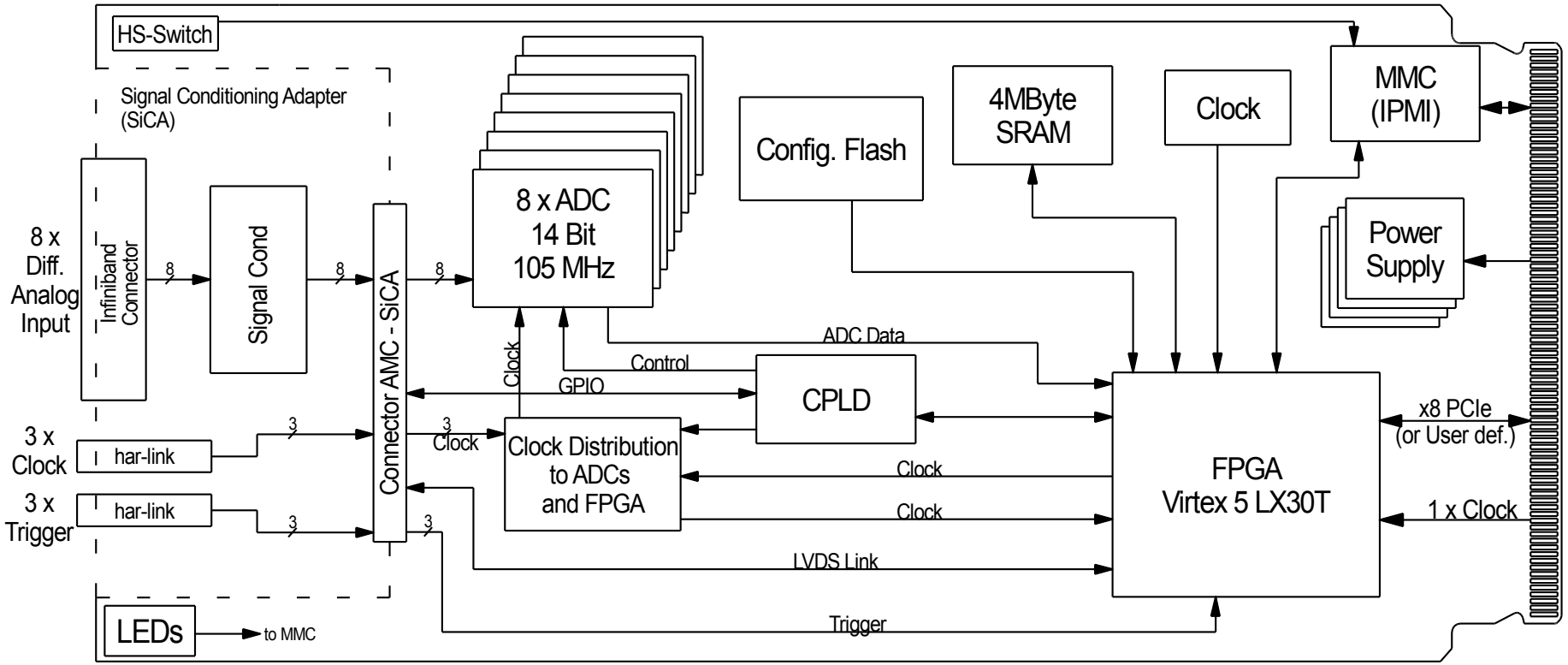


# Task 1 Development of ATCA carrier boards with FPGA, DSP



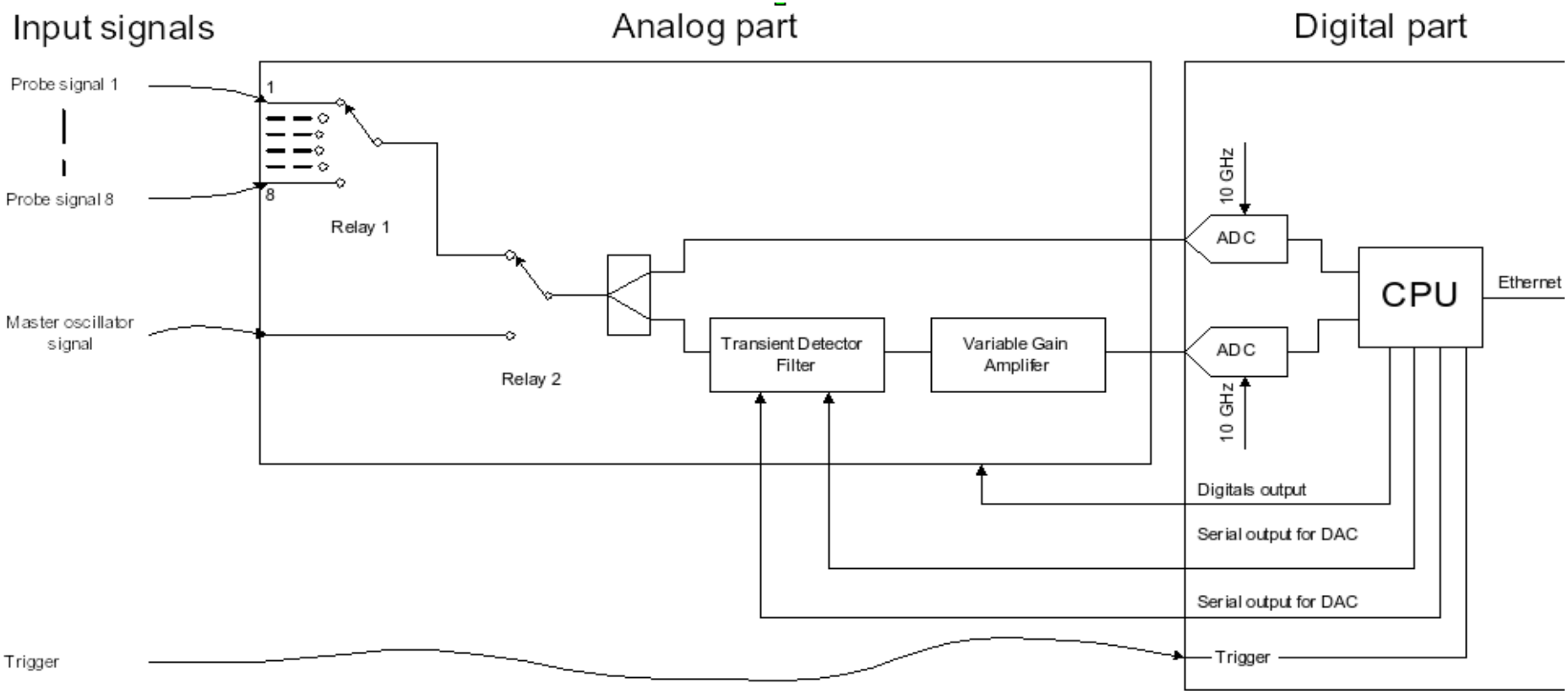
# Task 2 Development of AMC modules with fast analog and digital IO

- Provides the basic input/output functionality for field regulation (at least 14b, 100MHz)



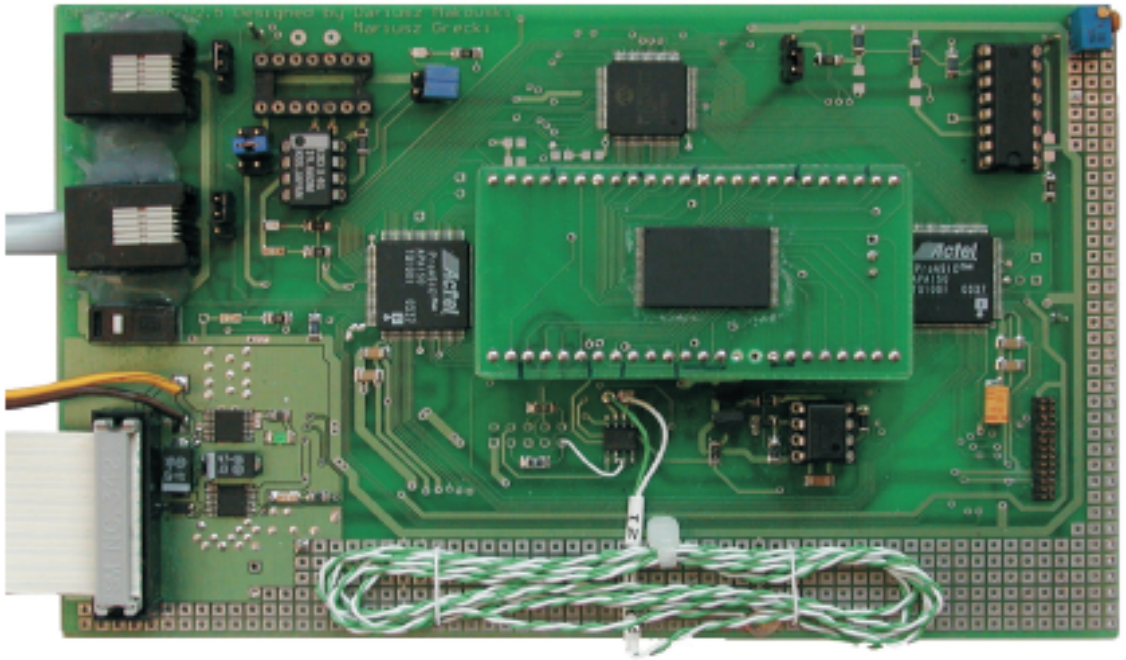
# Task 3 Development of AMC modules with ultra fast analog IO

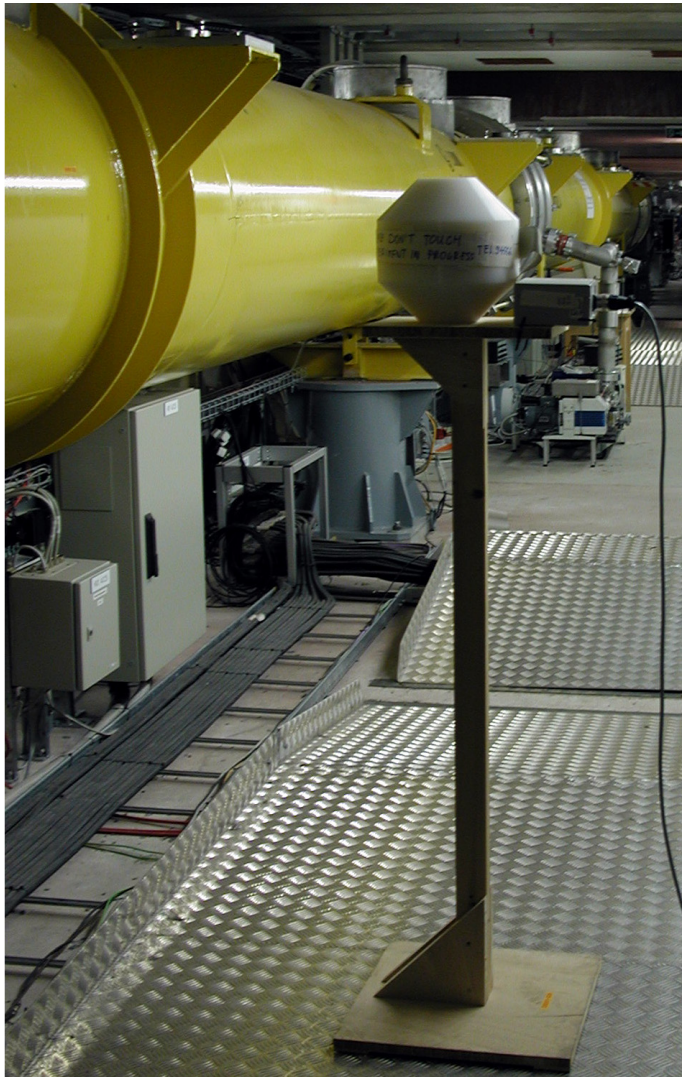
- Provides the very fast analogue input (at least 2GHz, 10b) for special purposes (direct sampling, transient detection, HOM measurements, etc.)



# Task 4 Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs)

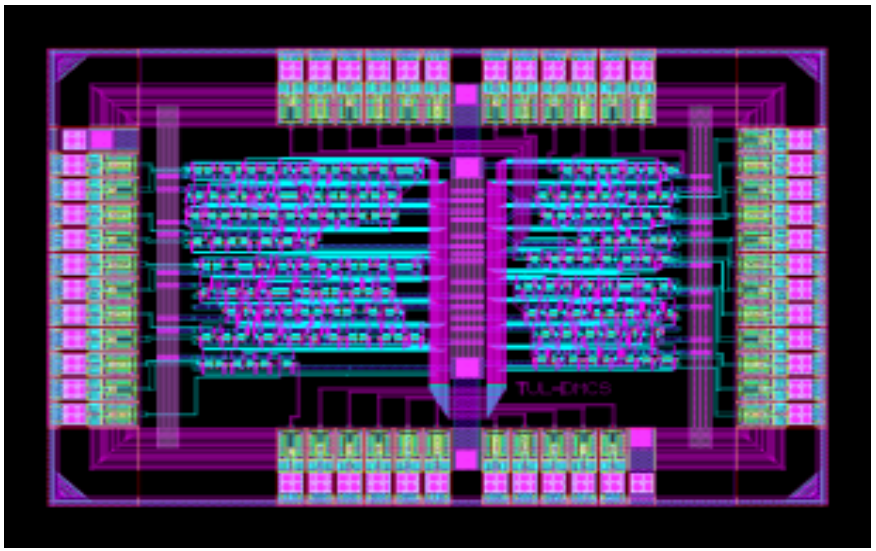
Provides real time radiation monitoring for diagnostics and momentum management

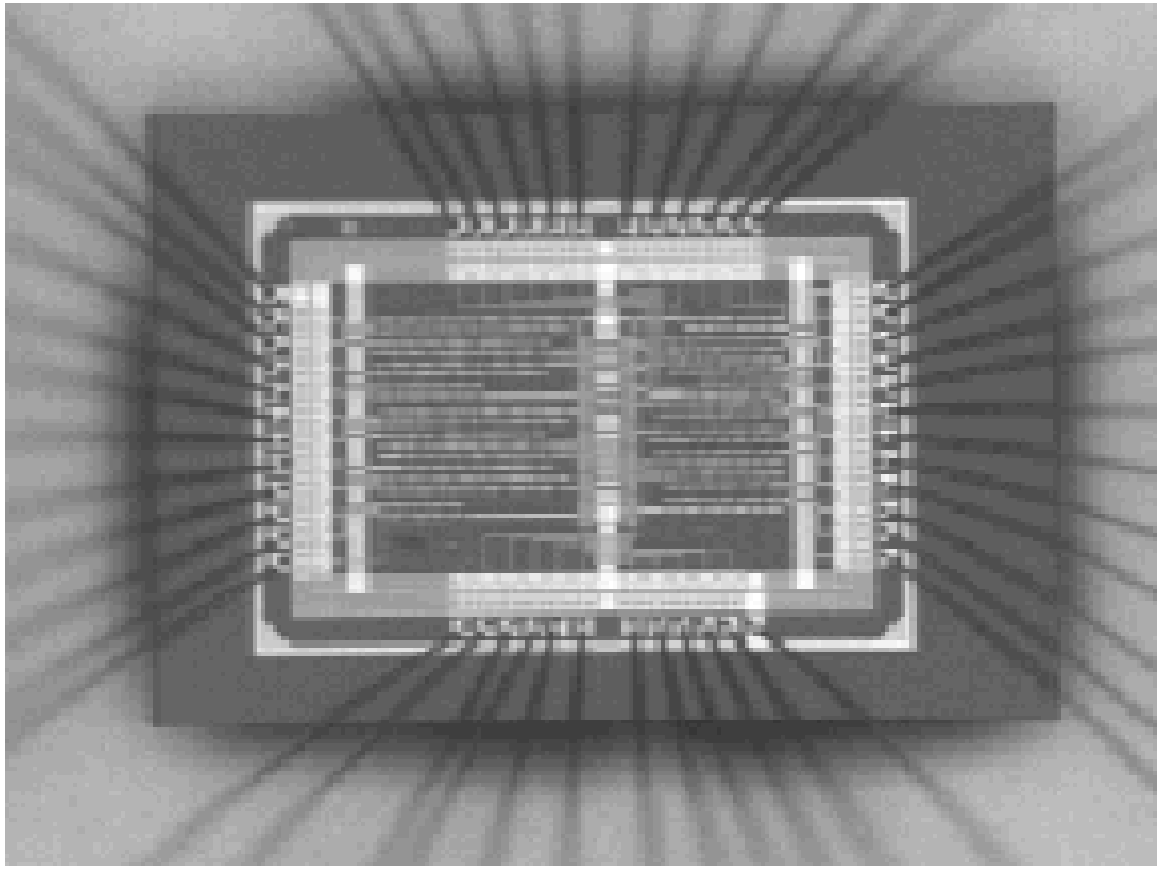




# Task 4 Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs)

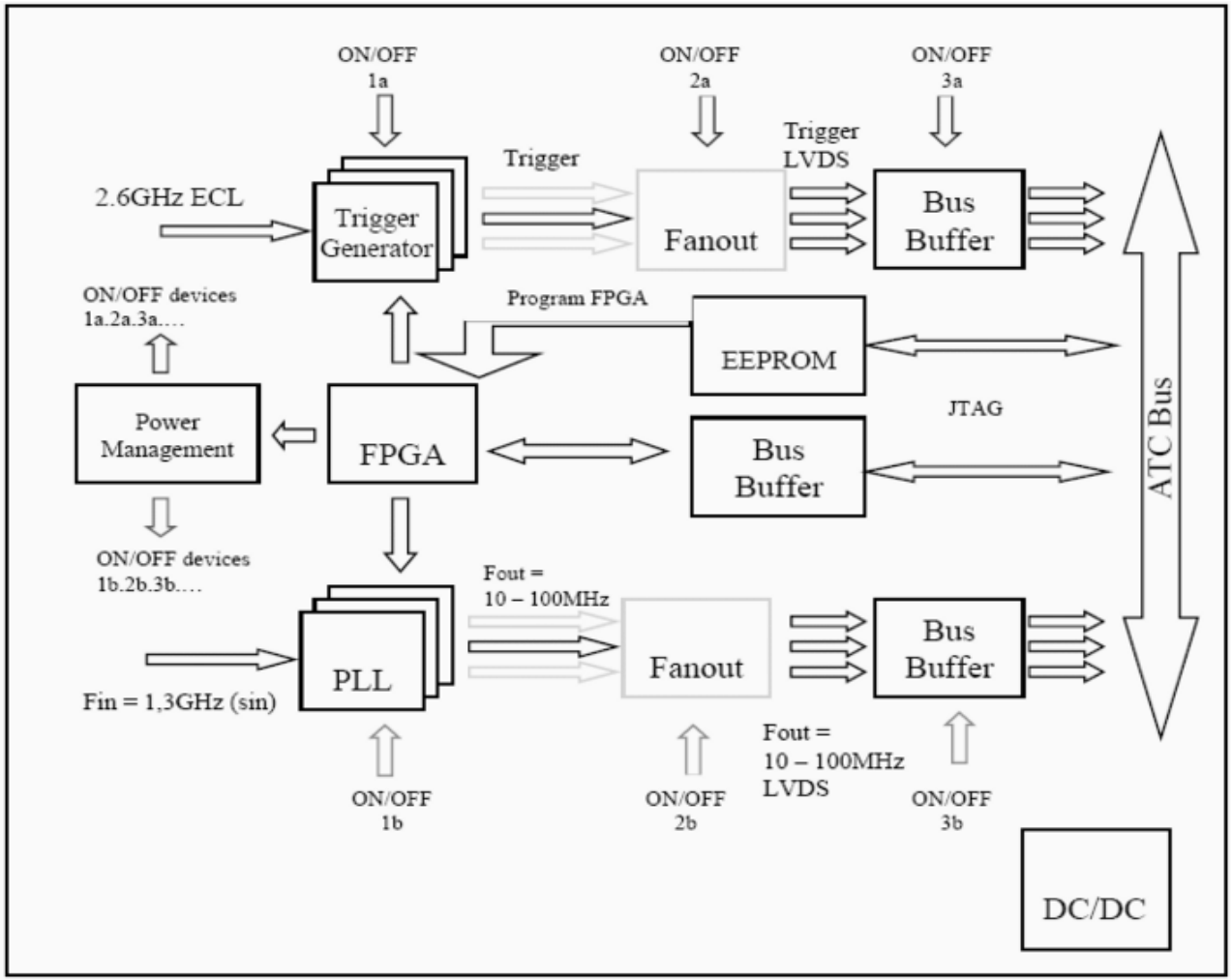
Development of specialized SRAM based neutron detector is needed





# Task 5 Development of reference, clock and timing distribution for ATCA based LLRF

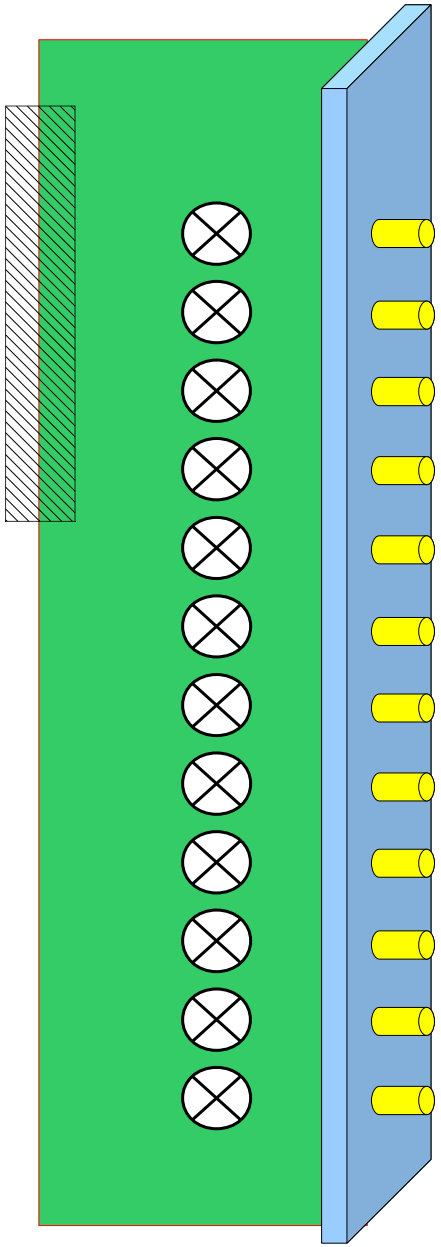
- One of the problem in FLASH is a long term phase drifts, especially in the injector section
- Reference signals for downconverters are needed to reduce drifts. They must be distributed over the LLRF system.
- Also timing signals (clocks and event triggers) must be generated from reference

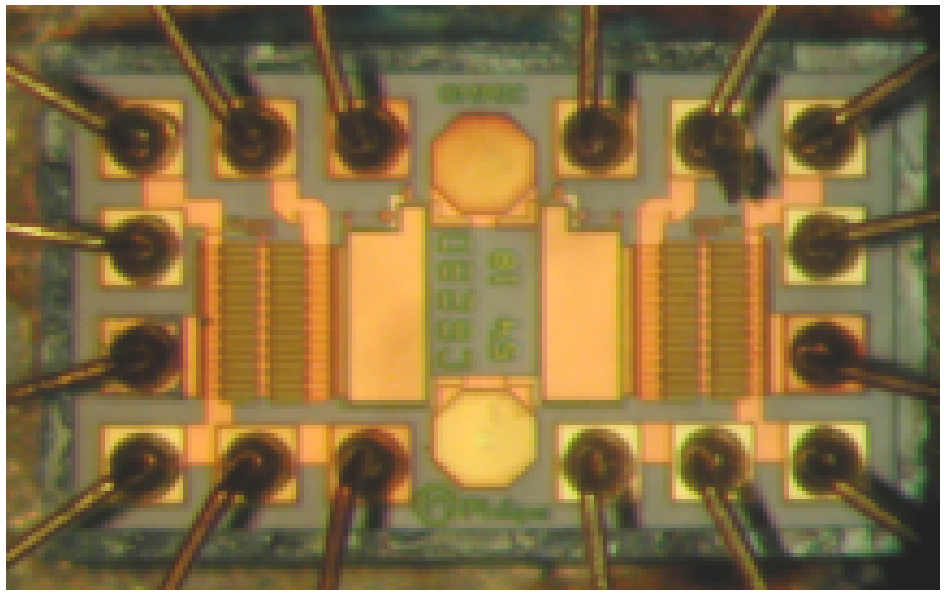


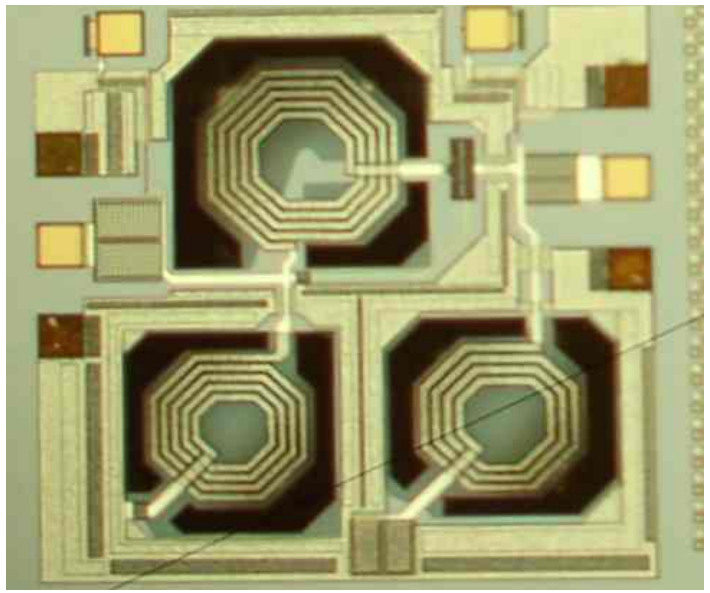
# Task 6 Development of AMC/RTM module for downconverters and upconverters

The main goal of this task is to test various solutions of down- and upconversion (including building specialized ASICs) to and to develop RTM (or AMC) modules with down- and upconverters.

It is expected that higher IF than it is used nowadays will improve stability and signal/noise ratio.

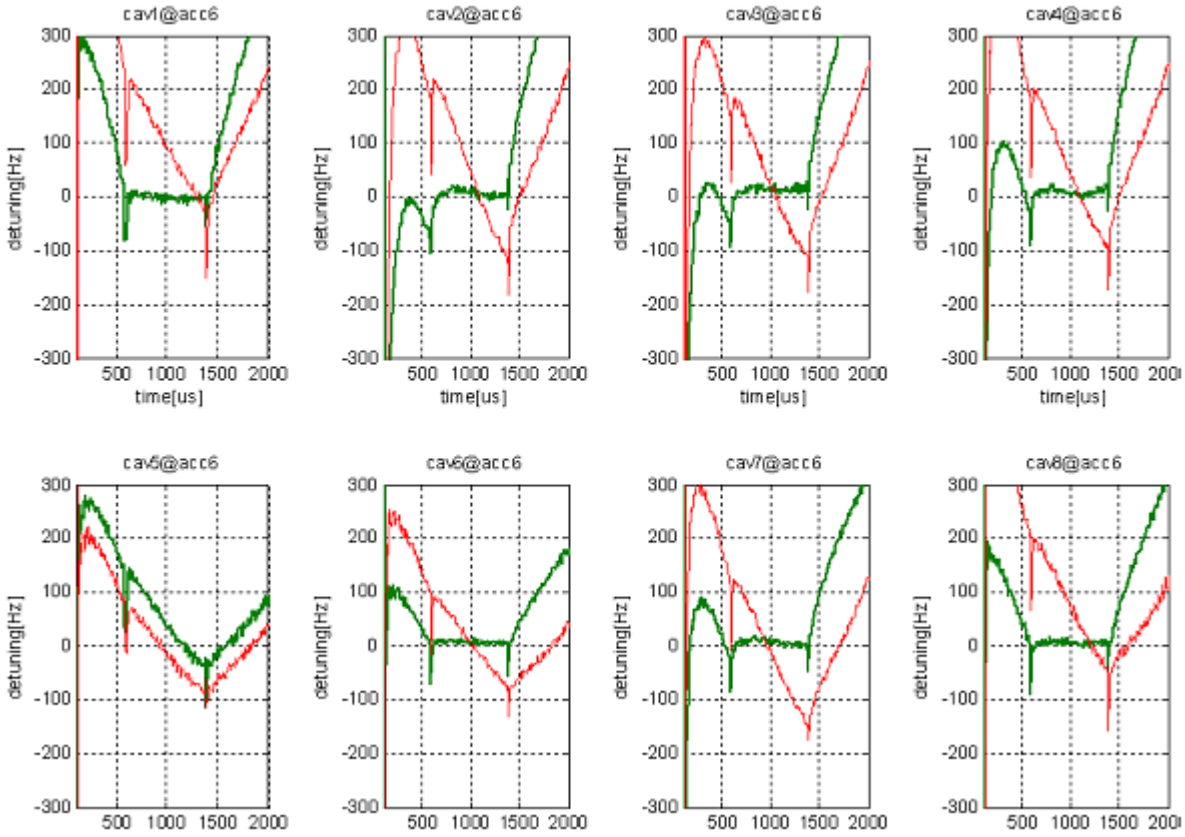


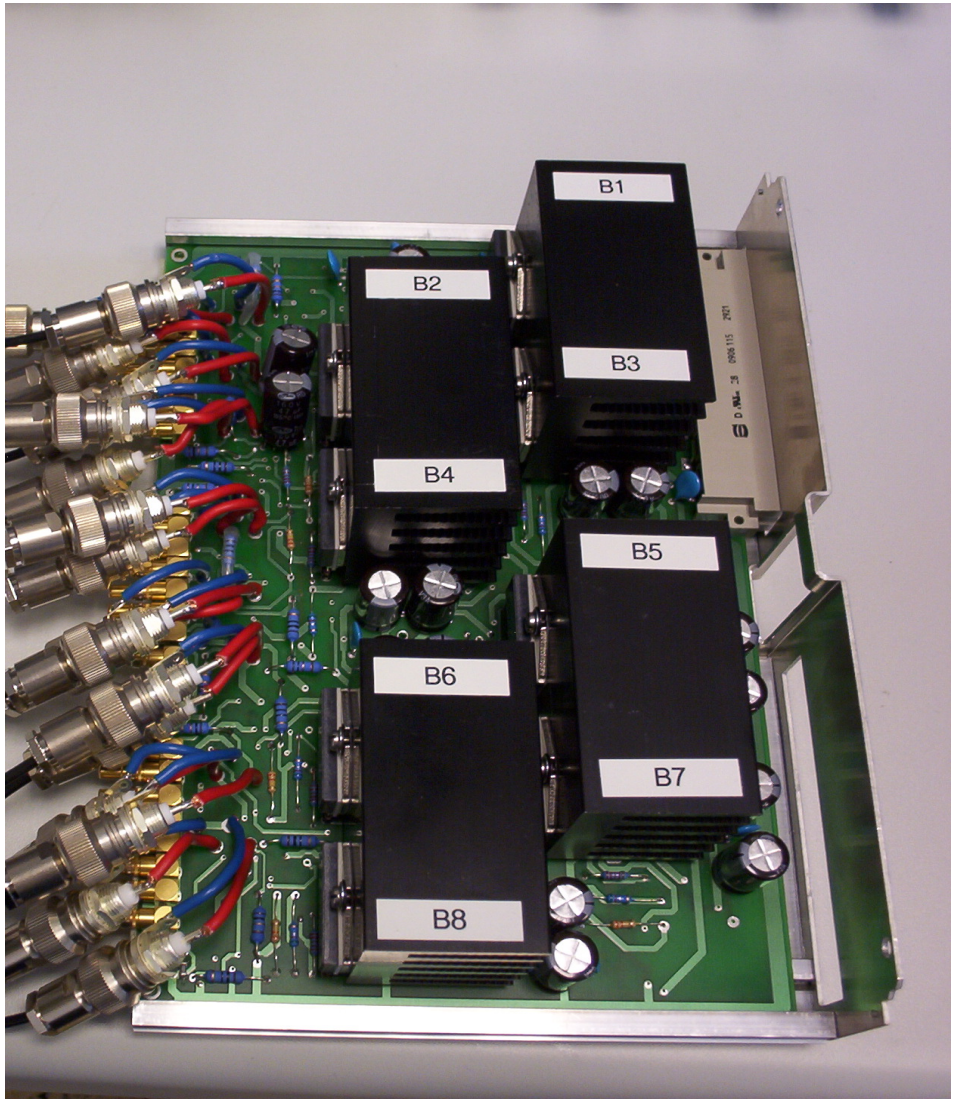




# Task 7 ATCA based implementation of cavity tuners & waveguide control

Other control system also have to be integrated with ATCA based LLRF system



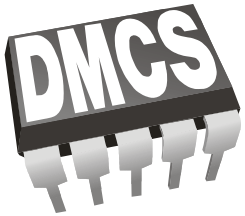
# Task 8 Development of beam based longitudinal feedbacks for the ATCA based LLRF system

The goal of this task is to explore the possibility to build up beam based feedbacks and test a prototype at FLASH. The diagnostic devices (measuring longitudinal beam parameters like beam energy, bunch arrival etc.) will be connected by developed interfaces to ATCA based LLRF system and fast low level algorithms to extract relevant correction parameters will be implemented. The corrections will be then fed back to the LLRF system within a bunch train.

# Institutions

Coordination: S.Simrock, DESY


DESY Deutsches Elektronen-Synchrotron, Hamburg, Germany




DMCS Department of Microelectronics and Computer Science, Technical University of Lodz, Poland


ISE Institute of Electronic Systems, Warsaw University of Technology, Poland

INP Niewodniczanski Institute of Nuclear Physics, Krakow, Poland


INP Institute for Nuclear Studies, Swierk, Poland

# Project budget (1)

| | | person-months | hardware [kE] | travel [kE] |
|---|---|---|---|---|
| 1 | Development of ATCA carrier boards with FPGA, DSP | 16 | 44 | 11 |
| 2 | Development of AMC modules with fast analog IO and digital IO | 9 | 35 | 8 |
| 3 | Development of ultra fast analog IO (2 Gs, 10 bit) | 10 | 20 | 5 |
| 4 | Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs) | 13 | 78.5 | 5 |
| 5 | Development of reference, clock and timing distribution for ATCA | 20 | 80 | 8 |
| 6 | Development of AMC/RTM module for downconverters and upconverters | 17 | 50 | 8 |
| 7 | ATCA implementation of piezo & waveguide | 13 | 40 | 11 |
| 8 | Development of beam based longitudinal feedbacks for the ATCA based LLRF system. | 22 | 40 | 10 |
| | Total | 120 | 387.5 | 66 |

# Project budget (2)

| | | DESY | DMCS | ISE | INP | INP PAN |
|---|---|---|---|---|---|---|
| 1 | Development of ATCA carrier boards with FPGA, | 82.6 | 45 | 0 | 0 | 0 |
| 2 | Development of AMC modules with fast analog IO and digital IO | 34.4 | 33.125 | 8 | 0 | 0 |
| 3 | Development of ultra fast analog IO (2 Gs, 10 bit) | 24.4 | 36 | 0 | 0 | 0 |
| 4 | Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs) | 39.1 | 91.75 | 0 | 0 | 0 |
| 5 | Development of reference, clock and timing distribution for ATCA | 82.6 | 0 | 89.5 | 0 | 0 |
| 6 | Development of AMC/RTM module for downconverters and upconverters | 66.4 | 0 | 63.75 | 0 | 0 |
| 7 | ATCA implementation of piezo & waveguide control | 22 | 28.375 | 0 | 38 | 0 |
| 8 | Development of beam based longitudinal feedbacks for the ATCA based LLRF system. | 43 | 0 | 0 | 0 | 86.875 |
| | Total | 394.5 | 234.25 | 161.25 | 38 | 86.875 |

# Project budget (3)

1st year personel

| | DESY | DMCS | ISE | INP (krakow | INP PAN(Swi | total |
|---|---|---|---|---|---|---|
| 1 | 4 | | 6 | | | 10 |
| 2 | 2 | | 5 | | | 7 |
| 3 | 2 | | 4 | | | 6 |
| 4 | 3 | | 7 | | | 10 |
| 5 | 5 | | | 6 | | 11 |
| 6 | 3 | | | 6 | | 9 |
| 7 | | | 3 | | 5 | 8 |
| 8 | 3 | | | | 10 | 13 |
| | 22 | | 25 | 12 | 5 | 10 |

hardware

| DESY | DMCS | ISE | INP | INP PAN | total |
|---|---|---|---|---|---|
| 18 | 10 | | | | 28 |
| 10 | 6 | 3 | | | 19 |
| 7 | 6 | | | | 13 |
| 5,5 | 25 | | | | 30,5 |
| 15 | | 40 | | | 55 |
| 10 | | 20 | | | 30 |
| 10 | 6 | | 6 | | 22 |
| | | | | 20 | 20 |
| 75,5 | 53 | 63 | 6 | 20 | |

travel

| DESY | DMCS | ISE | INP | 0 | total |
|---|---|---|---|---|---|
| 2 | 5 | | | | 7 |
| 1 | 2 | 2 | | | 5 |
| 1 | 2 | | | | 3 |
| 1 | 2 | | | | 3 |
| 2 | | 3 | | | 5 |
| 2 | | 3 | | | 5 |
| 1 | 2 | | 3 | | 6 |
| 1 | | | | 5 | 6 |
| 11 | 13 | 8 | 3 | 5 | |

2nd year personel

| | DESY | DMCS | ISE | INP (krakow | INP PAN(Swi | total |
|---|---|---|---|---|---|---|
| 1 | 4 | | 2 | | | 6 |
| 2 | | | 2 | | | 2 |
| 3 | | | 4 | | | 4 |
| 4 | | | 3 | | | 3 |
| 5 | 3 | | | 6 | | 9 |
| 6 | 4 | | | 4 | | 8 |
| 7 | | | 2 | | 3 | 5 |
| 8 | 2 | | | | 7 | 9 |
| | 13 | | 13 | 10 | 3 | 0 |

hardware

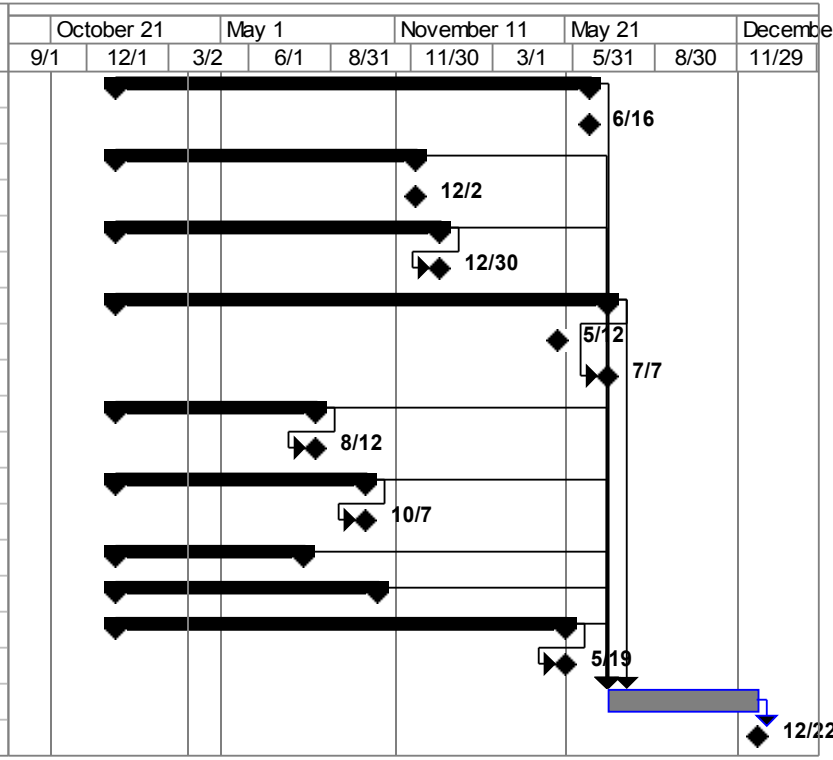
| DESY | DMCS | ISE | INP | INP PAN | total |
|---|---|---|---|---|---|
| 12 | 4 | | | | 16 |
| 10 | 4 | 2 | | | 16 |
| 3 | 4 | | | | 7 |
| 13 | 35 | | | | 48 |
| 5 | | 20 | | | 25 |
| 10 | | 10 | | | 20 |
| 10 | 4 | | 4 | | 18 |
| | | | | 10 | 20 |
| 73 | 51 | 32 | 4 | 0 | |

travel

| DESY | DMCS | ISE | INP | INP PAN | total |
|---|---|---|---|---|---|
| 1 | 3 | | | | 4 |
| 1 | 1 | 1 | | | 3 |
| 1 | 1 | | | | 2 |
| 1 | 1 | | | | 2 |
| 1 | | 2 | | | 3 |
| 1 | | 2 | | | 3 |
| 1 | 2 | | 2 | | 5 |
| 1 | | | | 3 | 4 |
| 8 | 8 | 5 | 2 | 0 | |

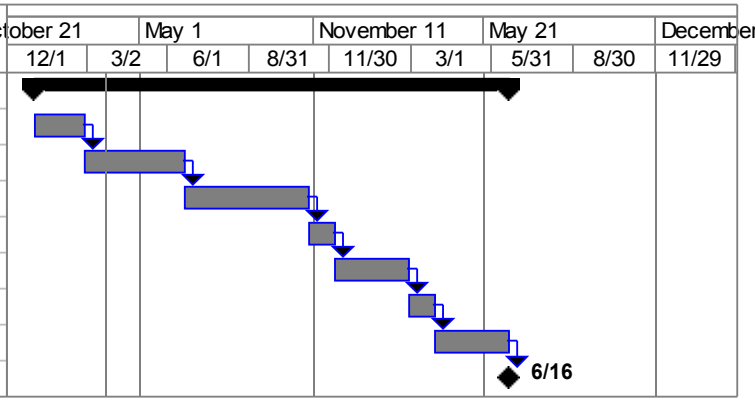
# Gantt chart of the project (1)

| ID | Task Name |
|---|---|
| 1 | **Development of ATCA carrier boards with FPGA, DSP** |
| 9 | Design and manufacturing of the carrier board prototypes. |
| 10 | **Development of AMC modules with fast analog IO and digital IO** |
| 18 | Design and manufacturing of the AMC modules with fast analogue and digital IO (at least 100 Ms/s, 14 b). |
| 19 | **Design and manufacturing of the AMC board with ultra fast ADC (at least 2 Gs/s, 10 b)** |
| 27 | Development of ultra fast analog IO (2 Gs, 10 bit) |
| 28 | **Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs)** |
| 46 | Design and manufacturing of AMC radiation dosimeter |
| 47 | Report on tests and calibration of the radiation dosimeter |
| 48 | **Development of reference, clock and timing distribution for ATCA** |
| 55 | Designed and manufactured Frequency Synthesizer Board (AMC) |
| 56 | **Development of AMC/RTM module for downconverters and upconverters** |
| 63 | Integration of downconverters and upconverters in RTM (ATCA) |
| 64 | **ATCA implementation of piezo & waveguide control** |
| 72 | **Design and fabrication of AMC modules for controlling step motors, piezo and waveguide tuners** |
| 80 | **Development of beam based longitudinal feedbacks for the ATCA based LLRF system.** |
| 86 | Report on longitudinal beam parameter studies and their controllability by fast feedback systems in conjunction with the LLRF system |
| 87 | System tests |
| 88 | Report on system test and and performance |

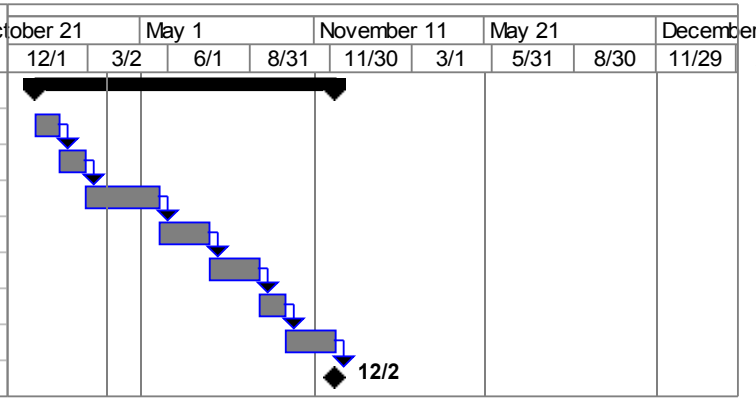


# Gantt chart of the project (2)

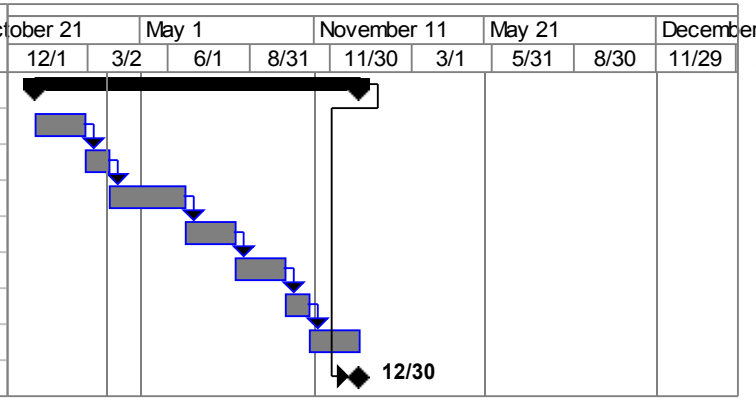
| ID | Task Name |
|---|---|
| 1 | **Development of ATCA carrier boards with FPGA, DSP** |
| 2 | Requirements analysis and capture |
| 3 | Schematic desig |
| 4 | PCB design |
| 5 | Prototype fabrication |
| 6 | Debugging |
| 7 | Schematic and PCB modifications |
| 8 | Fabrication of final boards |
| 9 | Design and manufacturing of the carrier board prototypes. |




| ID | Task Name |
|---|---|
| 10 | **Development of AMC modules with fast analog IO and digital IO** |
| 11 | Requirements analysis and capture |
| 12 | Schematic desig |
| 13 | PCB design |
| 14 | Prototype fabrication |
| 15 | Debugging |
| 16 | Schematic and PCB modifications |
| 17 | Fabrication of final boards |
| 18 | Design and manufacturing of the AMC modules with fast analogue and digital IO (at least 100 Ms/s, 14 b). |

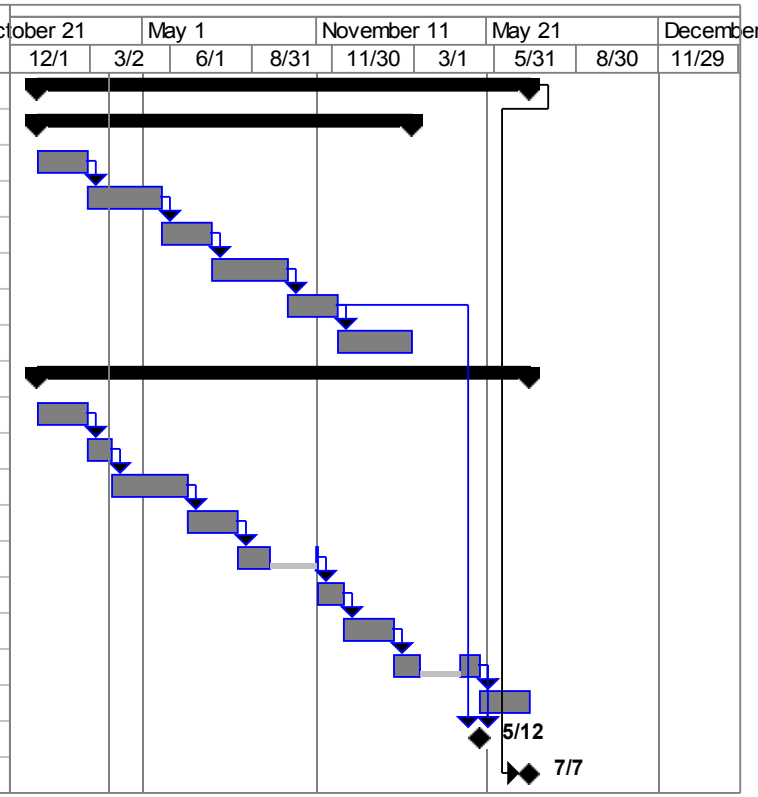



| ID | Task Name |
|---|---|
| 19 | **Design and manufacturing of the AMC board with ultra fast ADC (at least 2 Gs/s, 10 b)** |
| 20 | Requirements capture |
| 21 | Schematic desig |
| 22 | PCB design |
| 23 | Prototype fabrication |
| 24 | Debugging |
| 25 | Schematic and PCB modifications |
| 26 | Fabrication of final boards |
| 27 | Development of ultra fast analog IO (2 Gs, 10 bit) |

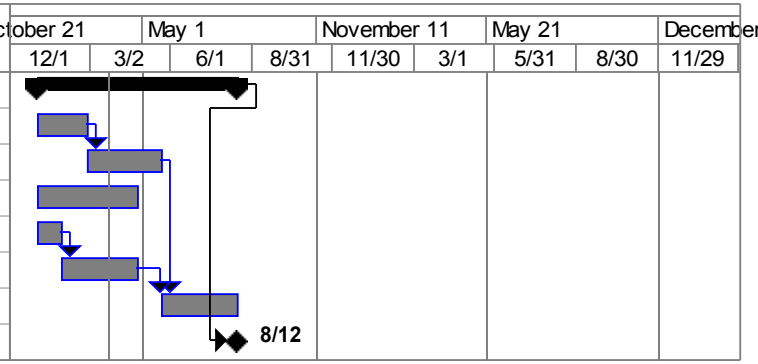


# Gantt chart of the project (3)

| ID | Task Name |
|---|---|
| 28 | **Development of AMC module with radiation sensors (gamma and neutron detector with customized ASICs)** |
| 29 | **Gamma detector board** |
| 30 | Study and comparison of available gamma dosimeters |
| 31 | Design and fabrication of prototype board for initial tests of dosimeters |
| 32 | Radiation sensitivity tests of selected gamma dosimeters |
| 33 | Design of detector board |
| 34 | Fabrication of detector board |
| 35 | Tests and calibration of gamma dosimeter |
| 36 | **Neutron detector board** |
| 37 | Study, comparison and simulation of various radiation sensitive SRAM cells |
| 38 | Selection of optimum radiation-sensitive cells for the neutron dosimeter array |
| 39 | Design of a test integrated circuit ASIC 1 |
| 40 | Design and fabrication of a prototype board for initial tests of dosimeters |
| 41 | Fabrication of the test integrated circuit ASIC 1 in the silicon foundry |
| 42 | Tests in the radiation environment and selection of final cells and the detector structure |
| 43 | Design of the final integrated circuit ASIC 2 of the neutron fluence dosimeter |
| 44 | Fabrication of the final integrated circuit ASIC 2 in silicon foundry |
| 45 | Tests and calibration of the neutron dosimeter |
| 46 | Design and manufacturing of AMC radiation dosimeter |
| 47 | Report on tests and calibration of the radiation dosimeter |

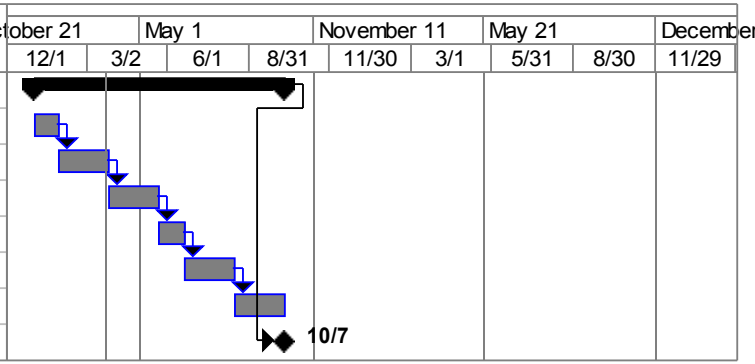



| ID | Task Name |
|---|---|
| 48 | **Development of reference, clock and timing distribution for ATCA** |
| 49 | Integration MLO, MO, Timing |
| 50 | Integration pulsed optical with RF |
| 51 | Precision temperature stabilization of the reference frequency coax cables |
| 52 | Calibration  Reference and LO to downconverters |
| 53 | Clock synthesizer for LLRF ADCs |
| 54 | Integration with ultrastable timing and clock |
| 55 | Designed and manufactured Frequency Synthesizer Board (AMC) |

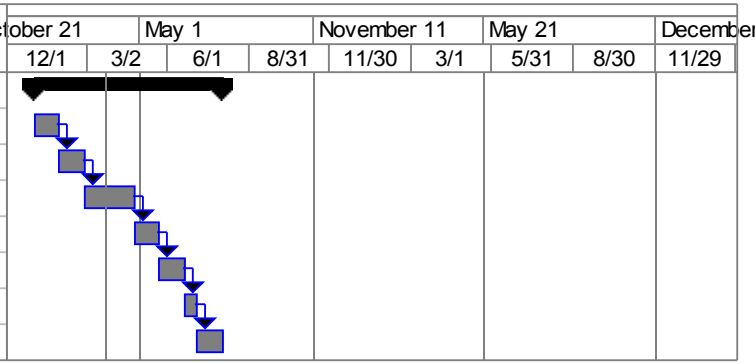


# Gantt chart of the project (4)

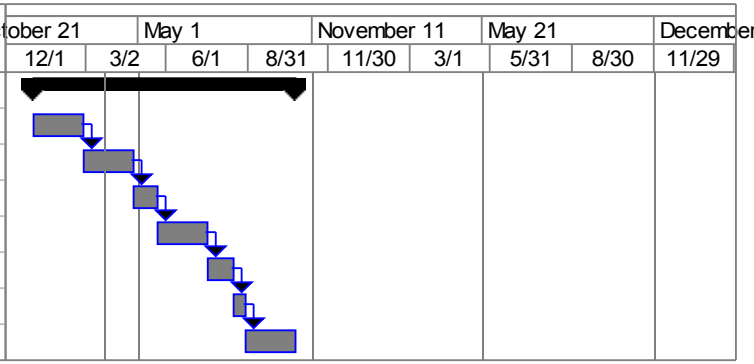
| ID | Task Name |
|---|---|
| 56 | **Development of AMC/RTM module for downconverters and upconverters** |
| 57 | Prototype design |
| 58 | Fabrication of prototype |
| 59 | Tests and debugging |
| 60 | Design modification |
| 61 | Production |
| 62 | Tests of final design |
| 63 | Integration of downconverters and upconverters in RTM (ATCA) |




| ID | Task Name |
|---|---|
| 64 | **ATCA implementation of piezo & waveguide control** |
| 65 | Requirements analysis and capture |
| 66 | Schematic desig |
| 67 | PCB design |
| 68 | Prototype fabrication |
| 69 | Debugging |
| 70 | Schematic and PCB modifications |
| 71 | Fabrication of final boards |




| ID | Task Name |
|---|---|
| 72 | **Design and fabrication of AMC modules for controlling step motors, piezo and waveguide tuners** |
| 73 | Requirements analysis and capture |
| 74 | Schematic desig |
| 75 | PCB design |
| 76 | Prototype fabrication |
| 77 | Debugging |
| 78 | Schematic and PCB modifications |
| 79 | Fabrication of final boards |



# Gantt chart of the project (5)

| ID | Task Name |
|---|---|
| 80 | **Development of beam based longitudinal feedbacks for the ATCA based LLRF system.** |
| 81 | Requirements analysis and capture |
| 82 | Design of required interfaces to LLRF controller |
| 83 | Software development |
| 84 | Installation and debugging |
| 85 | Performance tests |
| 86 | Report on longitudinal beam parameter studies and their controllability by fast feedback systems in conjunction with the LLRF system |
| 87 | System tests |
| 88 | Report on system test and and performance |