The European XFEL Detector Development program

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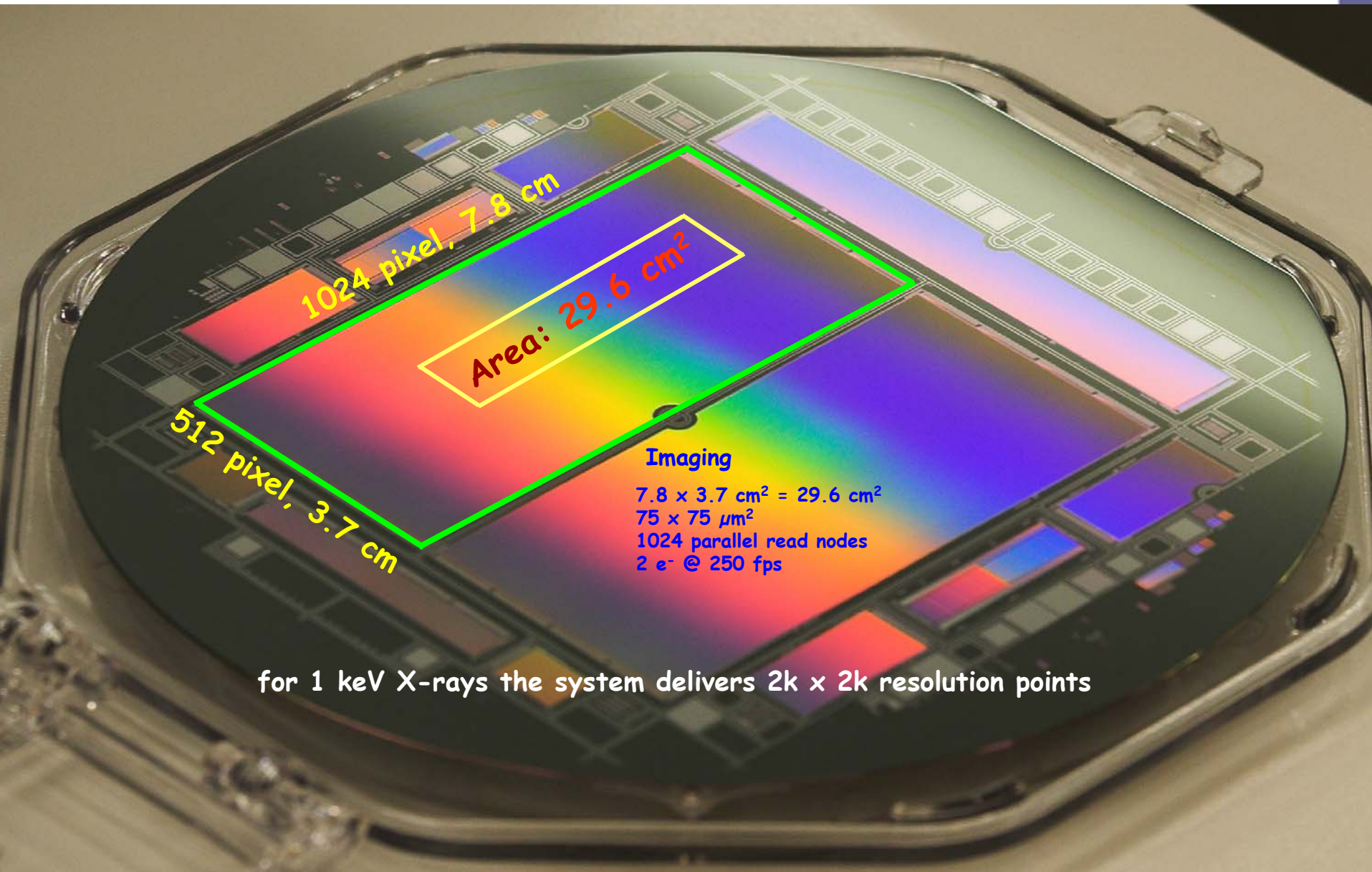
DESY-Photon Science Detector Group
WorkPackage Detectors for XFEL

Detectors for the low energies and low repetition rate

pnCCD: 1024 x 512, 30 cm²

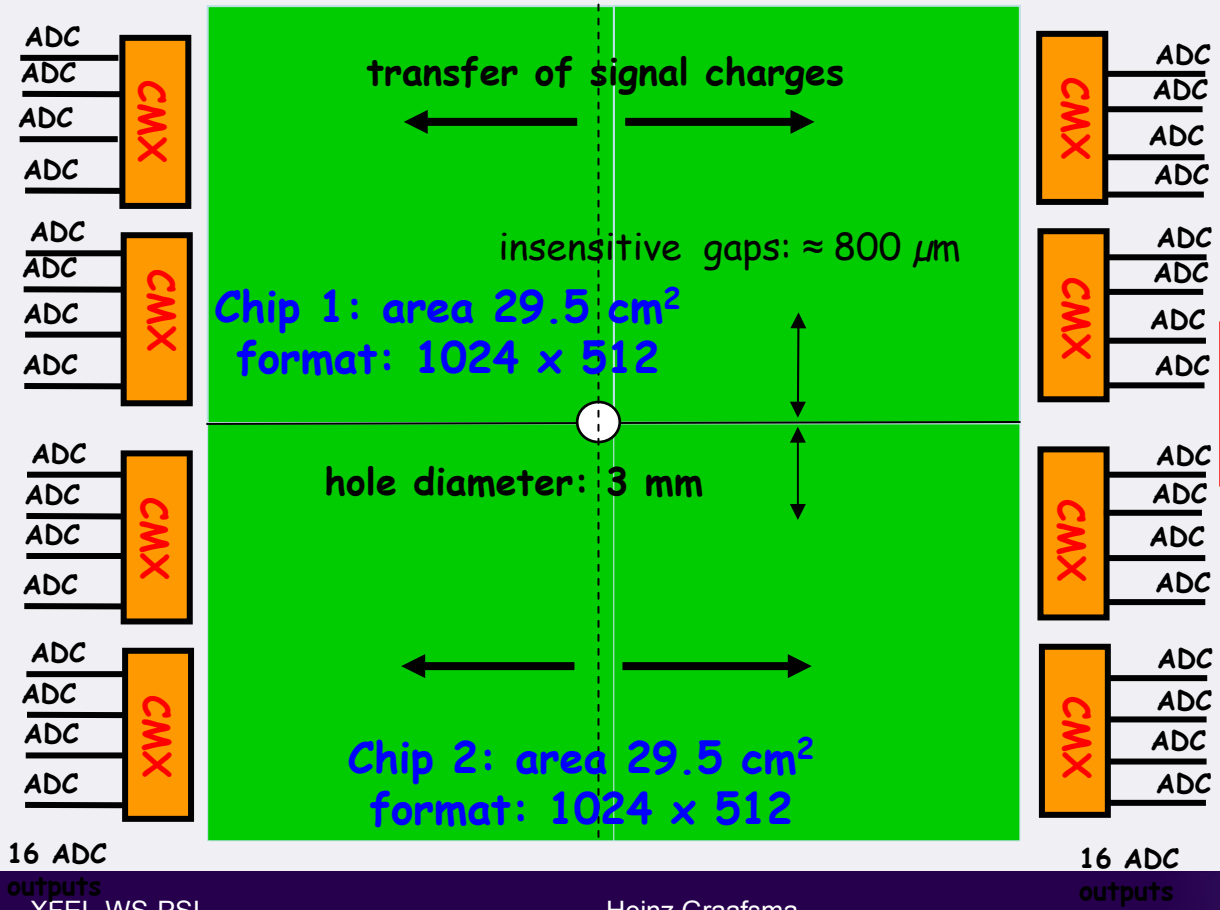


for 1 keV X-rays the system delivers 2k x 2k resolution points

Detectors for FLASH+LCLS+XFEL+Petra III

device fabrication is finished now

The full sensitive area of the system is 59 cm² with 75 µm pixels, 1024 x 1024



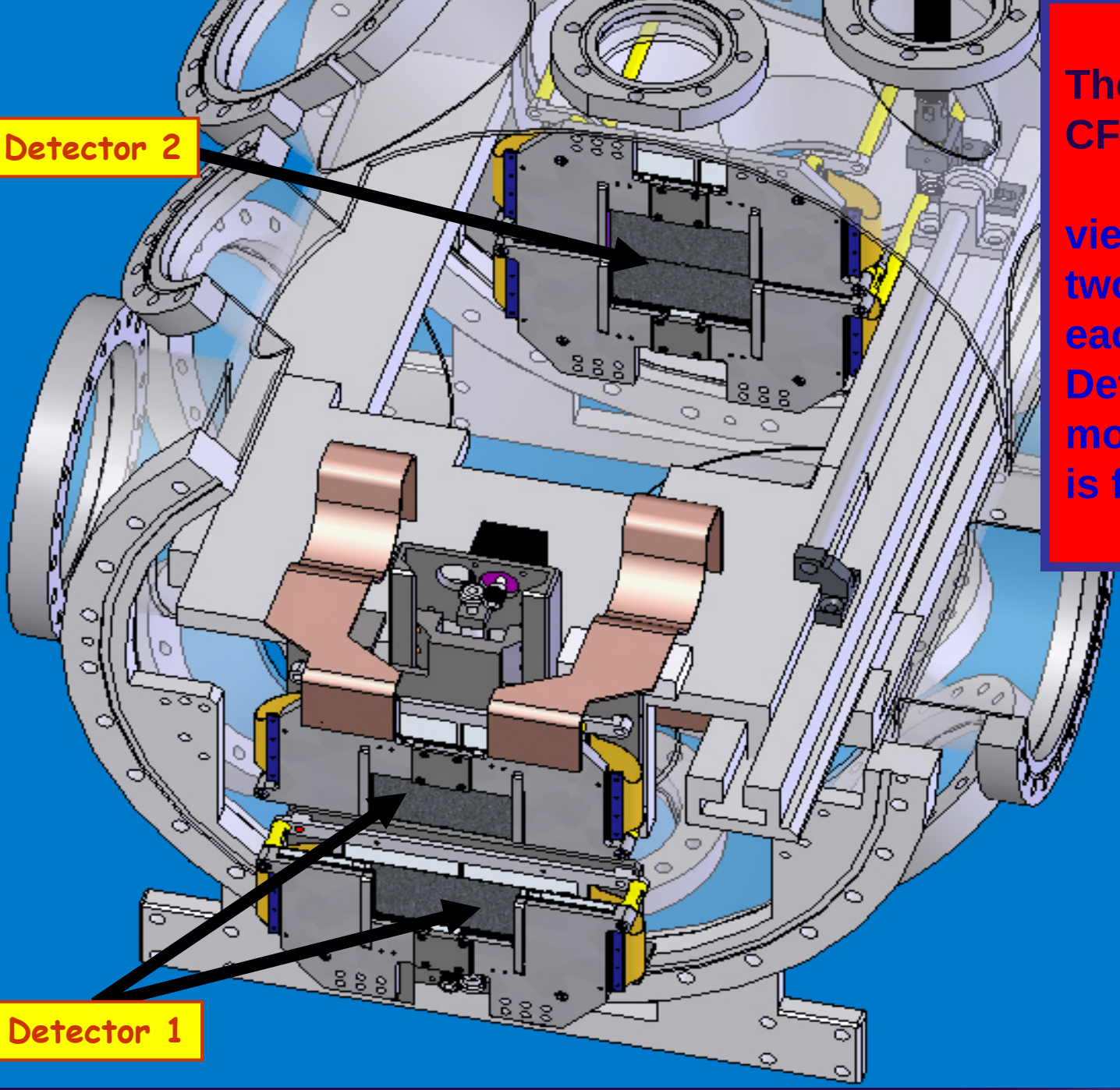
Full Frame imaging area per chip 512 x 1024

pixel size 75x75 µm²

total area per chip: 29.5 cm²

readout time per frame: 4 ms i.e. 250 fps can be triggered externally

Total sensitive system area: 59 cm



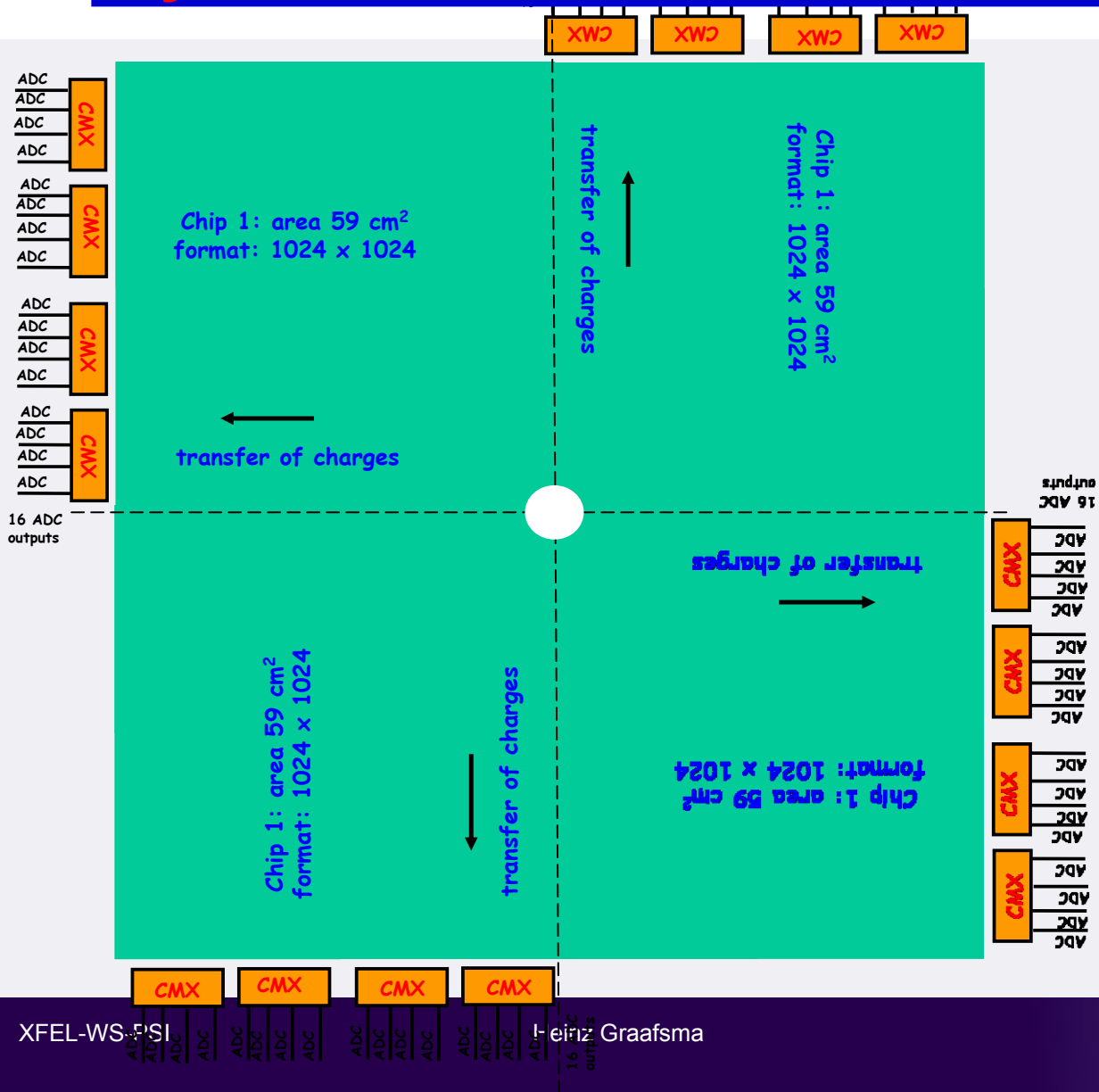
The Imagers of the CFEL-ASG Chamber

view on detector I+II, two systems 1k x 1k each.
Detector 1 is movable, Detector 2 is fixed

System alignment:
Detector 1 is movable in Y, Z and X (limited), 400 mm Ø

Detector 2 is fixed, 250 mm Ø

FLASH, LCLS, SCSS and XFEL systems in 2012



2048 x 2048 CCD array
(resolution points:
at least 4kx4k @ 1 keV)

pixel size: 75 x 75 μm^2

total area: 236 cm^2

readout time: < 8 ms

read noise < 15 electrons

Charge handling capacity:
> 1000 photons pp

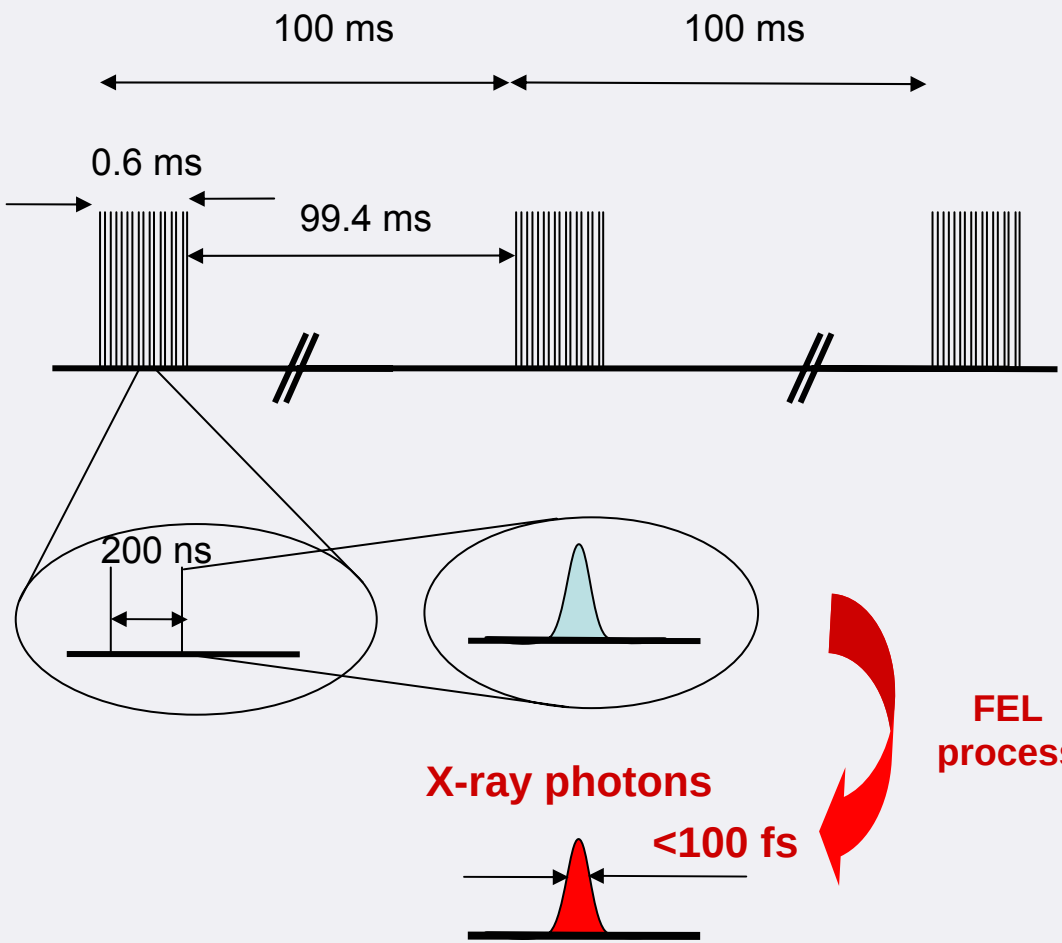
Energy 0.1<E<24 keV

thickness: 500 μm

operation temperature: -40°C

Detectors for the high energies and/or high repetition rates

European XFEL: where is the challenge?



Challenges:

- up to 30,000 bunches per second
- very high intensities (up to $10^{12}\gamma$/bunch)
- „instantaneous“ energy deposition
- very high repetition rates (up to 5 MHz)
- large variability
  - pulse patterns
  - pulse to pulse variations

DSSC - DEPFET Sensor with Signal Compression (MPI-HLL)

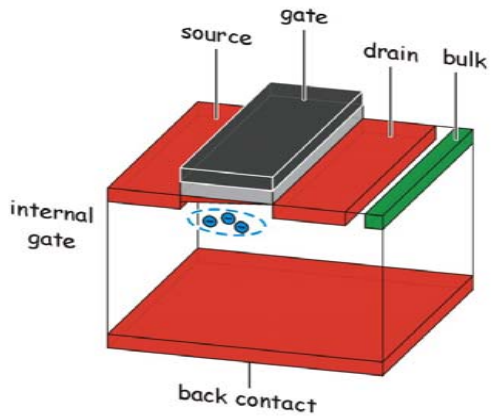
DEPFET per pixel

Very low noise (good for soft X-rays)

non linear gain (good for dynamic range)

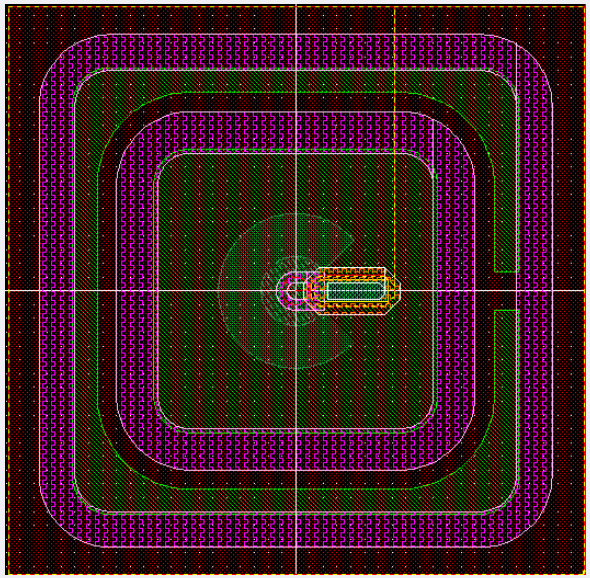
per pixel ADC

digital storage pipeline



Hexagonal pixels 200μm pitch

combines DEPFET with small area drift detector (scaleable)



MPI-HLL, Munich

Universität Heidelberg

Universität Siegen

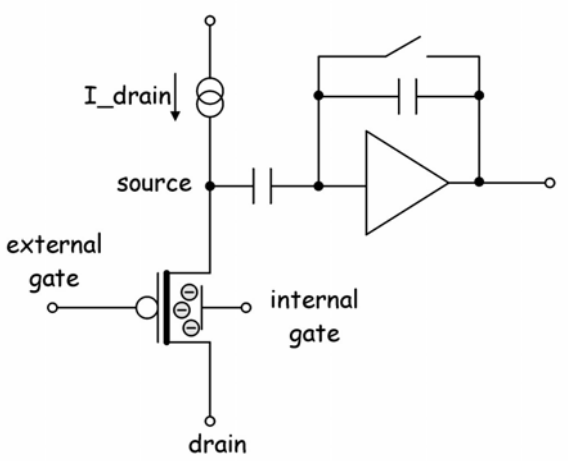
Politechnico di Milano

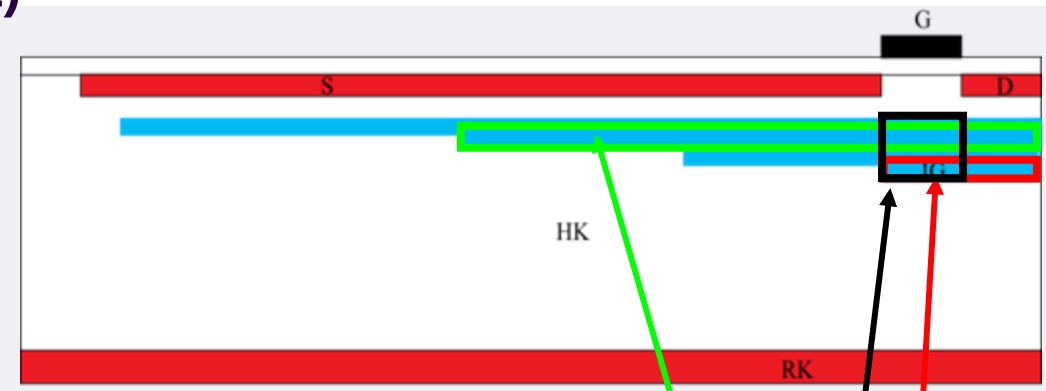
Università di Bergamo

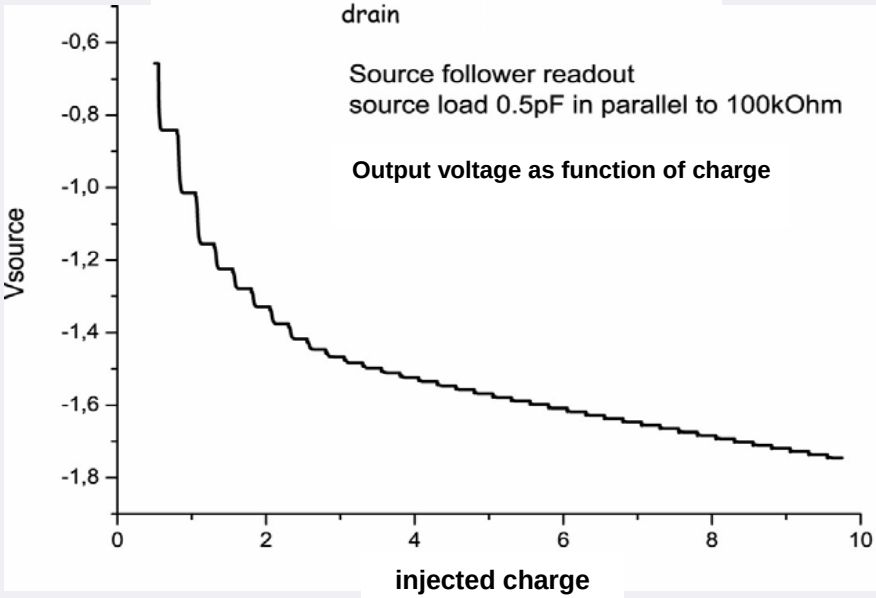
DESY, Hamburg

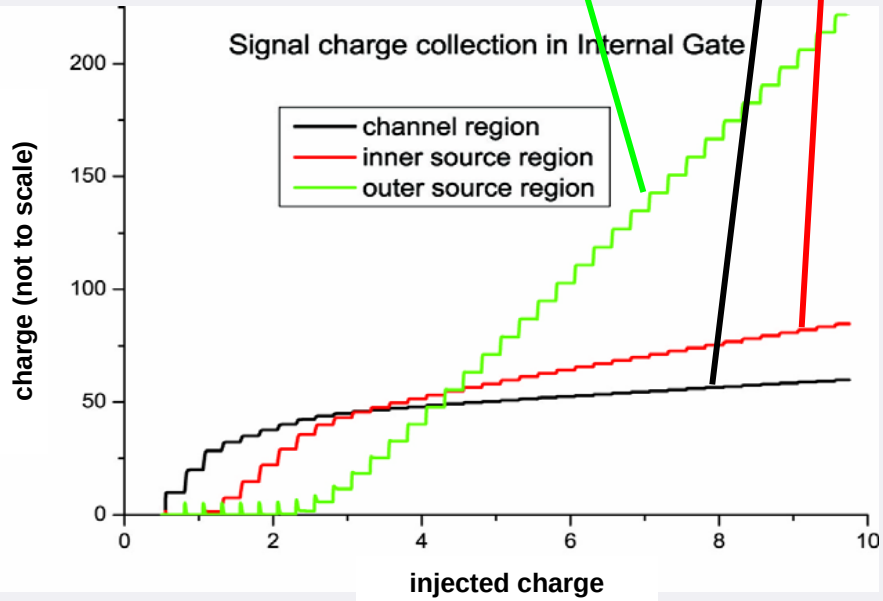
(L. Strüder, MPI HLL)

DSSC - DEPMOS Sensor with Signal Compression (MPI-HLL)









(L. Strüder, MPI-HLL)

The Large Pixel Detector (LPD) Project
(STFC)

Multi-Gain Concept

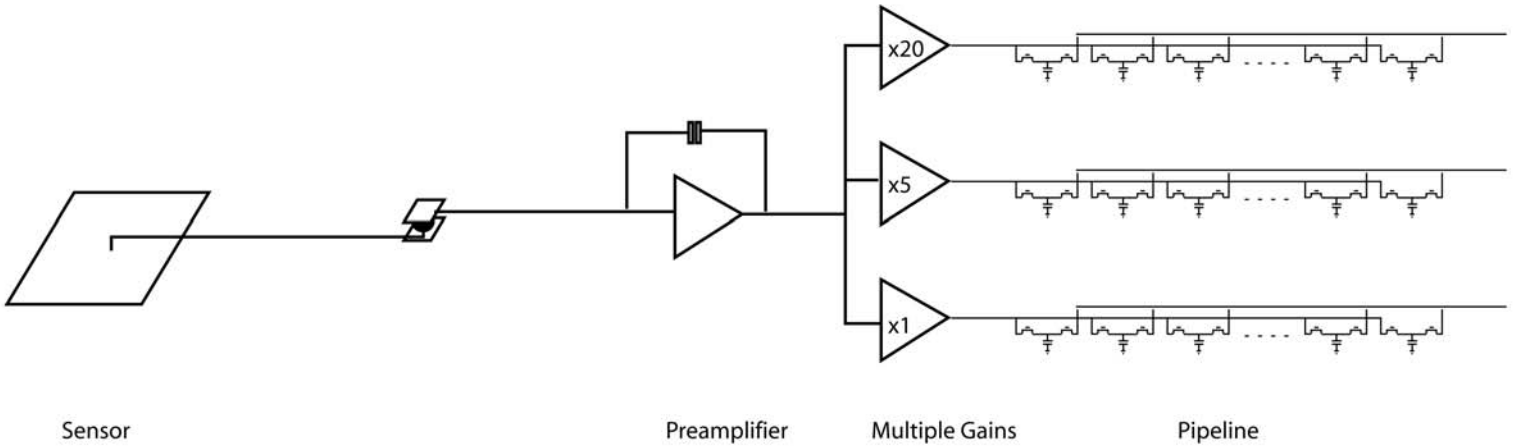
Dynamic Range Compression required

Experience with calorimetry at CERN

Relaxes ADC requirements

Fits with CMOS complexity

Threefold analogue pipeline
On-chip ADC



Science & Technology Facilities Council
Rutherford Appleton Laboratory

UNIVERSITY of GLASGOW

STFC/RAL

University of Glasgow

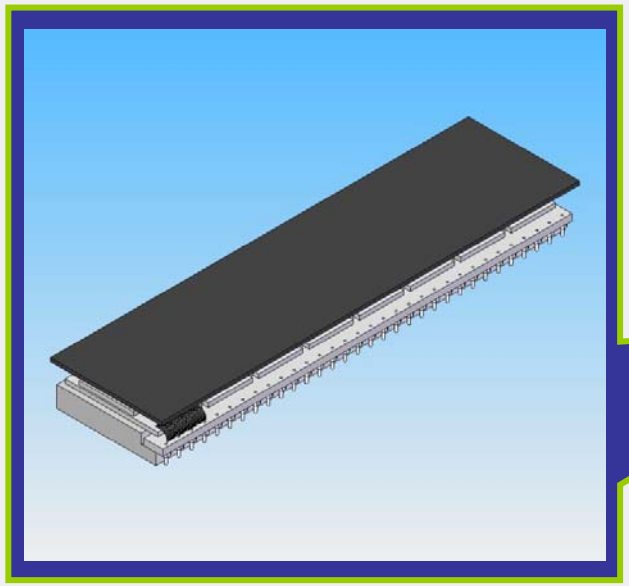
(M. French, STFC)

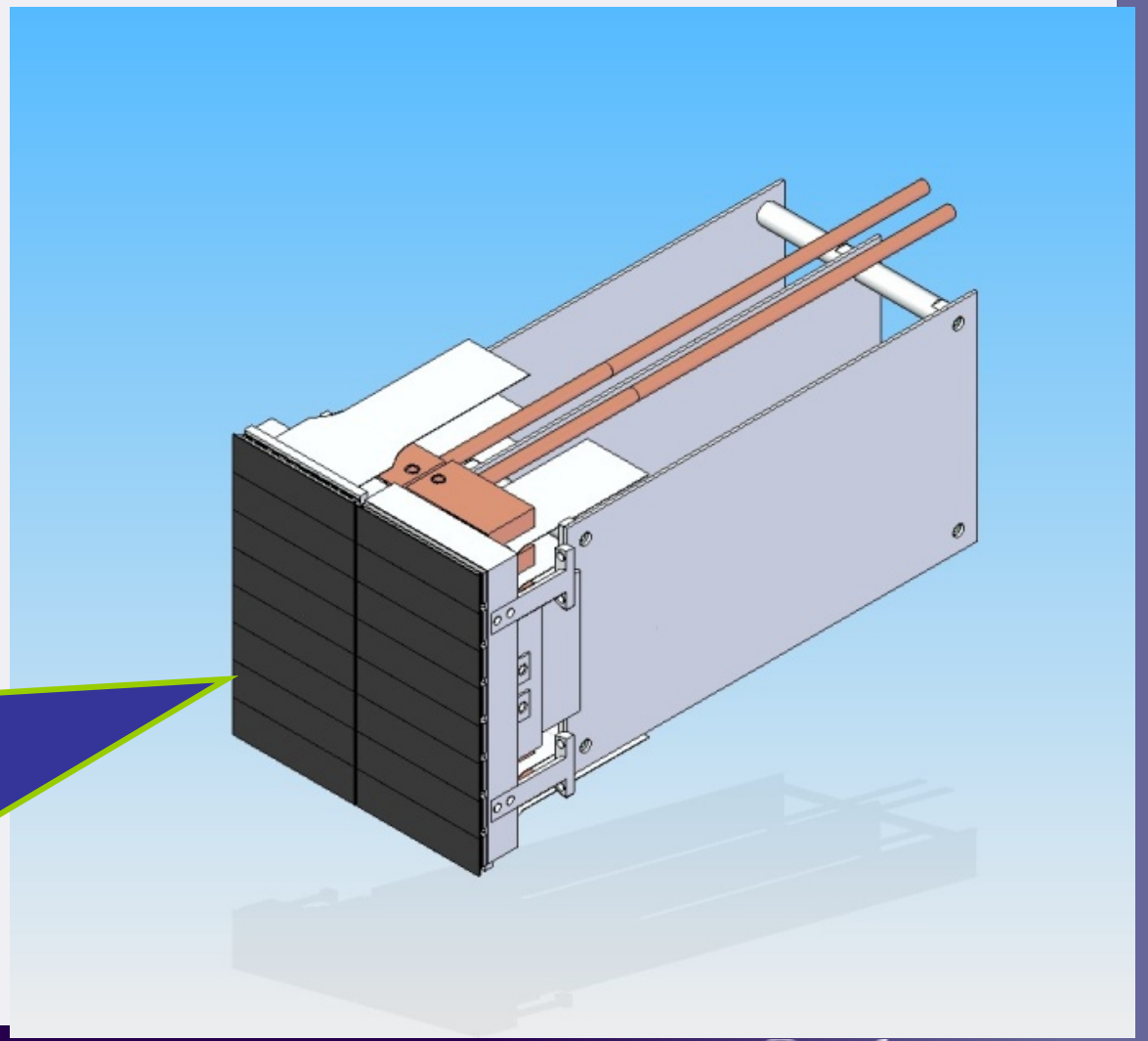
The Large Pixel Detector (LPD) Project
(STFC)

Super modules:

8 x 2 tiles

(256 x 256 pixels)





(M. French, STFC)

AGIPD - Adaptive Gain Integrating Pixel Detector (DESY)

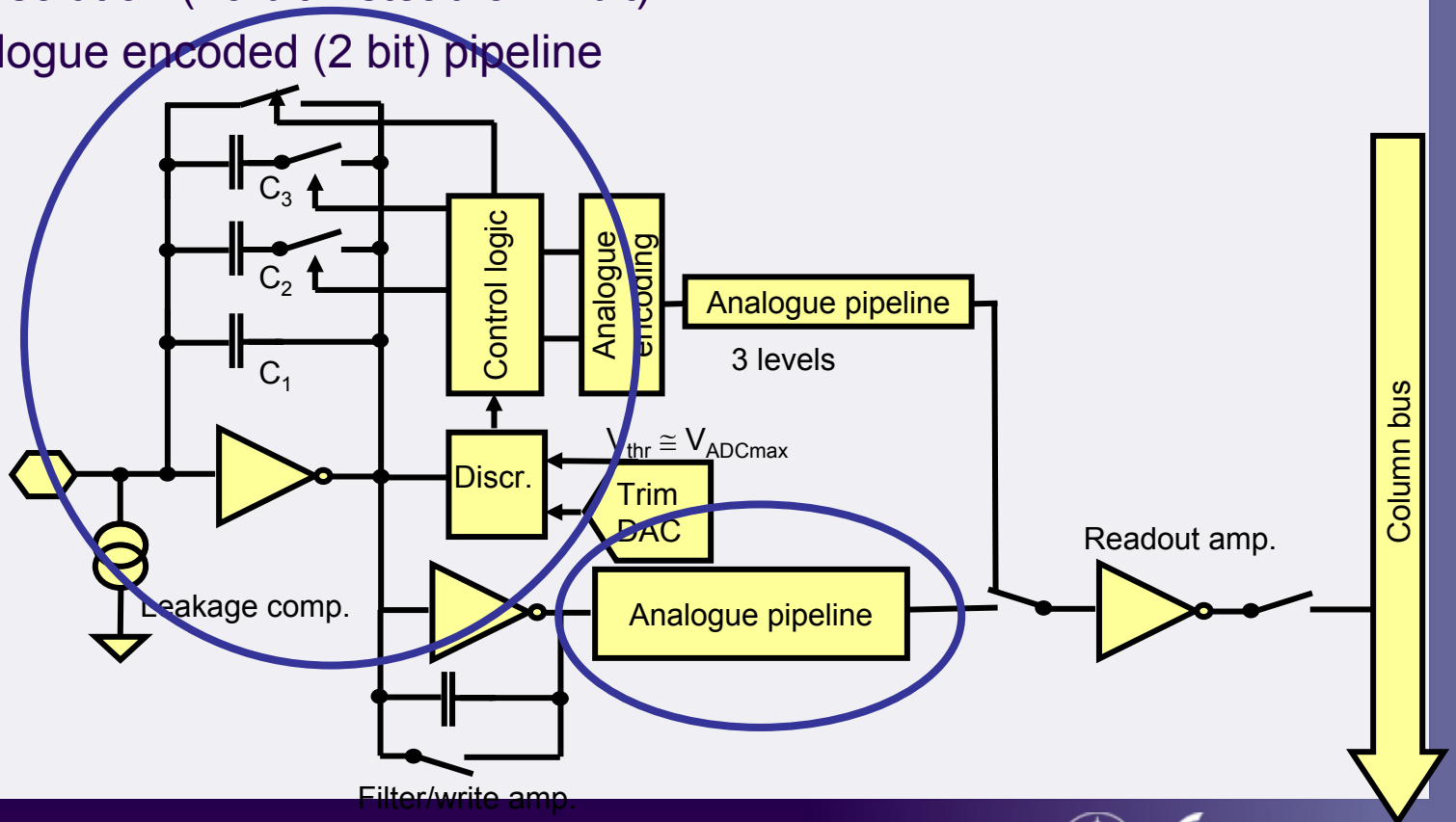
Concept

wide dynamic input range

multiple (3) scaled feedback capacitors

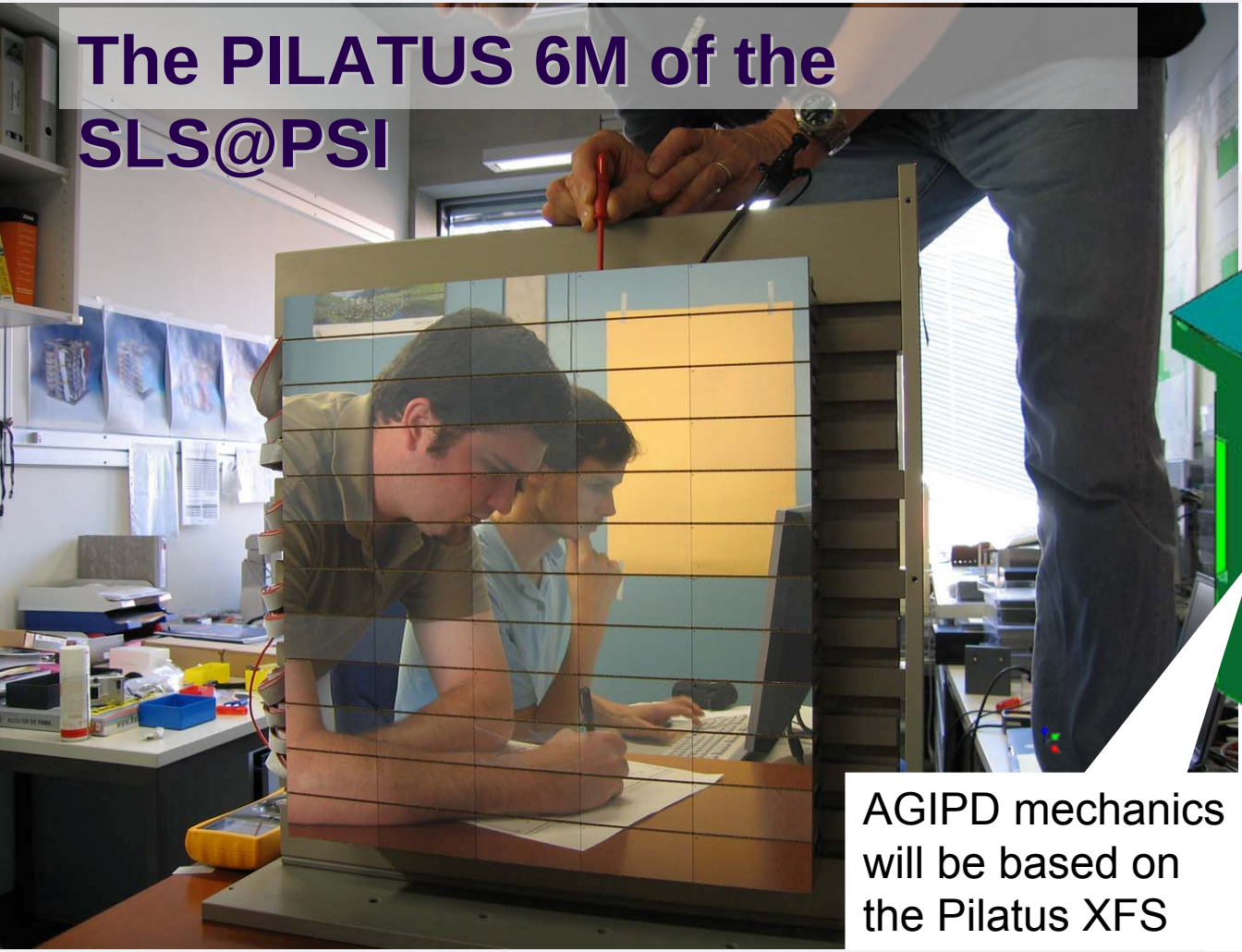
reduced ADC resolution (10 bit instead of 12bit)

analogue + analogue encoded (2 bit) pipeline

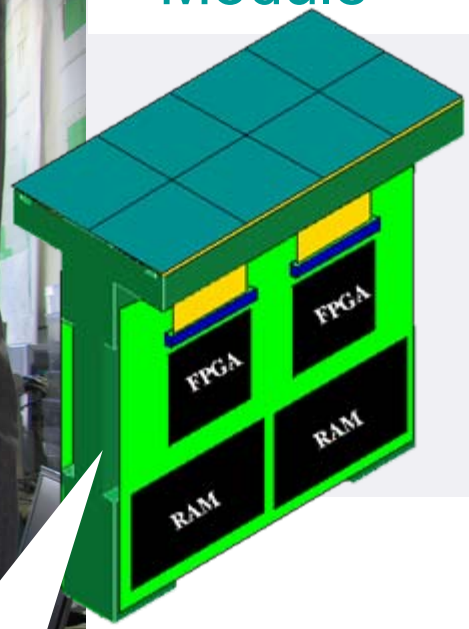


AGIPD: How things will look

The PILATUS 6M of the SLS@PSI



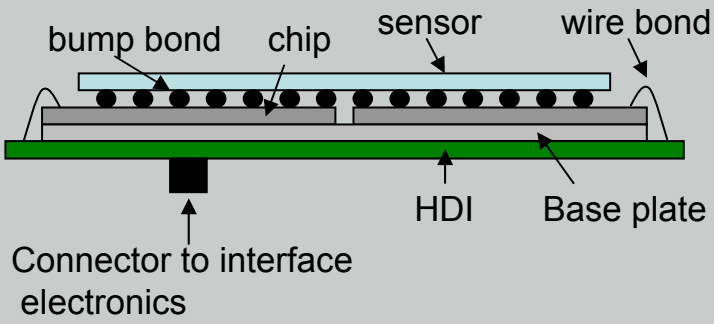
Pilatus XFS Module

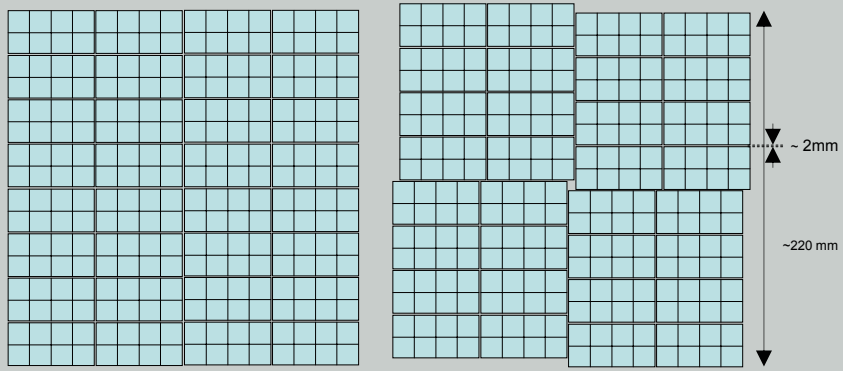


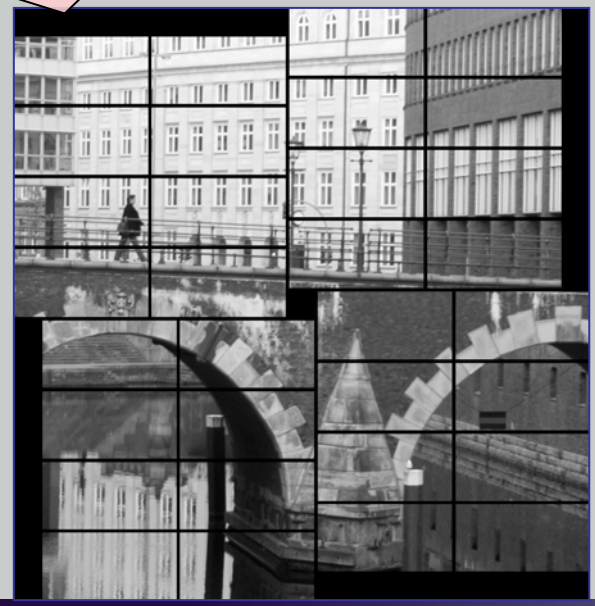
AGIPD mechanics will be based on the Pilatus XFS

2x4 (8) Chips per Module.
~78 x 39 mm² (XFS)
~50 x 27 mm² (HPAD)

Detector response simulations (G. Potdevin)

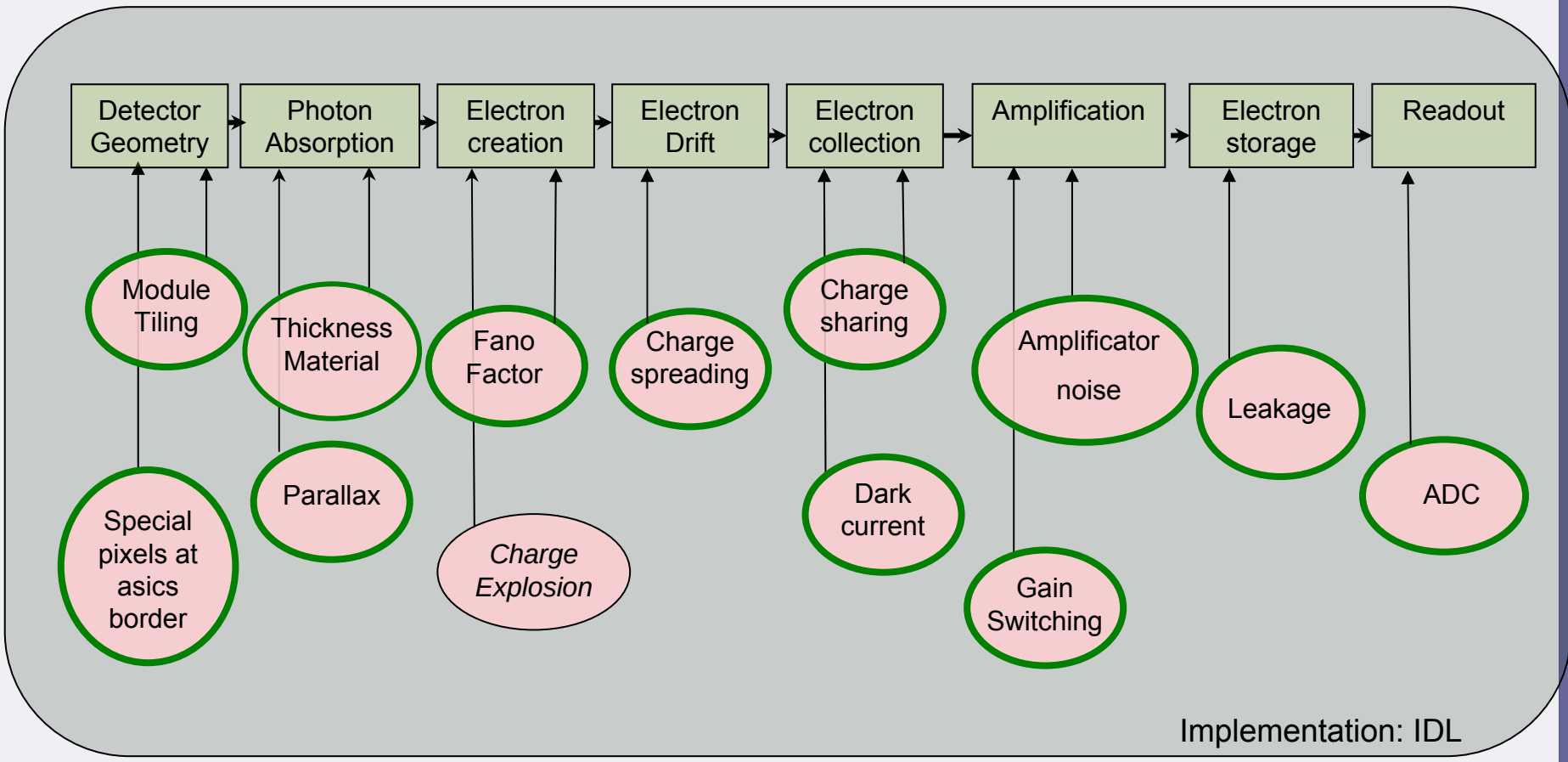




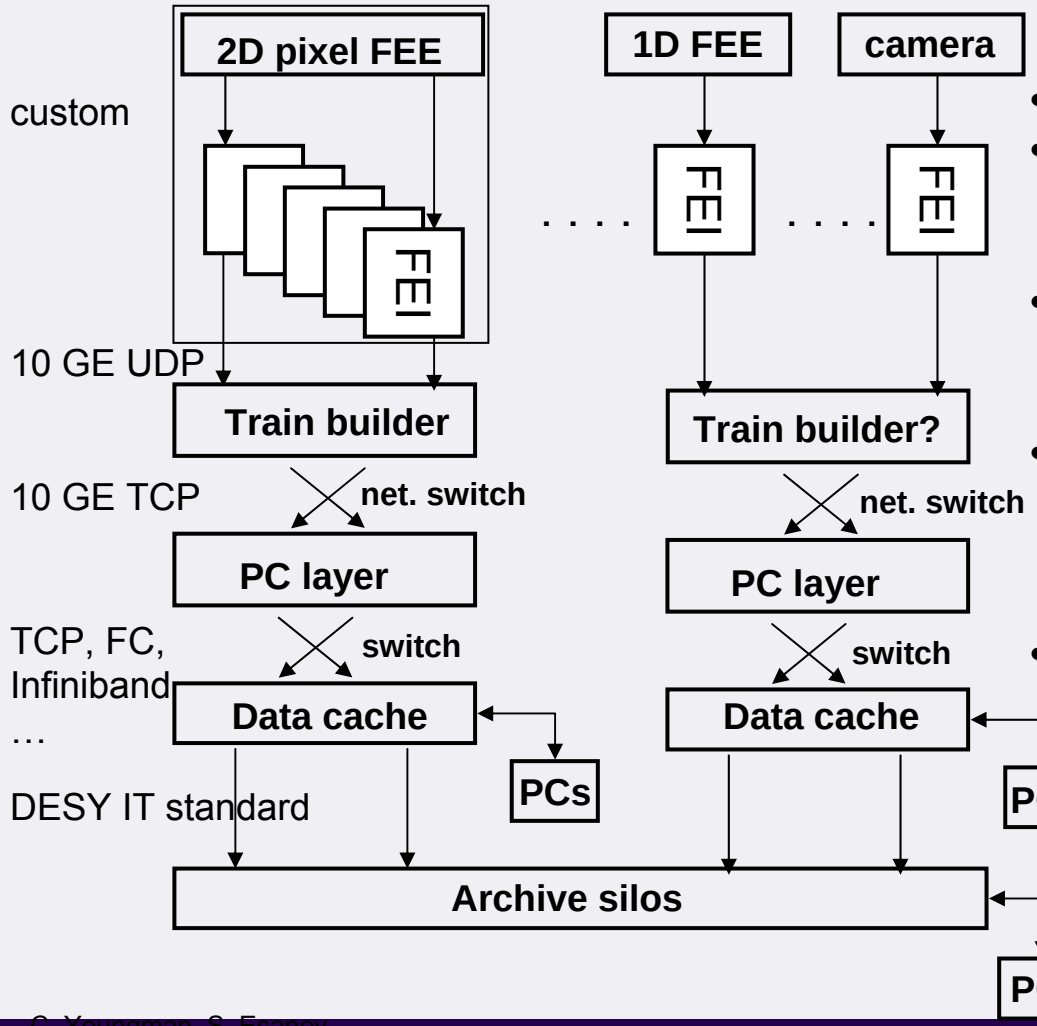


Simulation of the detector Performances (G. Potdevin)

The code is built on a modular structure



DAQ architecture (C. Youngman-WP76)



- Front End Electronics (FEE)
- Front End Interface (FEI)
  - interface to Train Builder.
  - integrated in 2D
- Train builder layer
  - builds trains
  - simple data processing
- PC layer
  - interface to cache
  - additional train building
  - more complex data process
- Data cache
  - hold, analyze, reduce and reject data
  - post processing
  - commit to silo