Depleted monolithic active pixel sensors using column drain readout – LF & TJ-Monopix

11th Terascale Detector Workshop

Tianyang Wang

University of Bonn:

C. Bespin, I. Caicedo, T. Hemperek, T. Hirono, F. Hügging, H. Krüger, K. Moustakas, D-L. Pohl, P. Rymaszewski, **T. Wang** and N. Wermes

Centre de Physique des Particules de Marseille:

M. Barbero, S. Bhat, P. Breugnon, Z. Chen, S. Godiot, P. Pangaud and A. Rozanov

CERN

I. Berdalovic, R. Cardella, T. Kugathasan, C.A. Marin Tobon, H. Pernegger, N. Egidos, W. Snoeys

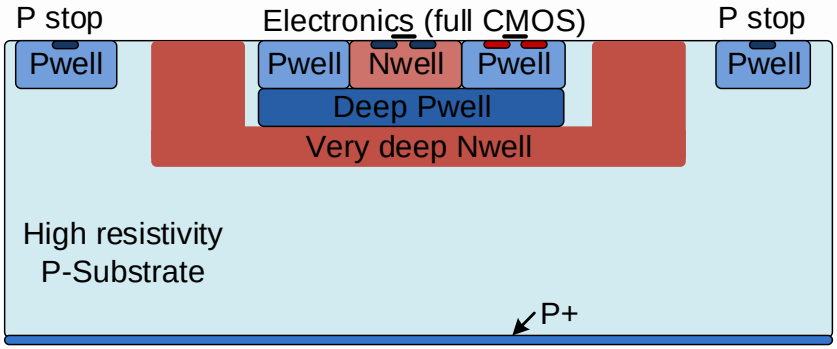
IRFU CEA-Saclay

Y. Degerli, F. Guilloux and P. Schwemling

Sensor concepts

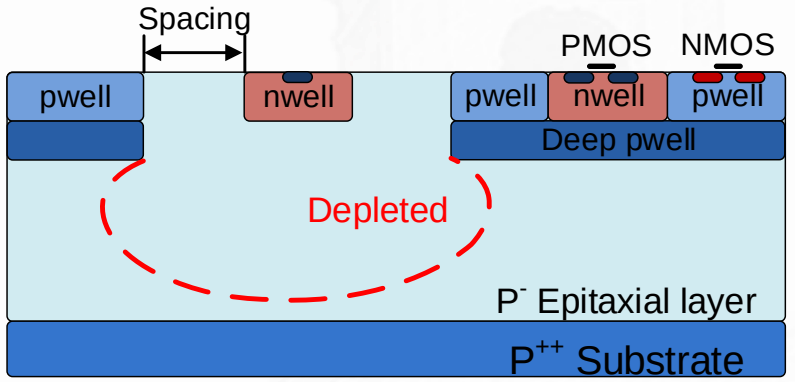
- High-rad. envir. => fast charge collection => **depleted** sensitive layer => $d \sim \sqrt{\rho \cdot V}$

Large fill factor: LF-Monopix



- *LFoundry 150 nm CMOS technology*
- *High res. (> 2 kΩ·cm) P-substrate*
- *High reverse bias > 400 V possible*
- *Deep nwell as the charge collection node*
- *Full CMOS by isolating nw & deep nw*
- *Backside thinning & processing possible*
  - *Fully depleted 100 µm sensor available*

Small fill factor: TJ-Monopix

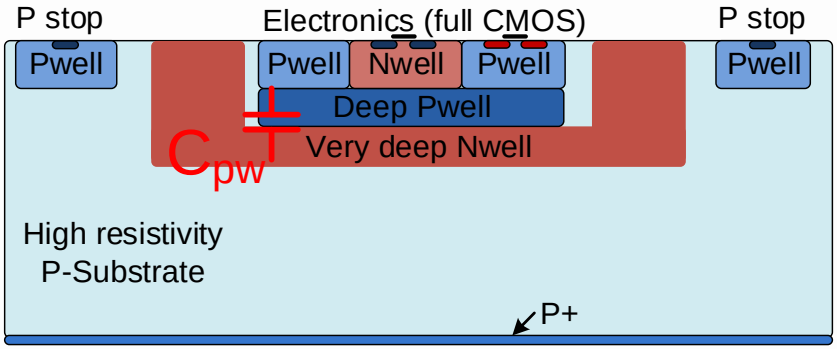


- *TowerJazz 180 nm CMOS technology*
- *High res. (> 1 kΩ·cm) epi. layer (25 µm)*
- *-6 V reverse bias*
- *Nwell as the charge collection node*
- *Full CMOS by using deep pw*
- *O(50 µm) thin detector possible*

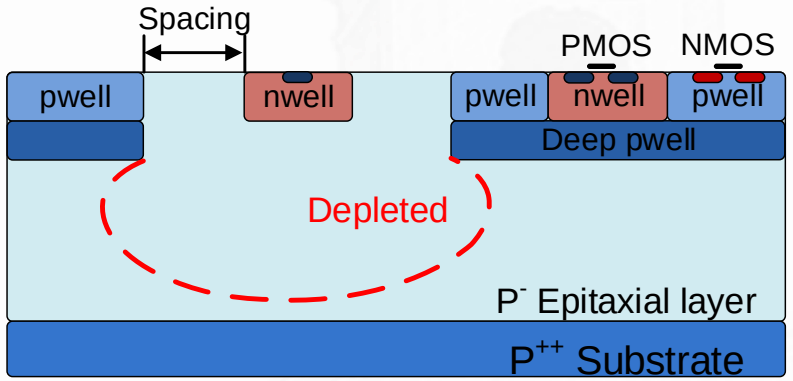
Sensor concepts

- High-rad. envir. => fast charge collection => **depleted** sensitive layer => $d \sim \sqrt{\rho \cdot V}$

Large fill factor: LF-Monopix



Small fill factor: TJ-Monopix



☺ *Rad. hard*
- *uniform field, short drift distance*

☹ *Large sensor capacitance (200 - 400fF)*
- *non-negligible C_{pw}*
- *noise & speed (power) penalties*
- *x-talk: dedicated pixel design needed*

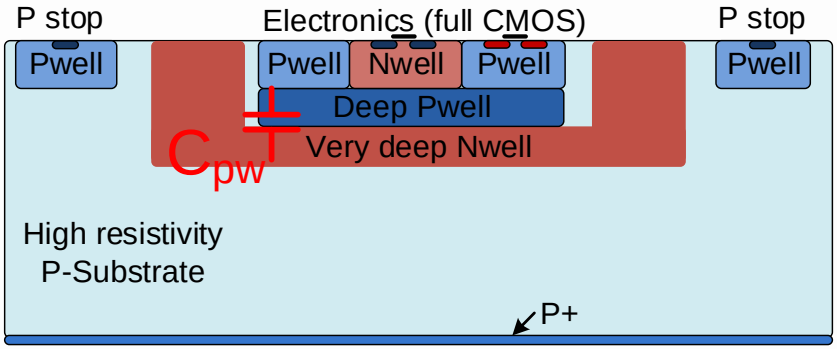
☺ *Very small sensor capacitance (< 10fF)*
- *low noise & power*

☹ *Limited depletion, long sig. travel path*
- *dedicated efforts to enhance depletion*

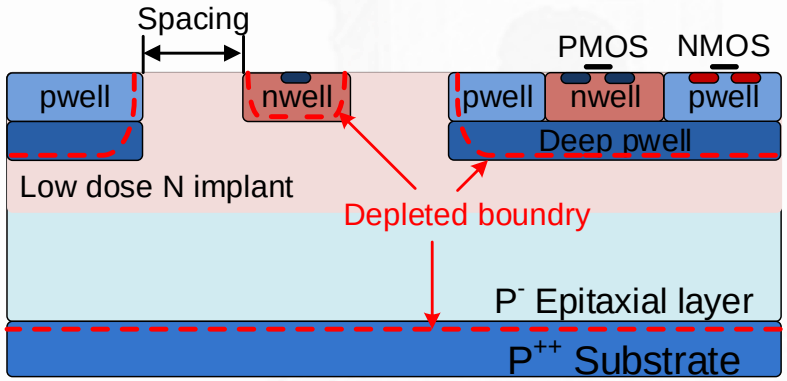
Sensor concepts

- High-rad. envir. => fast charge collection => **depleted** sensitive layer => $d \sim \sqrt{\rho \cdot V}$

Large fill factor: LF-Monopix



Small fill factor: TJ-Monopix



Rad. hard
- *uniform field, short drift distance*

Large sensor capacitance (200 - 400fF)
- *non-negligible C_{pw}*
- *noise & speed (power) penalties*
- *x-talk: dedicated pixel design needed*

Modified process adding a planar N layer

⇒ significantly enhanced lateral depletion

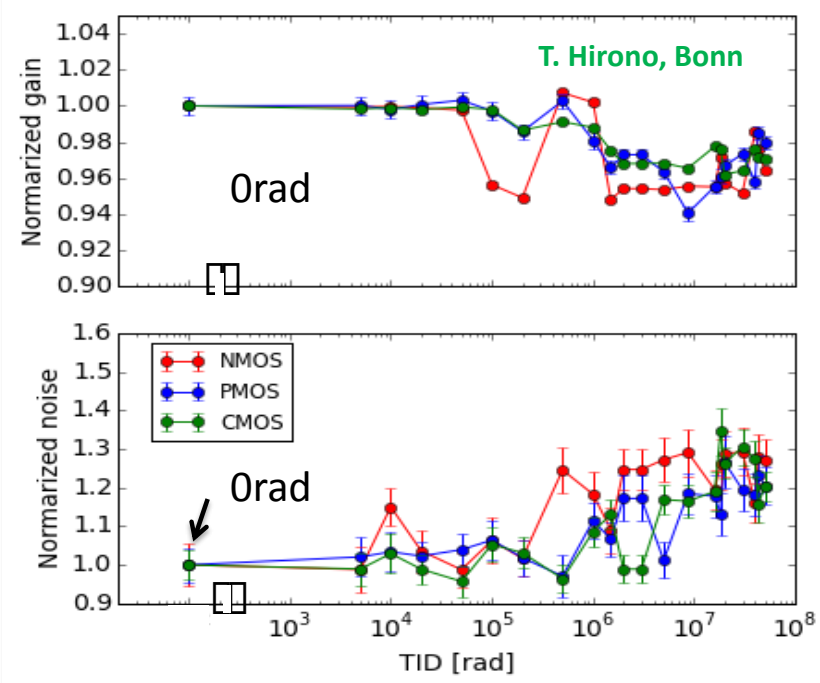
⇒ maintain small sensor capacitance

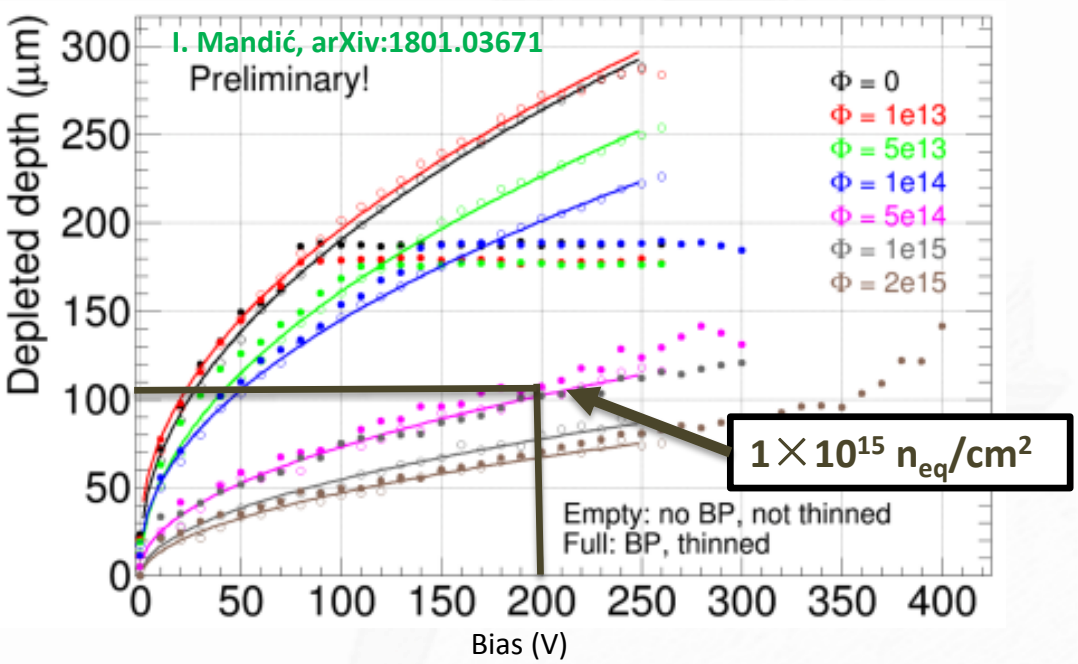
⇒ higher reverse bias possible

Irradiation performance based on previous prototypes

Irradiation performance: LFoundry

- Radiation tolerance evaluated with previous prototypes => **in line with ITk L4**
  - Total ionizing dose
  - NIEL





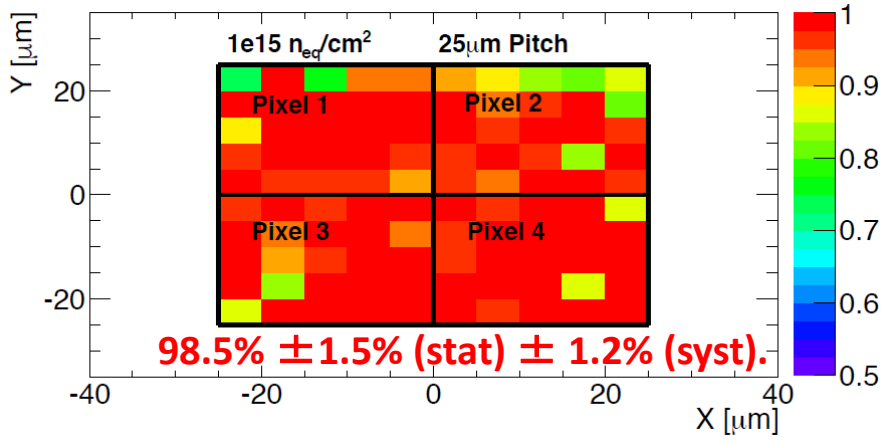
No significant performance loss after 50 Mrad

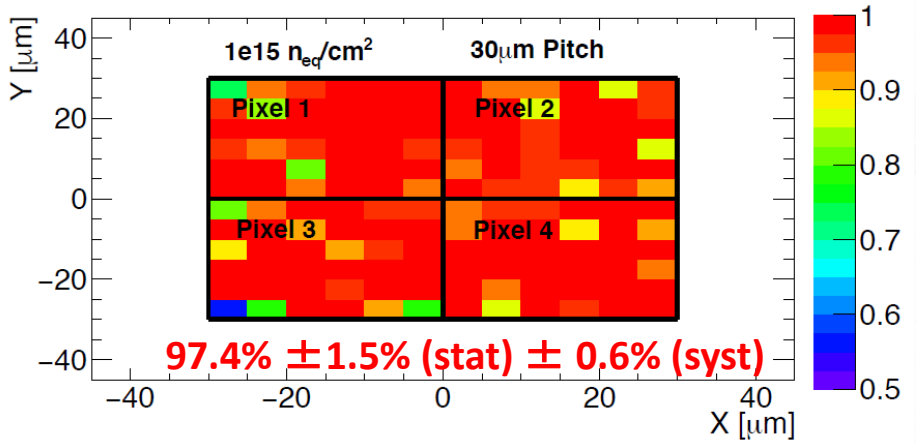
> 100 µm depletion after 10^{15} n_{eq}/cm^2

Irradiation performance: TowerJazz

- Uniform efficiency after $10^{15} n_{eq}/cm^2$ for modified process
  - *Measurement based on a pure analog test chip (named "Investigator")*
  - *High overall efficiency for 25 µm and 30 µm square pixel*

    ***=>** not possible with standard process*



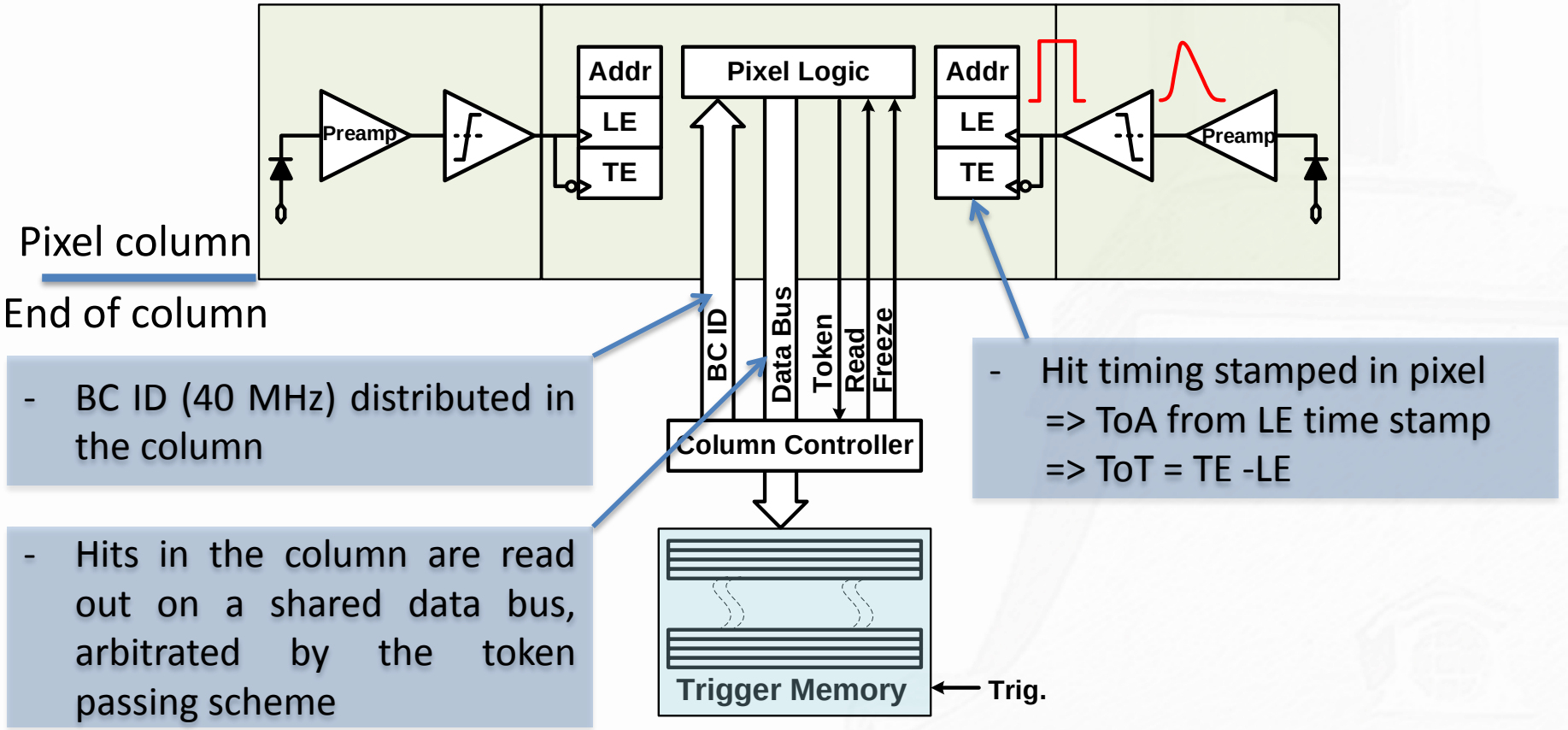


H. Pernegger, et al., DOI: 10.1088/1748-0221/12/06/P06008

Besides sufficient radiation tolerance, the sensor should also integrate a fast readout architecture

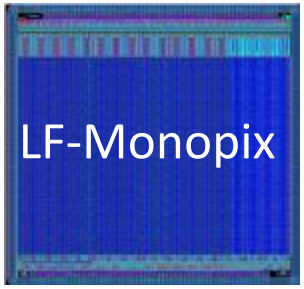
Column drain readout architecture

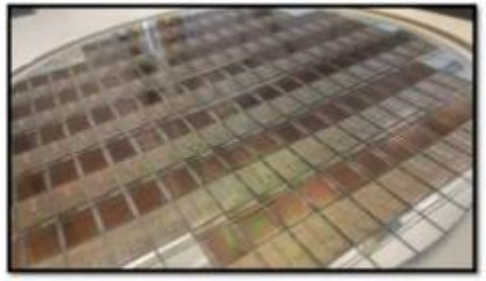
- Similar to the current ATLAS pixel readout chip “FE-I3”
  - Particle rate @ L4 of ITk is similar to the current inner pixel detector
  - Sufficient rate capability with affordable in-pixel logic density for CMOS pixels



Prototype design

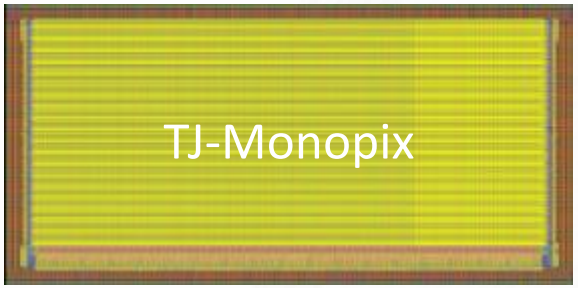
Submitted: August, 2016
back: January, 2017





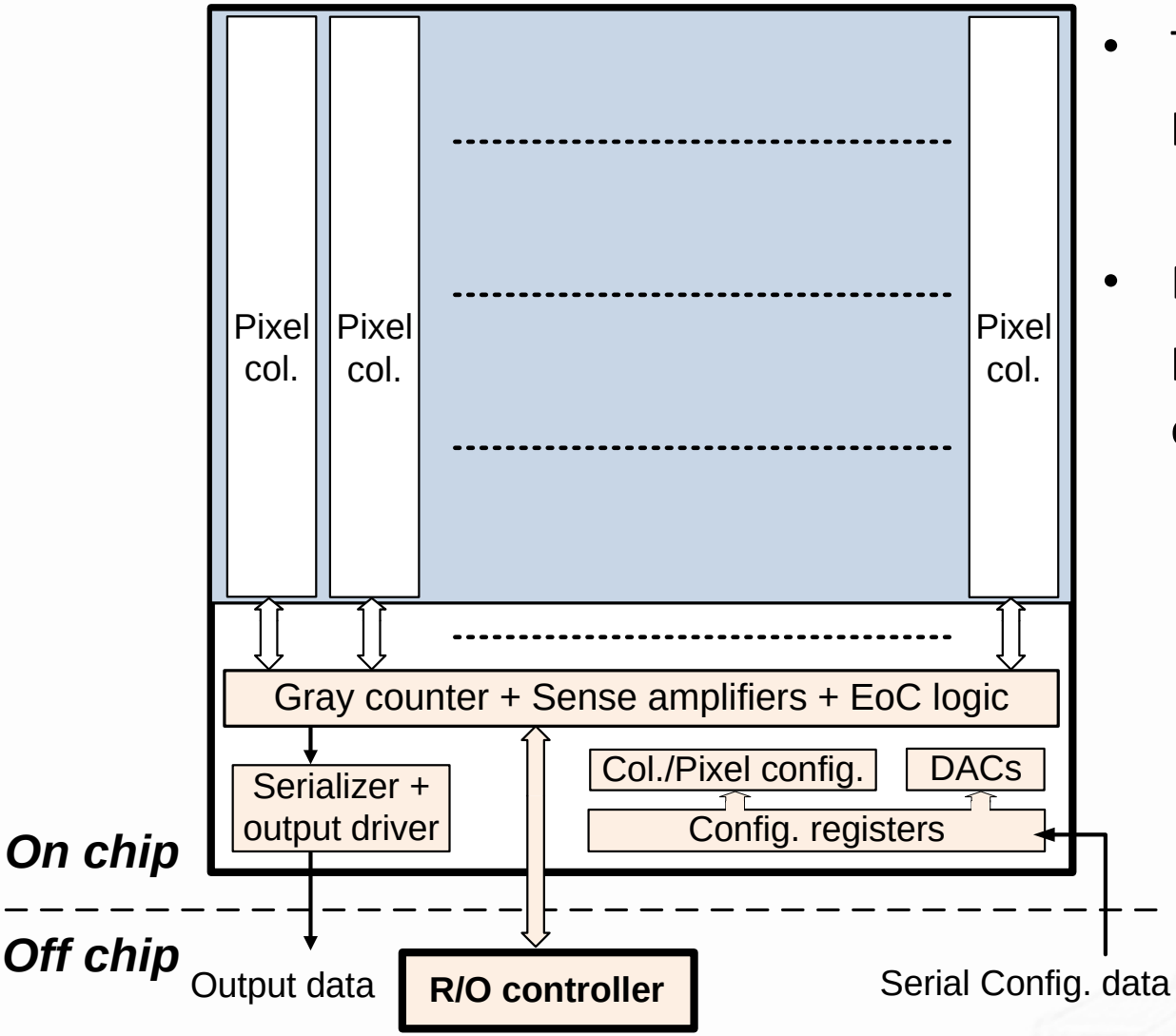
Design by: UNIVERSITÄT BONN, CPPM, Irfu - CEA Saclay Institut de recherche sur les lois fondamentales de l'Univers

Submitted: September, 2017
back: January, 2018



Design by: UNIVERSITÄT BONN, CERN

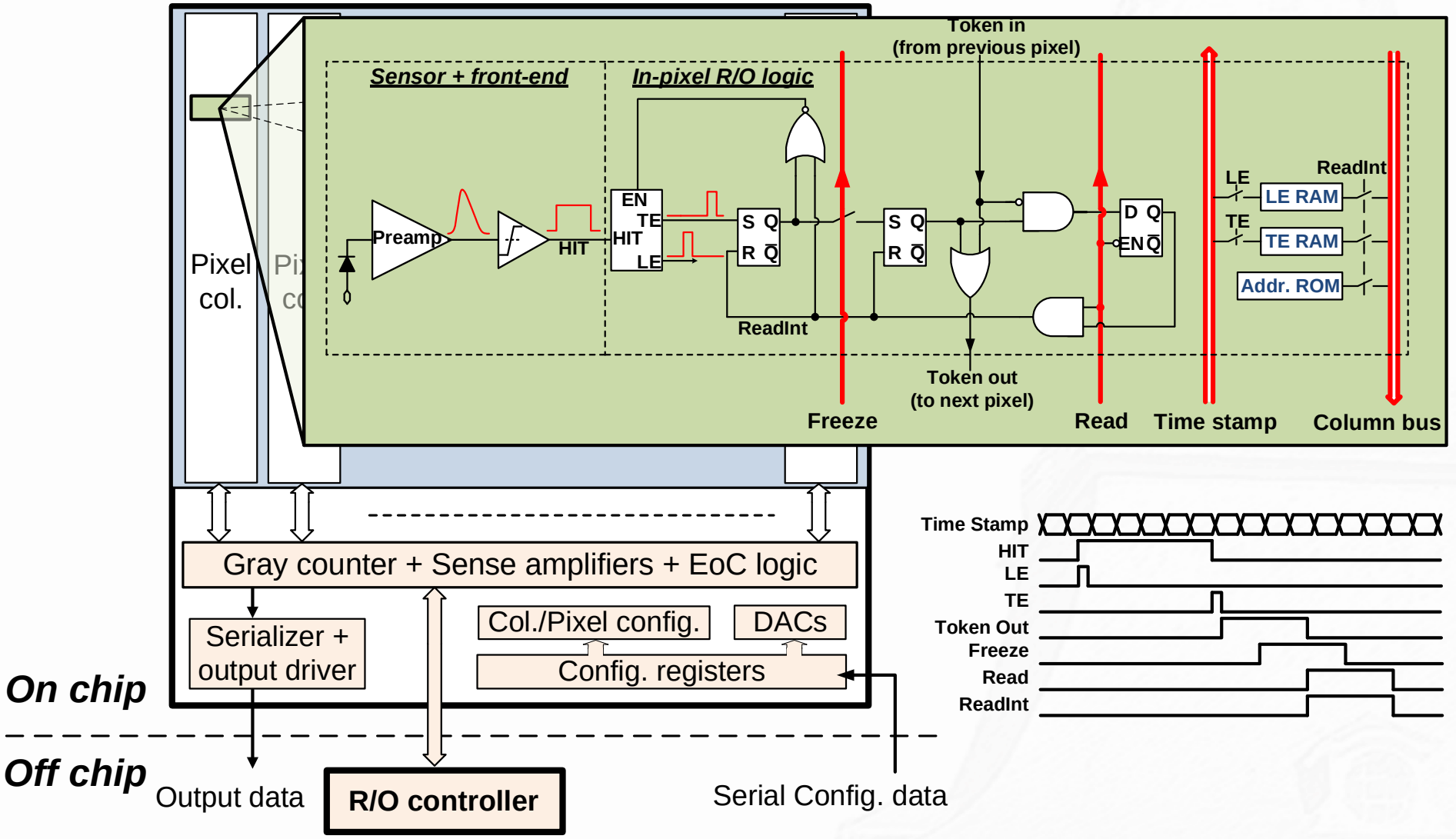
Chip design strategy



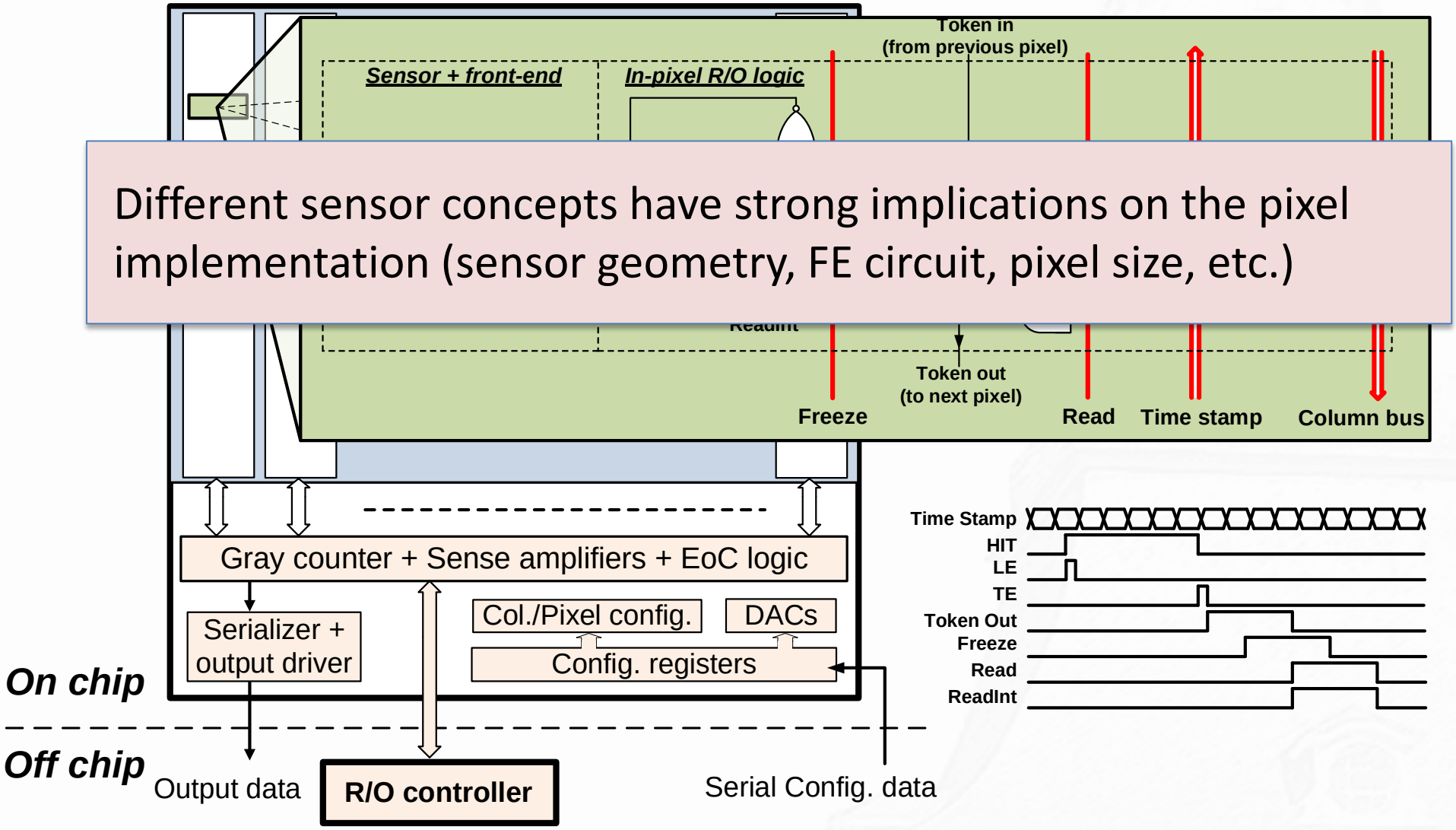
- The goal is to demonstrate a large pixel array with column drain r.o.
  - 1 - 2 cm^2 chip size
- For design simplicity, not all the peripheries expected for the final chip are included
  - *Off-chip r.o. controller by FPGA*
  - *No trigger memory on chip*

    => All hits r.o. sequentially via a serial link
  - *No high speed (Gbps) link, serial powering, etc.*

Pixel design: A functional view

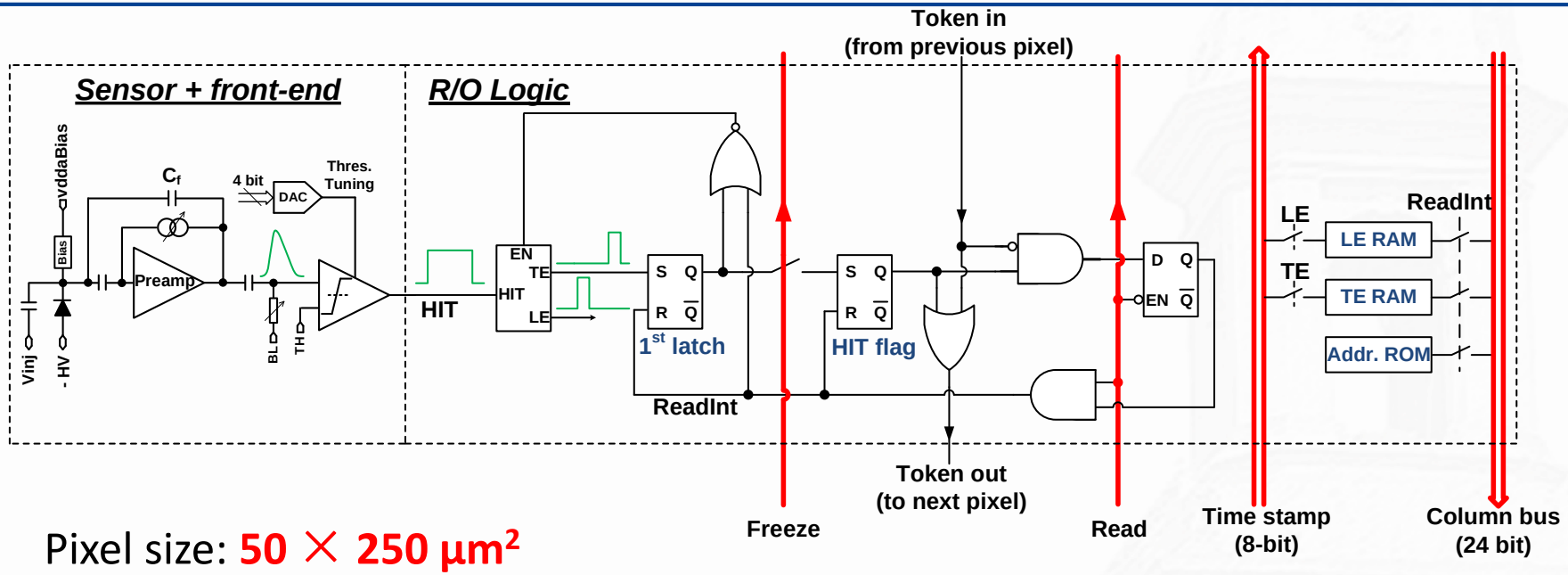


Pixel design: A functional view

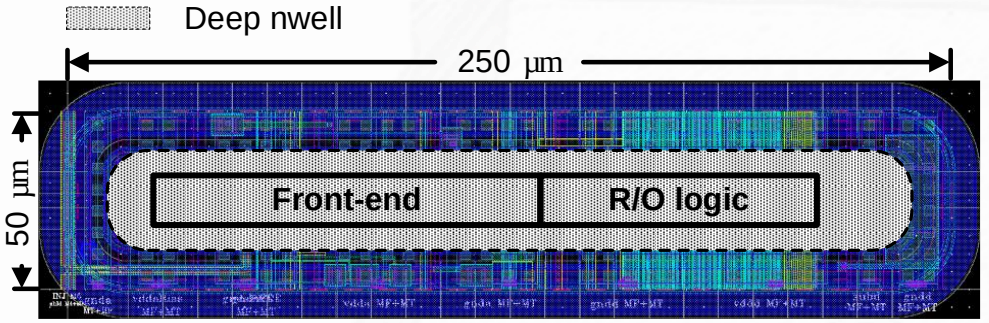


Different sensor concepts have strong implications on the pixel implementation (sensor geometry, FE circuit, pixel size, etc.)

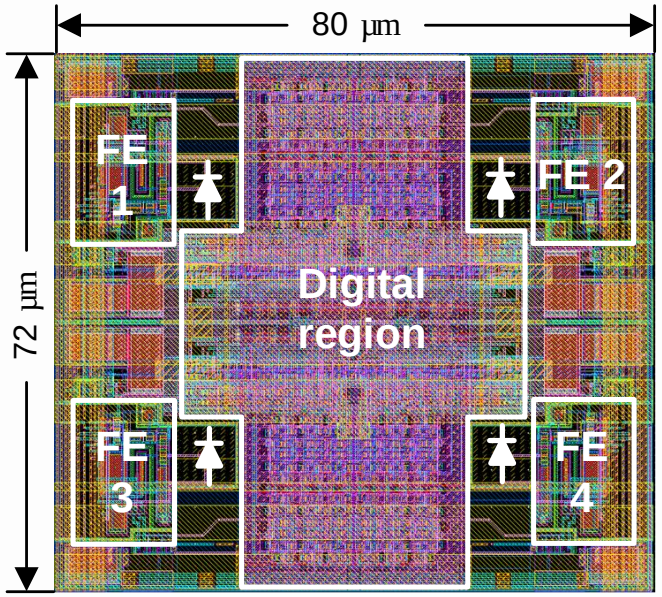
Pixel design: LF-Monopix

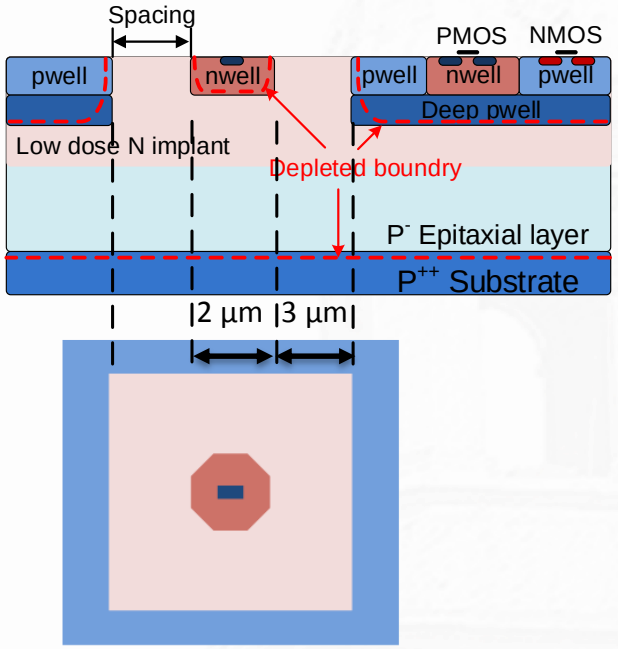


- Pixel size: **50 × 250 µm²**
- Fill factor **~ 55%**
- CSA + Discri. with **4-bit DAC**
  - *Optimized for **< 25 ns** time walk*
  - *Static current **~ 20 µA/pixel***
- **Full-custom** dig. Circuit
  - *Minimized area => reduce C_d*
  - *Special **low noise design**, e.g. current steering circuit*



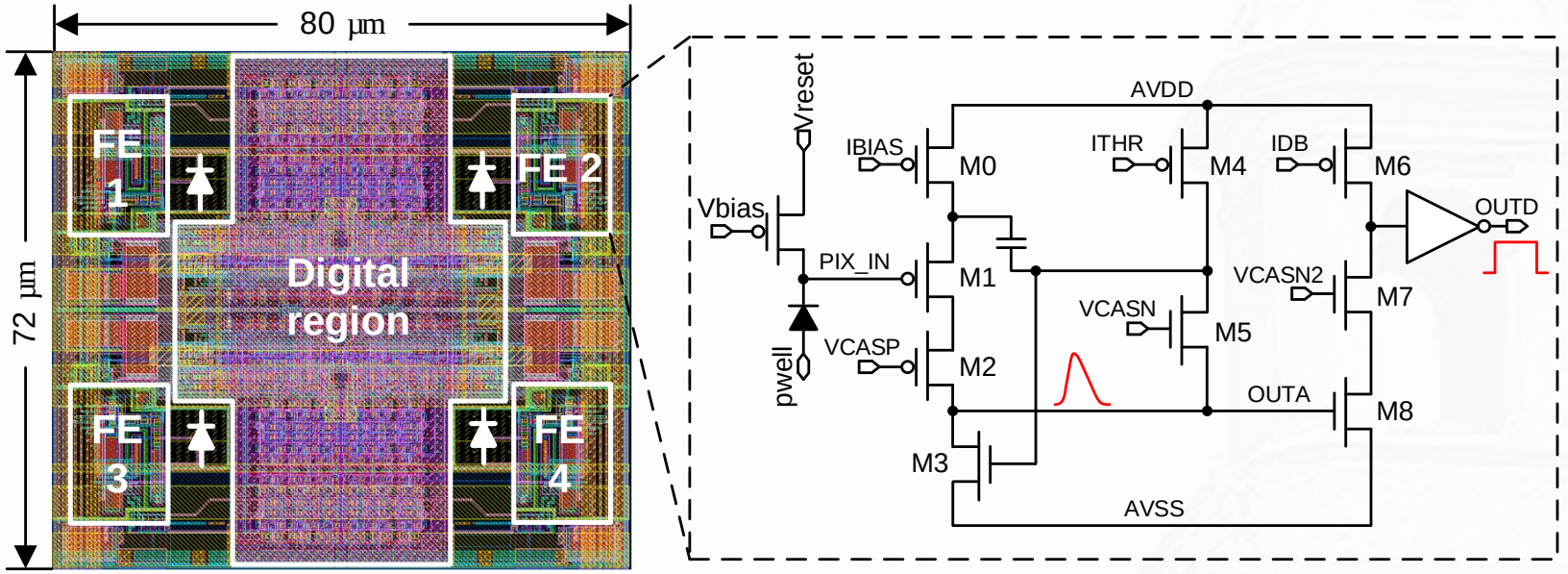
Pixel design: TJ-Monopix





- Pixel size **36 × 40 µm²** => smaller than large fill factor design
- Small sensor footprint: **2 µm** diameter diode + **3 µm** spacing
- Separate digital & analog region
- **Full-custom** digital design
  - *Minimize area*

Pixel design: TJ-Monopix



- Front-end derived from the ALPIDE detector
  - *Benefit from small C_d (~ 5fF)*
  - *Very **compact** and **low power** FE circuit*
  - *No need for in-pixel threshold trimming*
- Circuit optimized for fast response
  - *Power vs. speed trade-off*

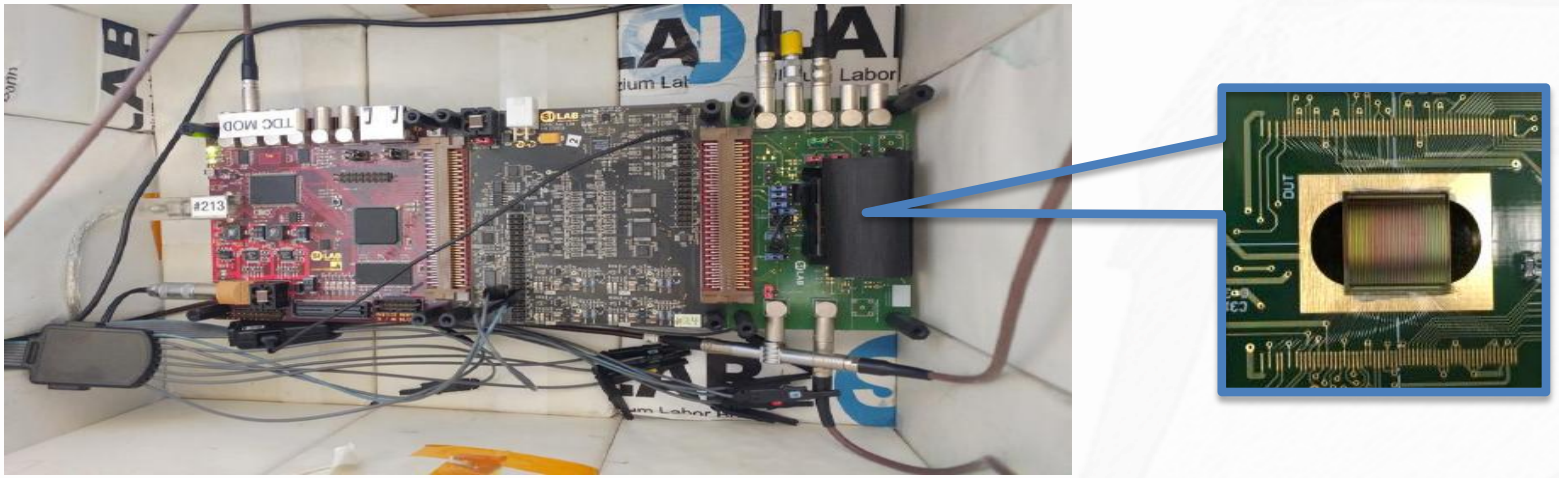
Threshold	300 e^-
ENC	7.1 e^-
Thres. dispersion	10.2 e^-
Time walk	**< 25 ns**
Power	**< 1 µW**

LF-Monopix vs. TJ-Monopix

UNIVERSITÄT BONN

	LF-Monopix	TJ-Monopix
Tech.	LFoundry 150 nm CMOS	TowerJazz 180 nm CMOS
Sensor concept	Large fill factor	Small fill factor
Chip size	~ 1 × 1cm^2	~ 1 × 2cm^2
Pixel array	129 × 36	224 × 448
Pixel size	50 × 250 µm^2	36 × 40 µm^2
Ana. current/pixel	~ 20 µA/pixel	~ 0.5 µA/pixel
Pixel variants	9	4

Key measurement results from LF-Monopix

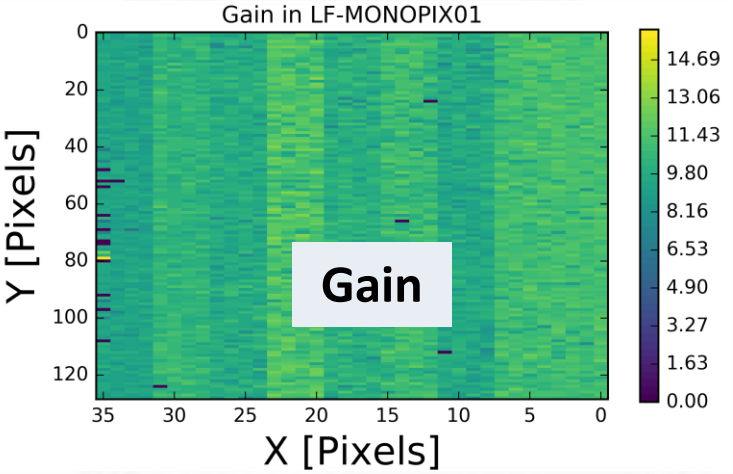


Full read-out firmware & software based on the BASIL framework:
https://github.com/SiLab-Bonn/monopix_daq

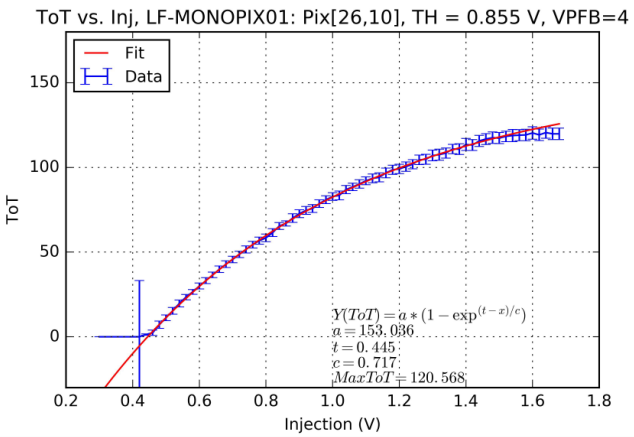
Laboratory results

- Breakdown @ **-280 V** => up to ~ 300 µm depletion
- ToT calibrated with sources: ^{241}Am, terbium
- Gain **10 -12 µV/e$^-$**
- Typical ENC ~ **200 e$^-$**
- Tunable threshold down to **1400 e$^-$**
  - dispersion ~ **100e$^-$**

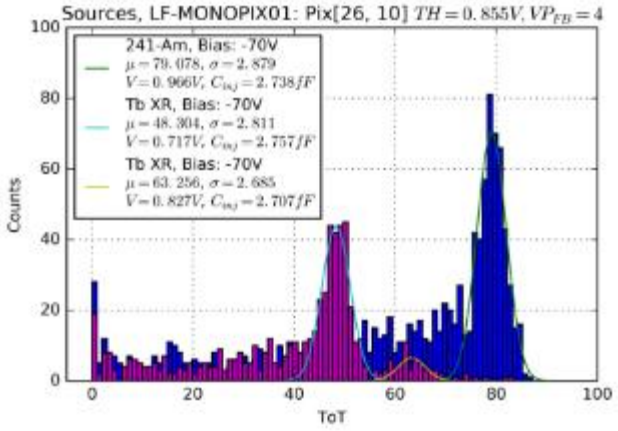
I. Caicedo, Bonn

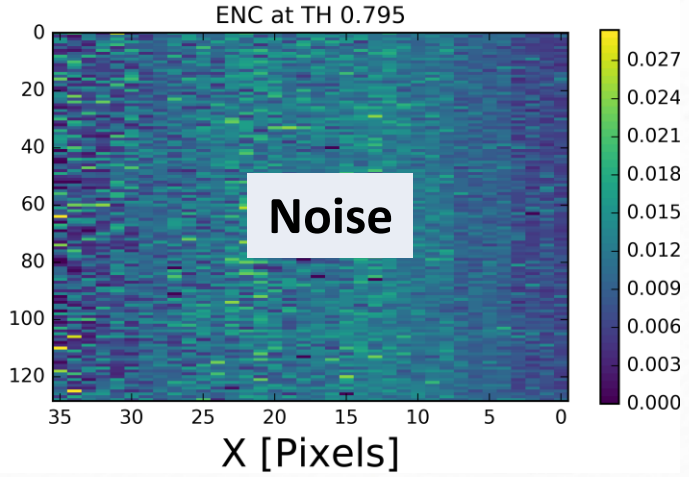


ToT vs. Injection



Response to sources

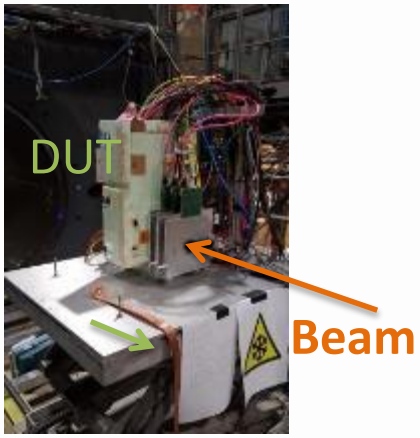




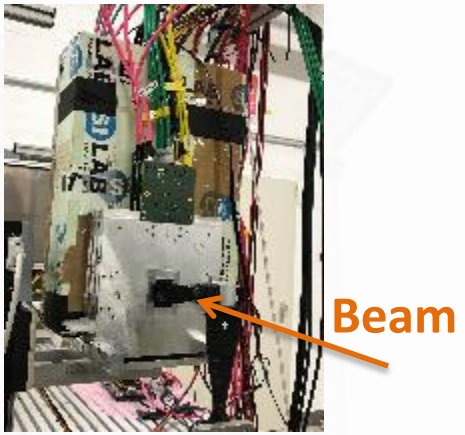
Test beam

UNIVERSITÄT BONN

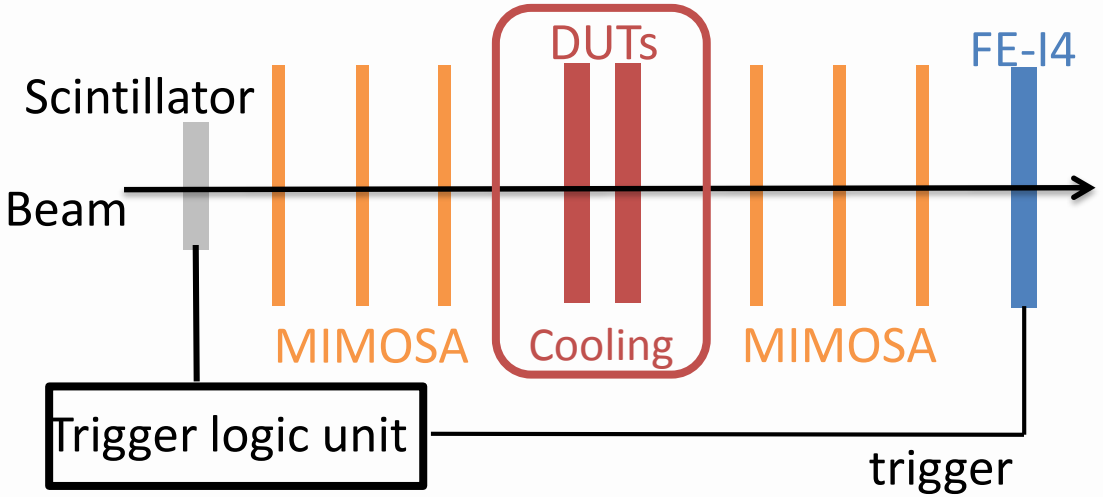
SPS CERN
- 180 GeV pion
- Sep. 20-28, 2017



ELSA Bonn
- 2.5 GeV electron
- Nov. 8-10, 2017



DUTs: 1 non-irradiated + 1 neutron-irradiated $10^{15} n_{eq}/cm^2$



- MIMOSA × 6
  - Pixel size: 18.2 µm × 18.2µm
  - 1152 µs/frame (rolling shutter)
- FE-I4 × 1
  - Pixel size: 250 µm × 50 µm
  - Timing resolution: 25ns
  - Triggered by scintillator + TLU

ANEMONE telescope: https://indico.desy.de/indico/event/18050/session/9/contribution/17/material/slides/0.pdf

ELSA test beam: Efficiency

T. Hirono, Bonn

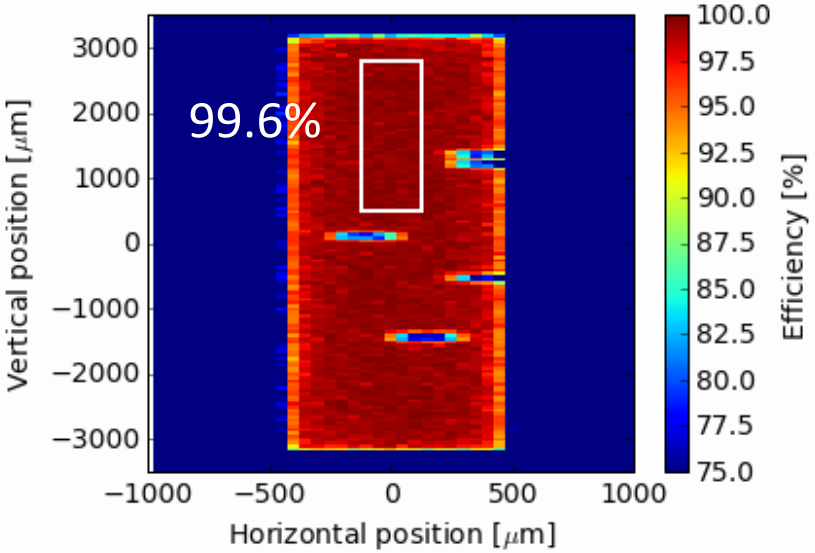
- Non-irradiated

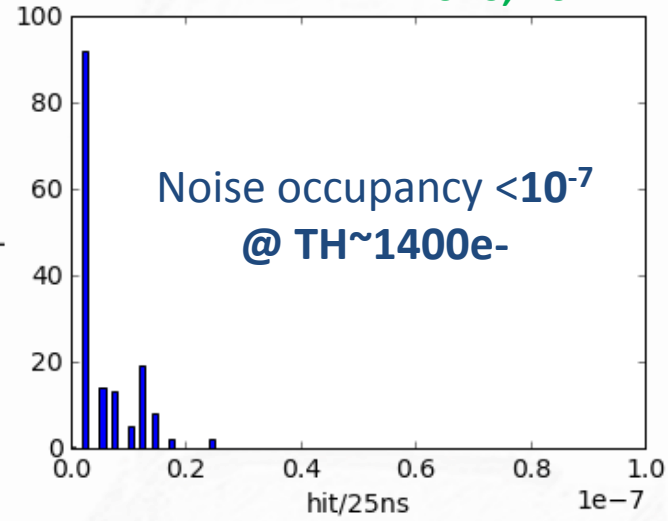
TH tuned by noise

Columns: 16-20

HV: -200V

Temp: dry ice





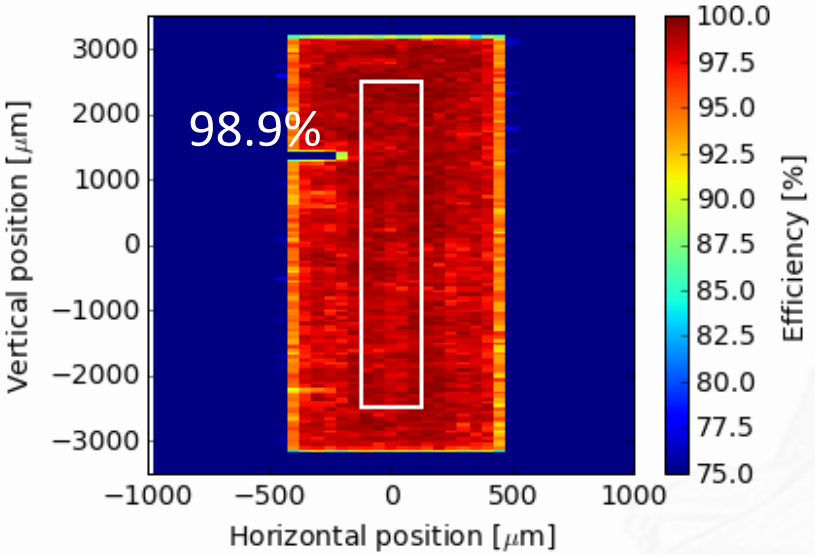
- 1 x $10^{15} n_{eq}/cm^2$

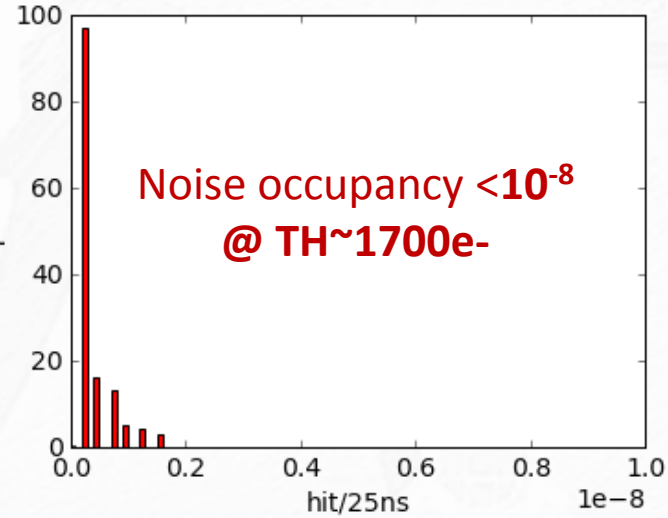
TH tuned by noise

Columns: 16-20

HV: -130V

Temp: dry ice

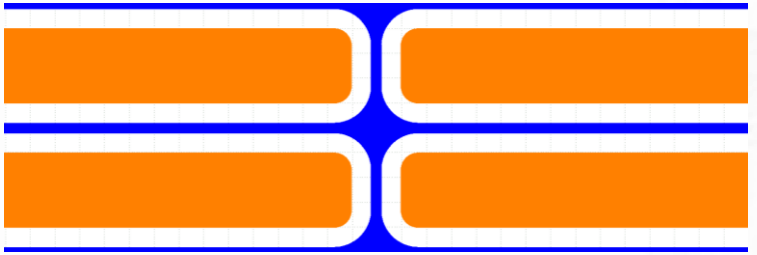




ELSA test beam: In-pixel Efficiency

N-well (collection well)

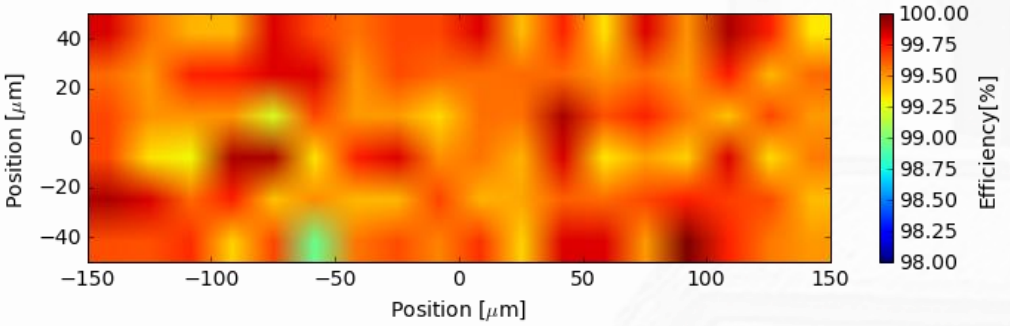
P-well

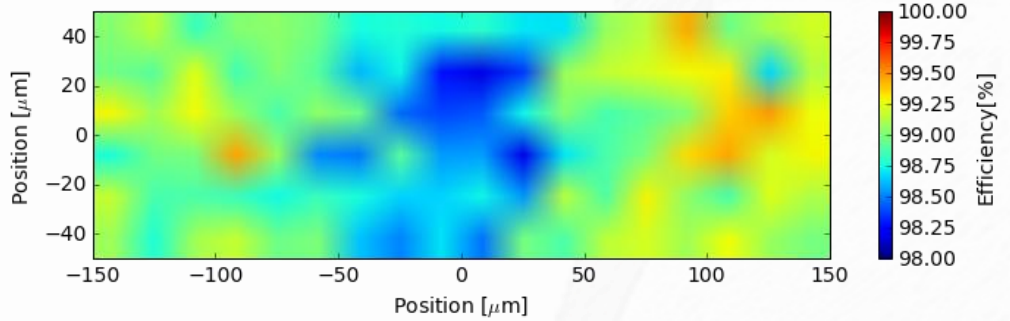


T. Hirono, Bonn

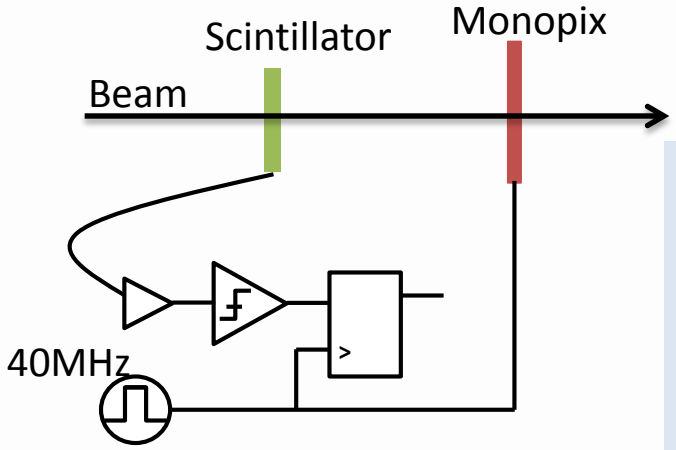
- Non-irradiated

- 1 x $10^{15} n_{eq}/cm^2$





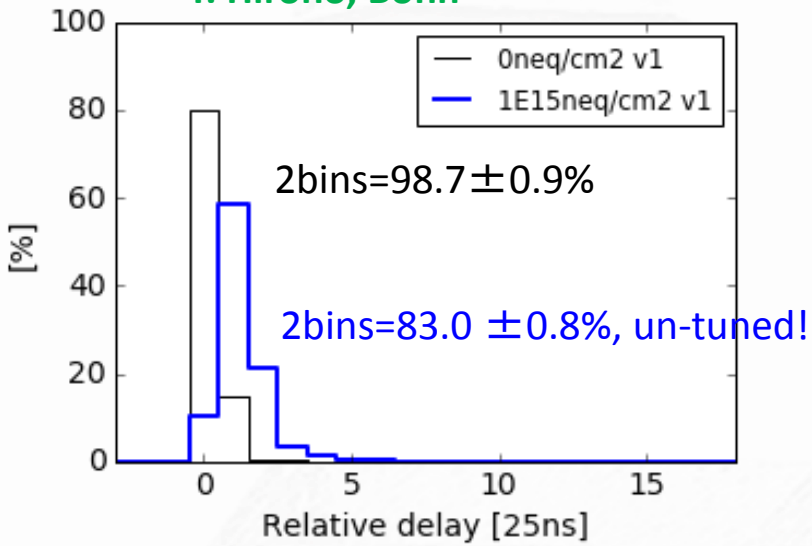
ELSA test beam: Timing performance



TH: ~1700 e-
Columns: 16-20
HV: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
DAC setting: default
Temp: dry ice

Delay = (Monopix LE) - (Scintillator LE)

T. Hirono, Bonn



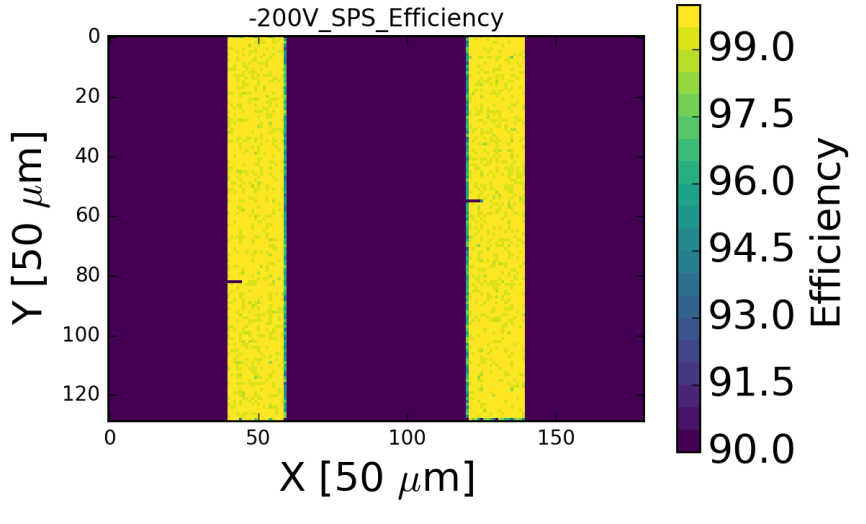
- Promising timing results from non-irradiated chip for 400 fF C_d
  - *Measurement limited by the timing resolution given by the clock cycle*
    => the 2nd bin also includes in-time hits => More precise measurement needed
- Higher time walk for irradiated chip @ default settings, can be improved by
  - *Optimization of DAC settings, e.g. CSA/discriminator bias*
  - *Higher bias voltage + back side process => larger signal*
  - *Time walk correction of "small" hits*

SPS test beam

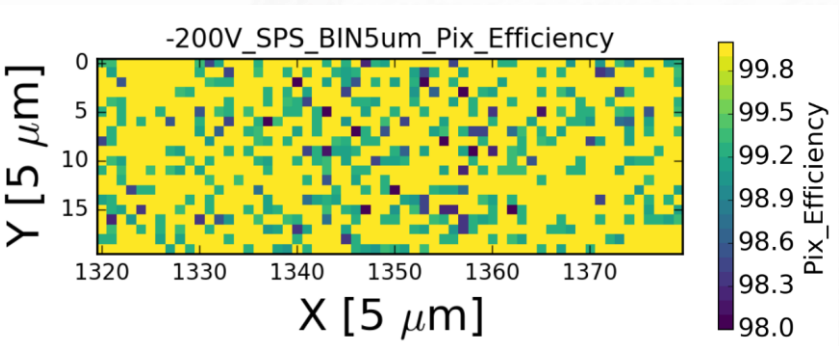
- Analysis finished on non-irradiated sample for the SPS test beam
  - *Columns 8 - 11 & 24 - 27*
  - *Threshold ~ 2700 e-*
  - *Room temperature*

99.7%
@ -200V

I. Caicedo, Bonn

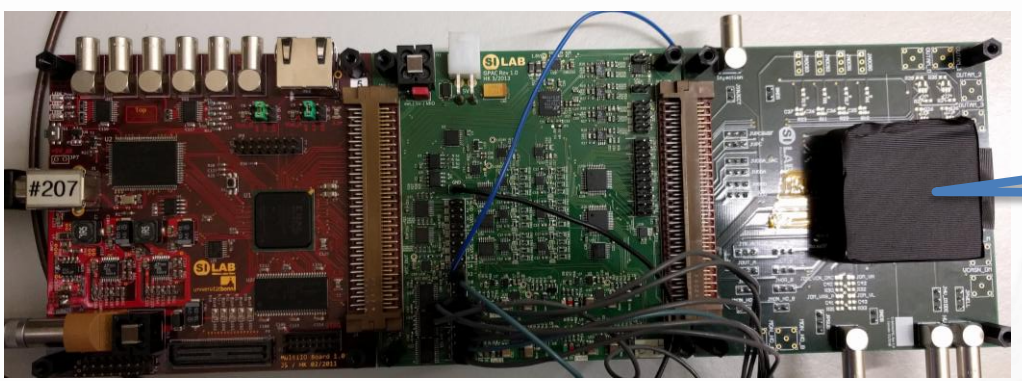


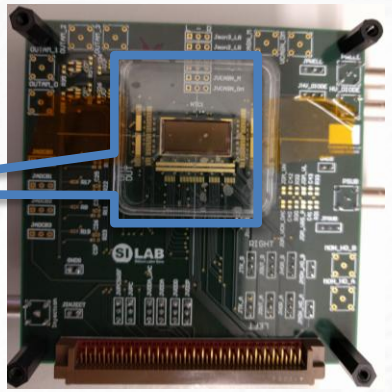
Uniform in-pixel efficiency
@ -200V



First sign of alive for TJ-Monopix

Chip received on 09/02/2018
Wired bonded on 16/02/2018

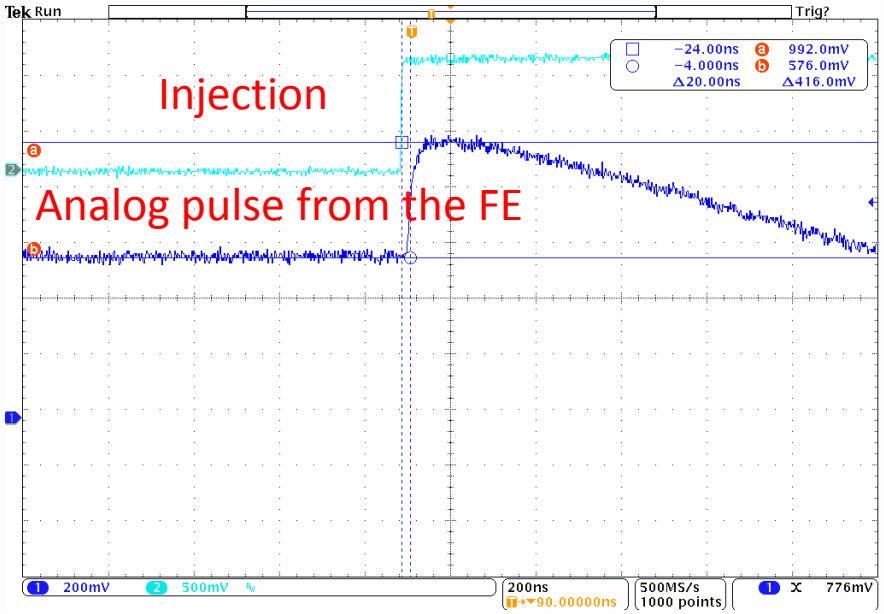


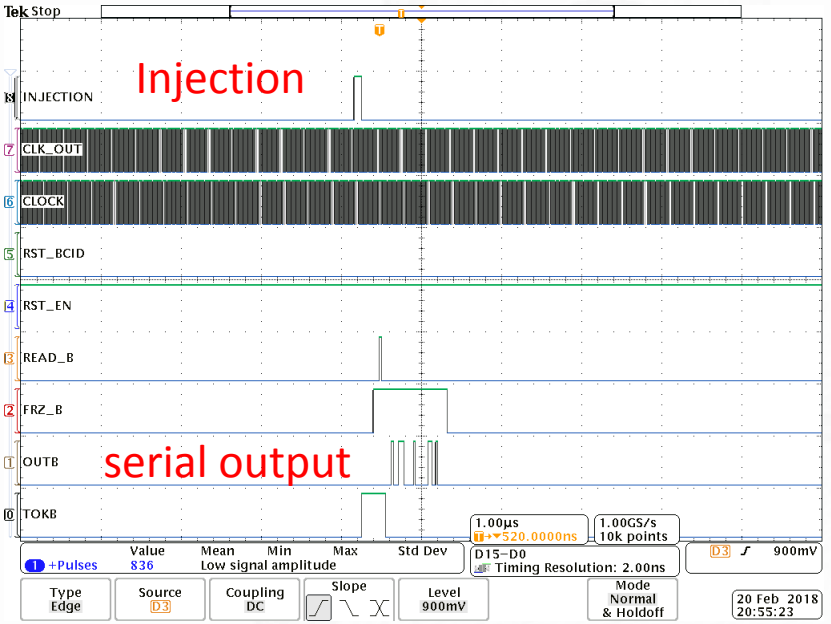


Measurement with charge injection

- Analog monitoring
- Full monolithic readout chain

K. Moustakas, Bonn





The chip shows full functionality already!

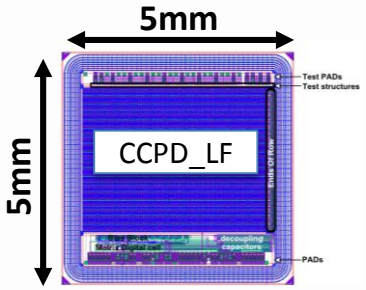
Summary

- Two large scale DMAPS demonstrator chips developed for the ATLAS ITk
  - *Aimed for the outermost pixel layer:* ***cheap module***, ***simple assembly***
  - *Different sensor concepts pursued:* ***large & small fill factor***
  - ***Column drain readout*** *for sufficient rate capability with affordable in pixel logic density*
- **LF-Monopix**, at least matrix-wise, is a **fully functional** LHC pixel chip
  - *Fully monolithic readout, 40 MHz time stamping, tunable threshold, etc.*
  - *High efficiency* ***~99%*** *after* ***1 x $10^{15} n_{eq}/cm^2$*** *@ very low noise occupancy* ***< 10^{-8}***
    => ***meet the ATLAS spec.***
  - ***Good timing performance*** *already @ default setting => will be improved by tuning*
  - *Wafer thinned down to 100 µm and backside processed soon available (sent for dicing)*
    => better charge collection after irradiation expected
- **TJ-Monopix** is **fully functional now**, more results will come soon
  - *Chip samples sent for neutron irradiation up to 2 x $10^{15} n_{eq}/cm^2$ @ JSI Ljubljana*
  - *Test beam planned for April/May*

Thank you!

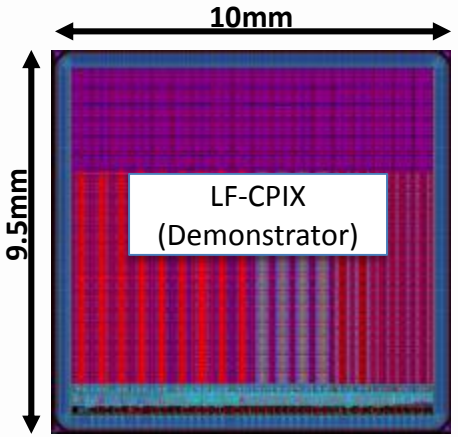
Back up

LFoundry prototypes



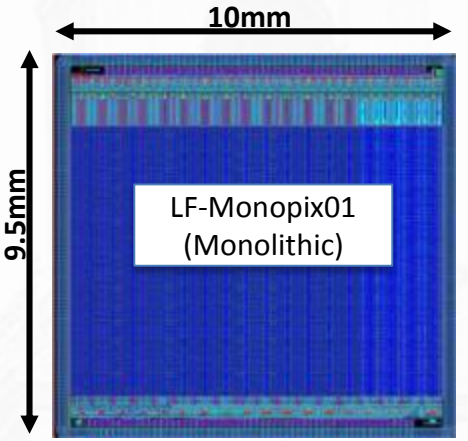
CCPD_LF

- *Subm. in **Sep. 2014***
- *33 x 125 µm² pixels*
- *Fast R/O coupled to R/O chip*
- *Standalone R/O for test*



LF-CPIX (DEMO)

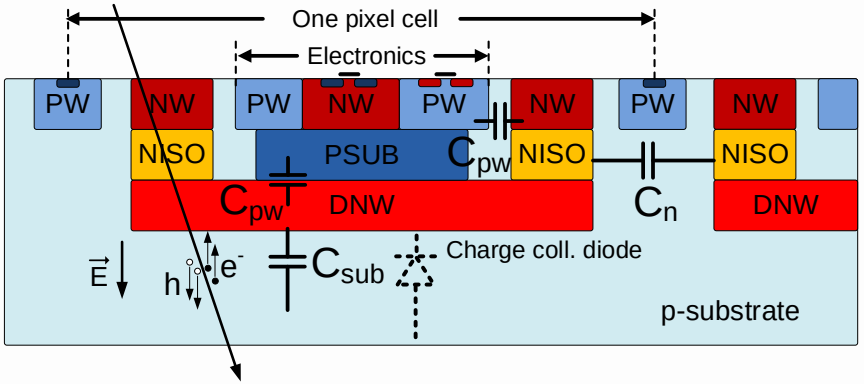
- *Subm. in **Mar. 2016***
- *50 x 250 µm² pixels*
- *Fast R/O coupled to R/O chip*
- *Standalone R/O for test*

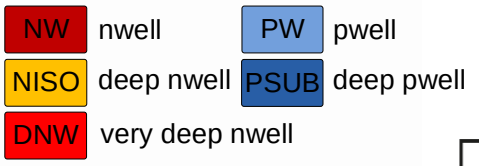


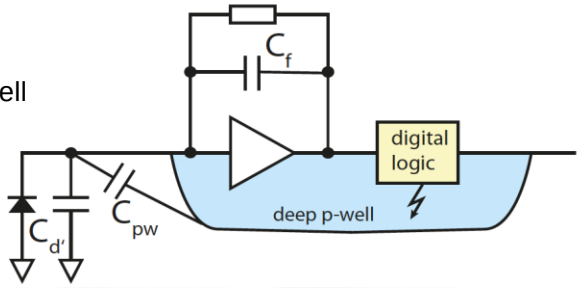
LF-Monopix

- *Subm. in **Aug. 2016***
- *50 x 250 µm² pixels*
- ***Fast standalone R/O***
- *Standalone R/O like LF-CPIX*

Design challenges for LF-Monopix







- Large detector capacitance $C_d = C_{sub} + C_n + \mathbf{C_{pw}}$
  - ***C_{pw}*** *tends to be* ***dominant*** *=> depends on electronics area & DNW/PW junction width*
  - *Timing*

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$$

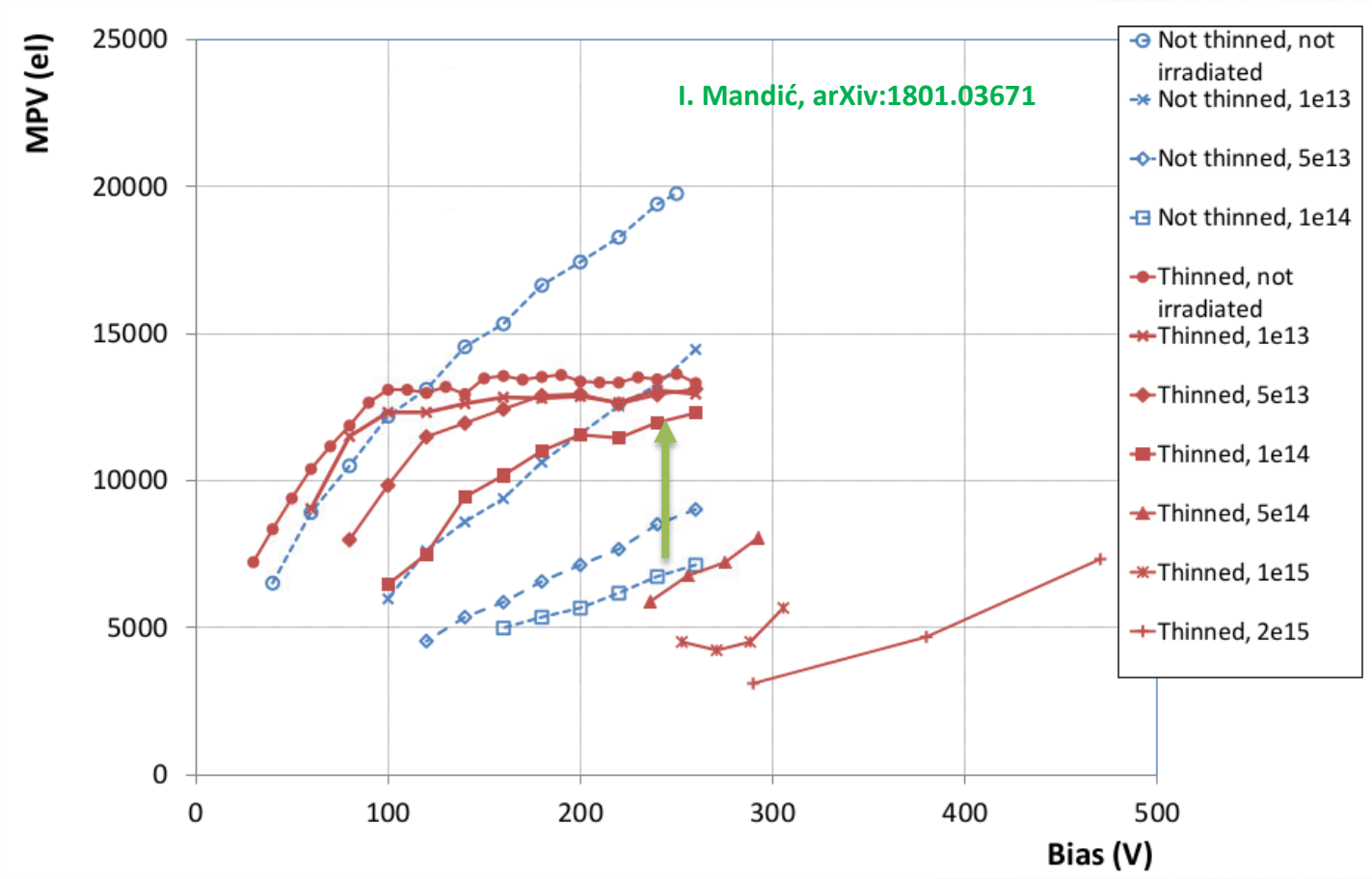
  - *Noise*

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$$

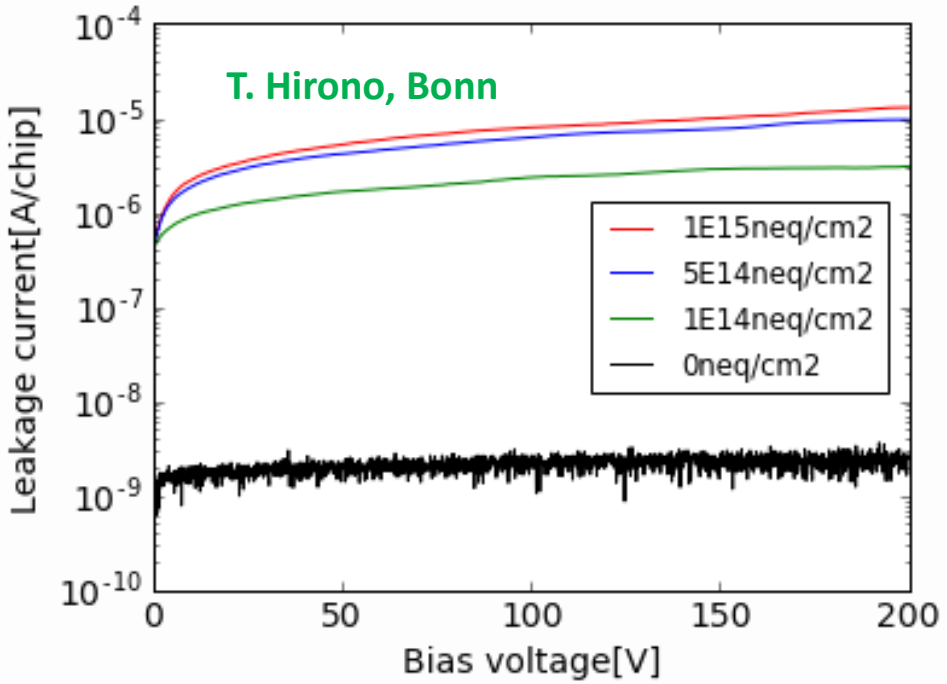
More ***power*** needed to compensate => $g_m \propto I_d$

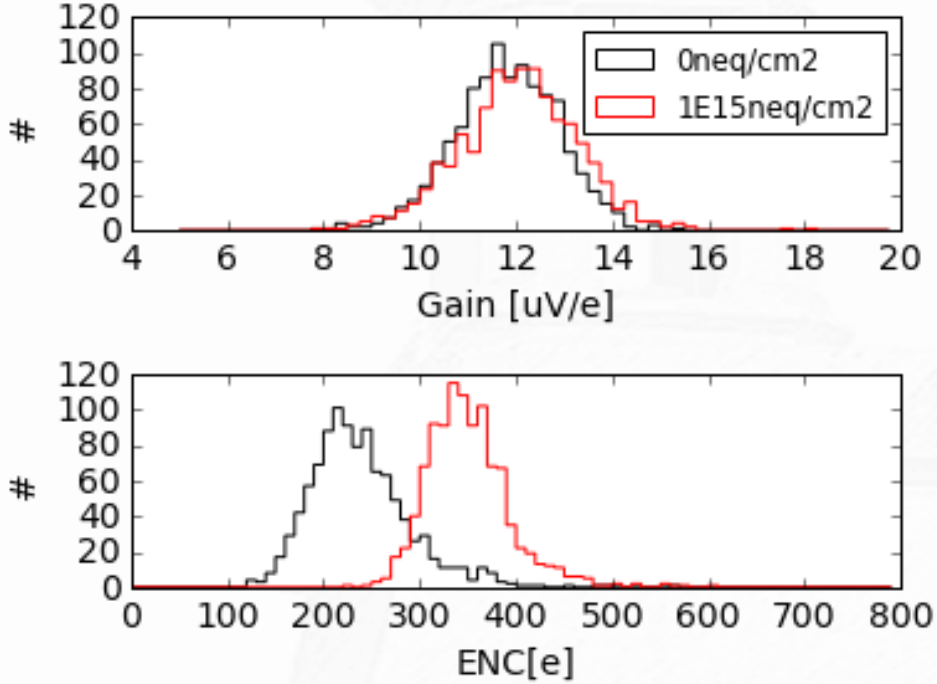
  - *Cross talk => C_{pw} directly couples the substrate noise into the sensor*
    - *The minimum operation threshold may be affected*

Improvement after back-side processing



NIEL: LF-Monopix



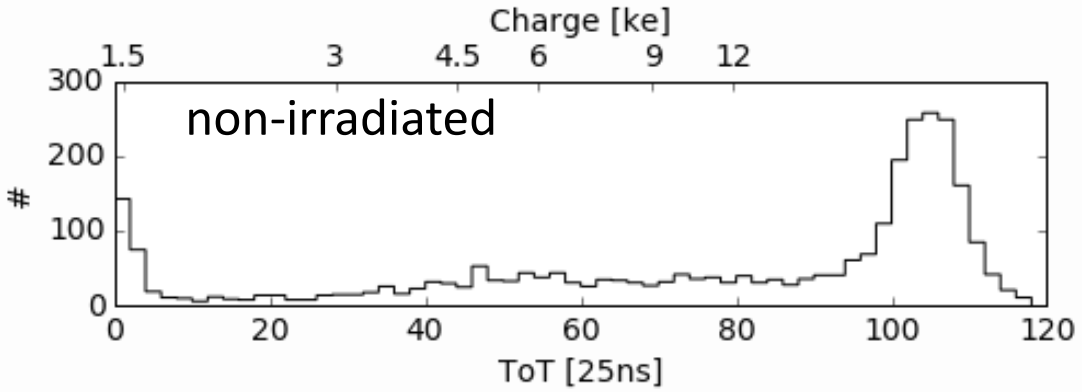


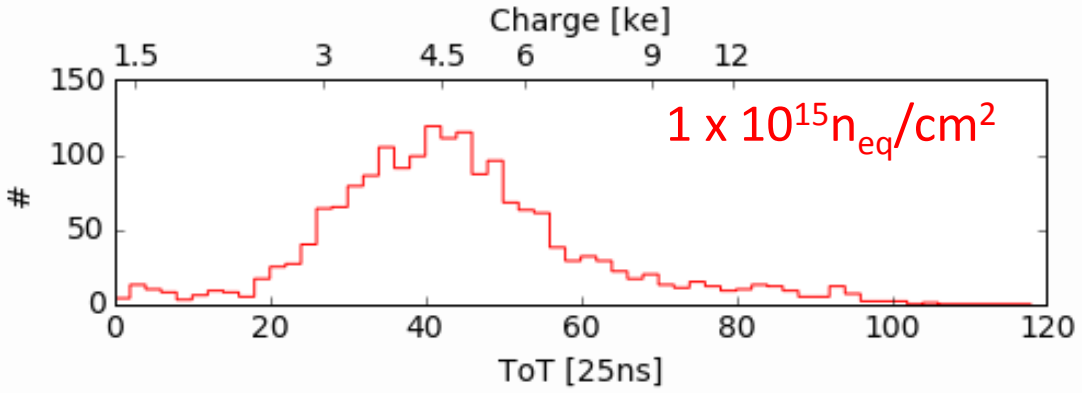
- No breakdown after 200V
- Noise increase => 1 Mrad back ground?

Charge spectrum

UNIVERSITÄT BONN

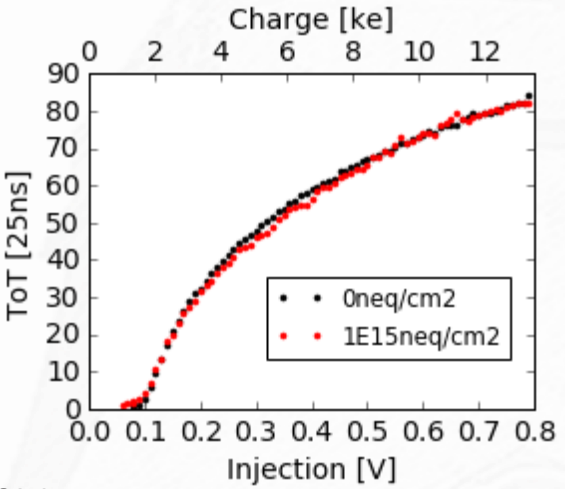
❑ ToT values of seed pixel





Threshold: 1500 e
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
Flavor: CMOS V1
DAC setting: Default
Source: 2.5GeV electron
Temperature: cooled by dry ice

❑ Injection vs ToT



- Un-irradiated ~20ke at -100V, irradiated ~4.5ke at -130V
- The MPV is decreased after neutron irradiation.

ELSA test beam: Noise occupancy

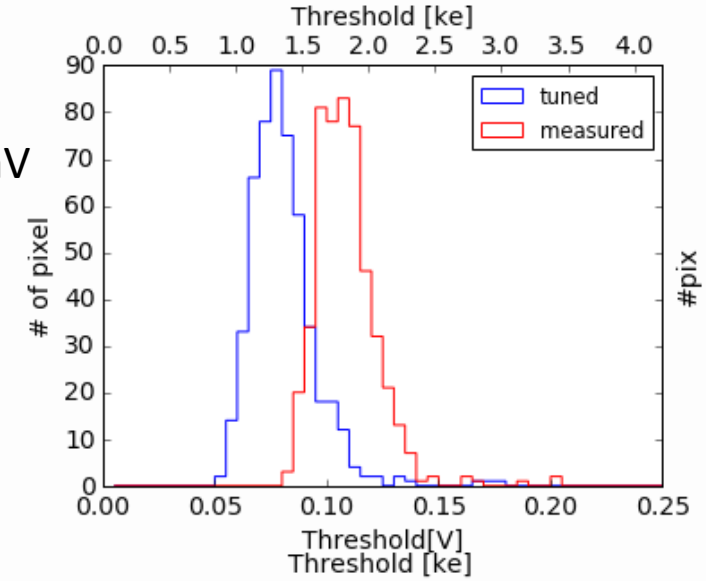
- Non-irradiated

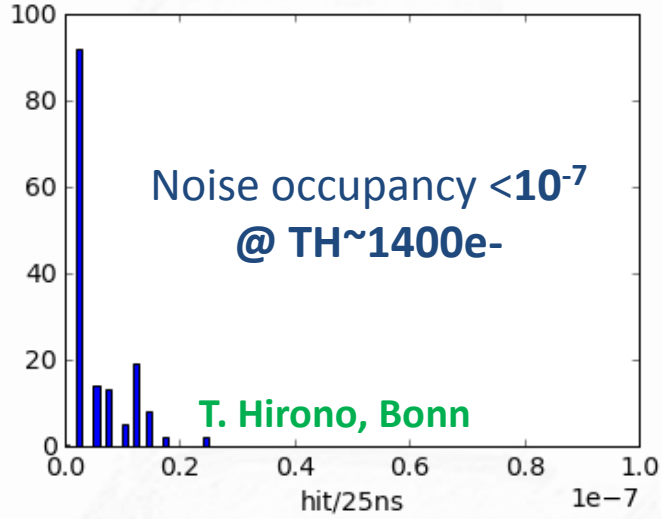
  TH: tuned by noise + 4mV

  Columns: 16-20

  HV: -200V

  Temp: dry ice





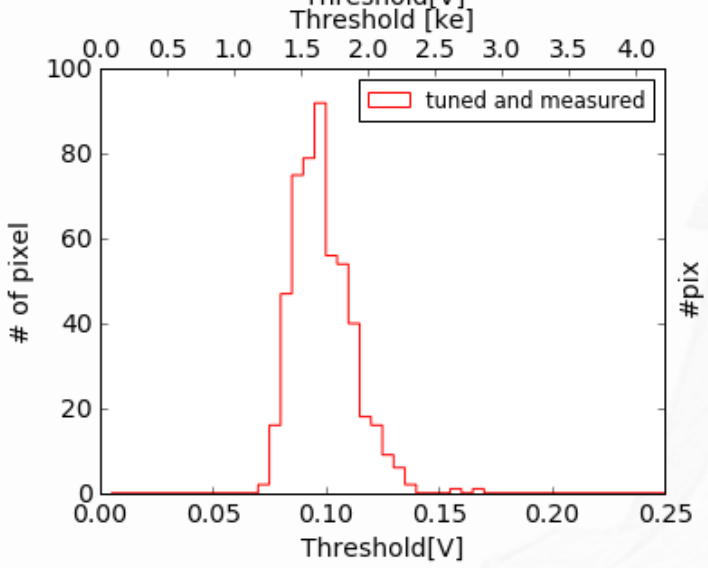
- $1 \times 10^{15} n_{eq}/cm^2$

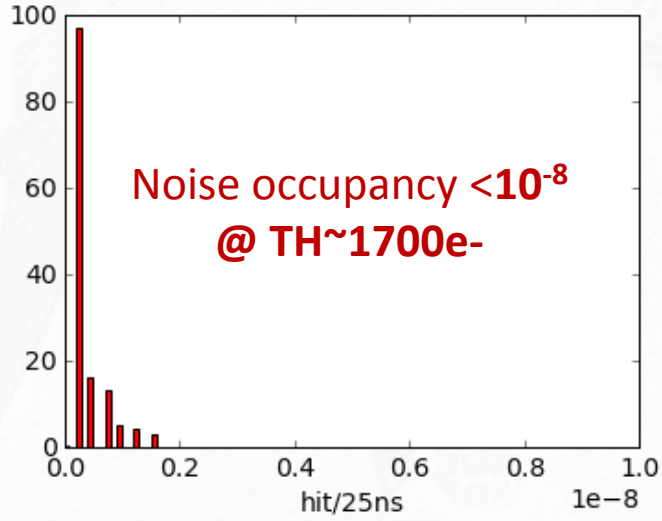
  TH: tuned by noise

  Columns: 16-20

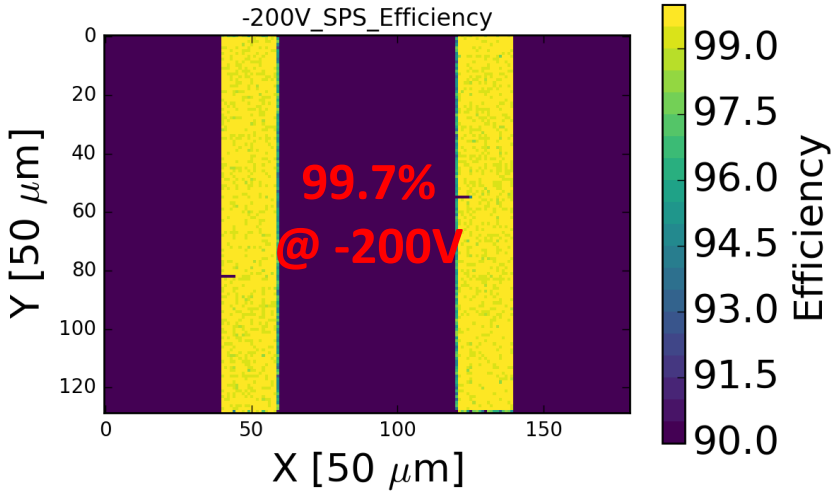
  HV: -130V

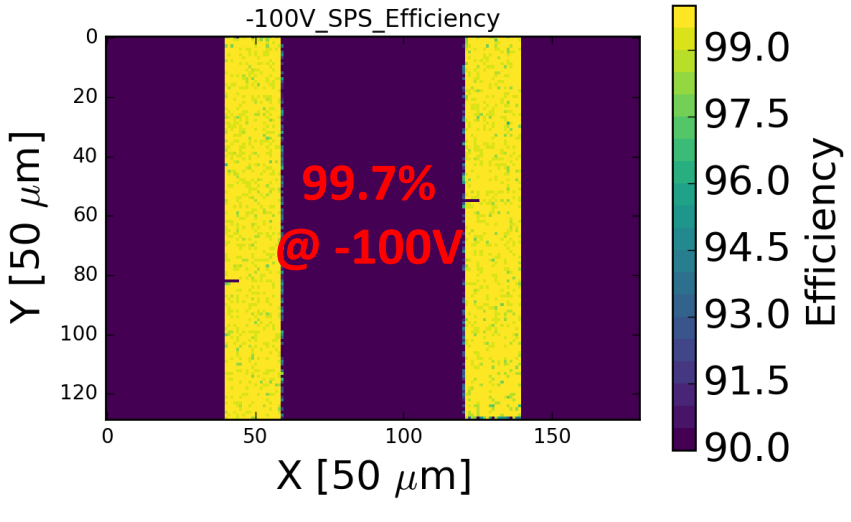
  Temp: dry ice

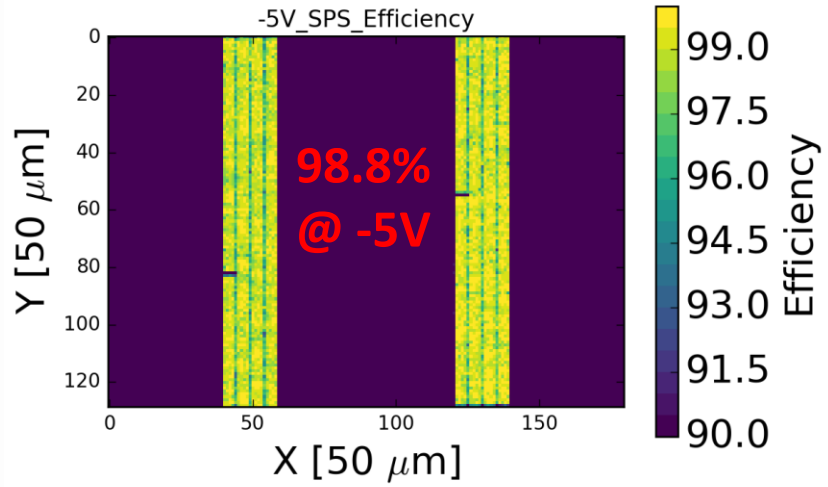




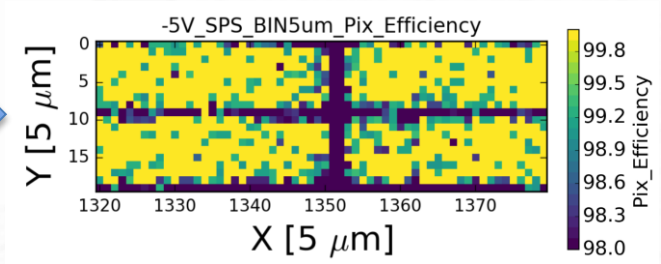
Efficiency @ SPS test beam: LF-Monopix







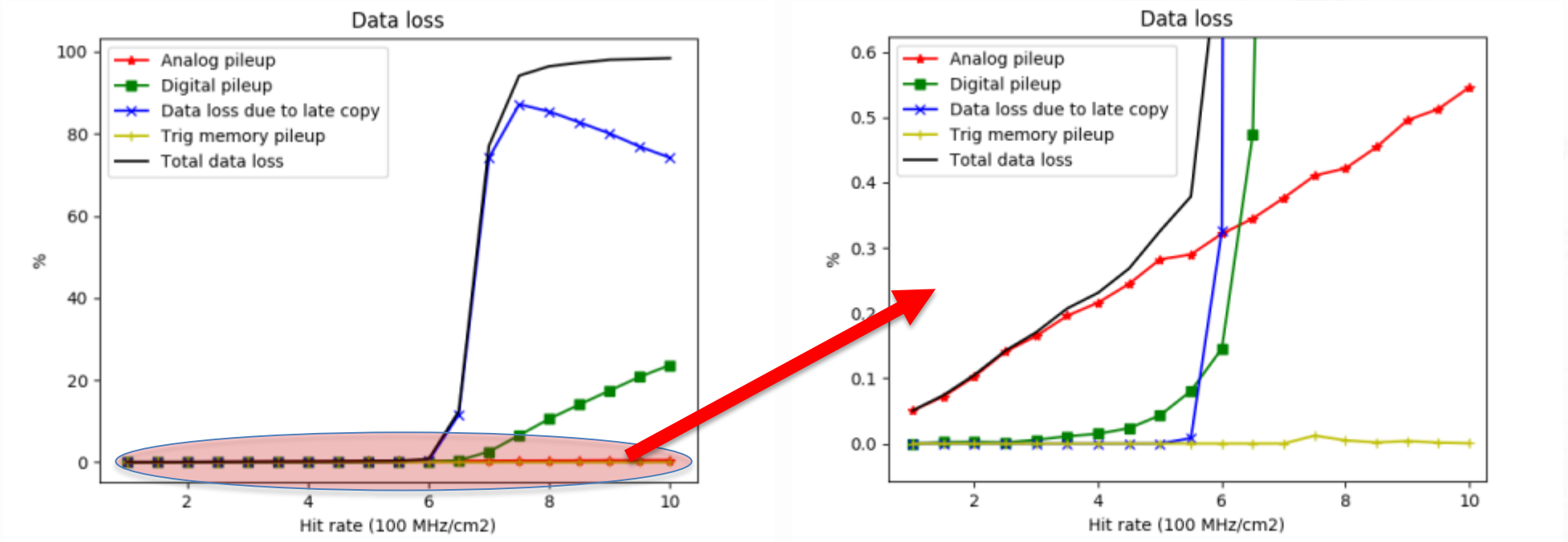
Lower efficiency due to less signal @ low bias
=> Efficiency drop between pixels



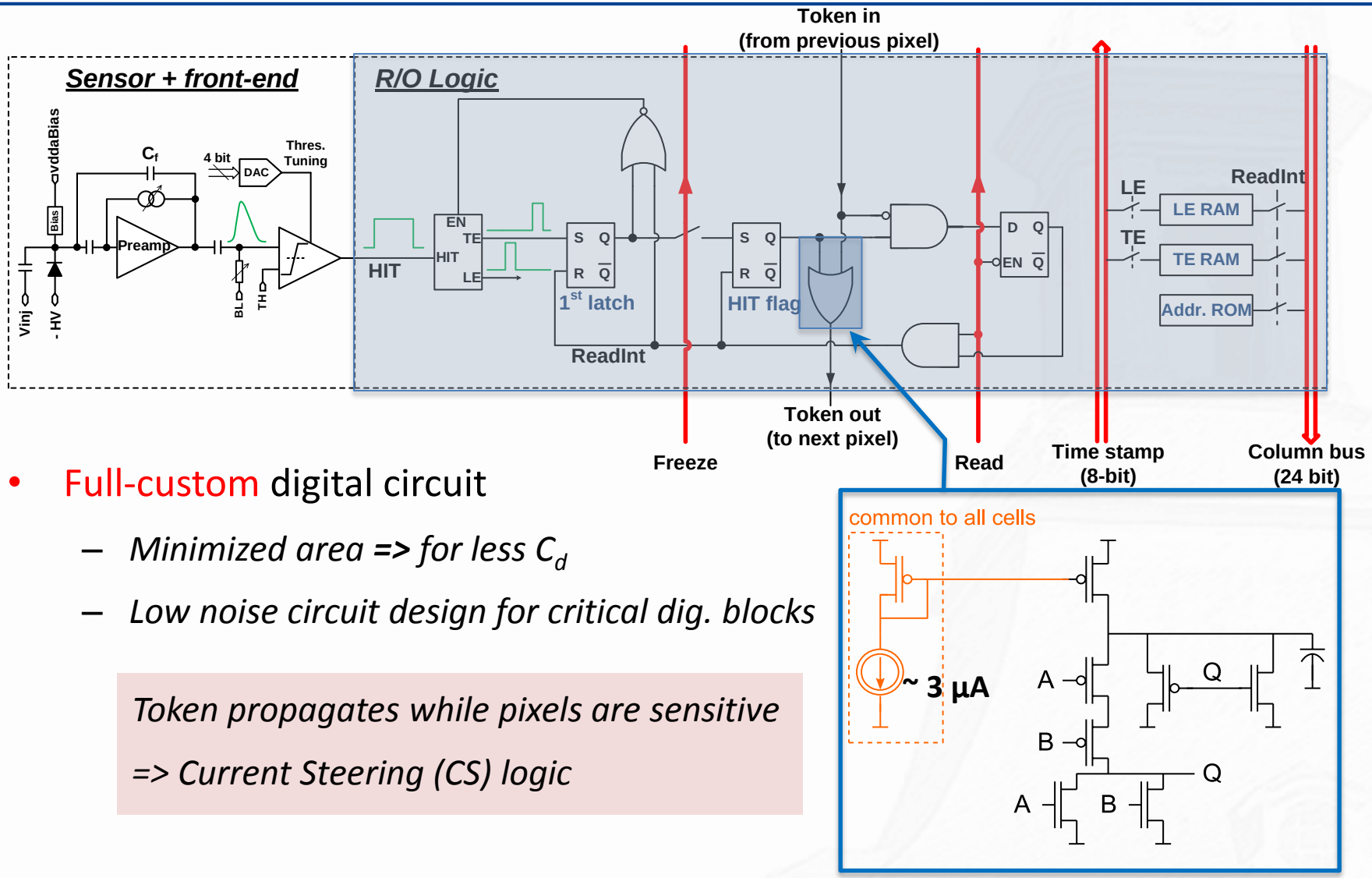
Rate capability of TJ-Monopix – the matrix

- It is assumed that in the final prototype
  - 2 double columns per r.o. unit **=>** 512 × 4 pixels
  - 20 MHz column bandwidth: **50 ns (2 BC)** per hit readout

    => a simple math: max. allowed hit rate = 1/column bandwidth = **0.5 hit/r.o.unit/BC**
- Inefficiency caused by trig. memory pileup not included here **=>** pure matrix performance
- Data loss increases steeply beyond **600 MHz/cm² => ~ 0.44 hits/r.o.unit/BC**



Pixel design: LF-Monopix

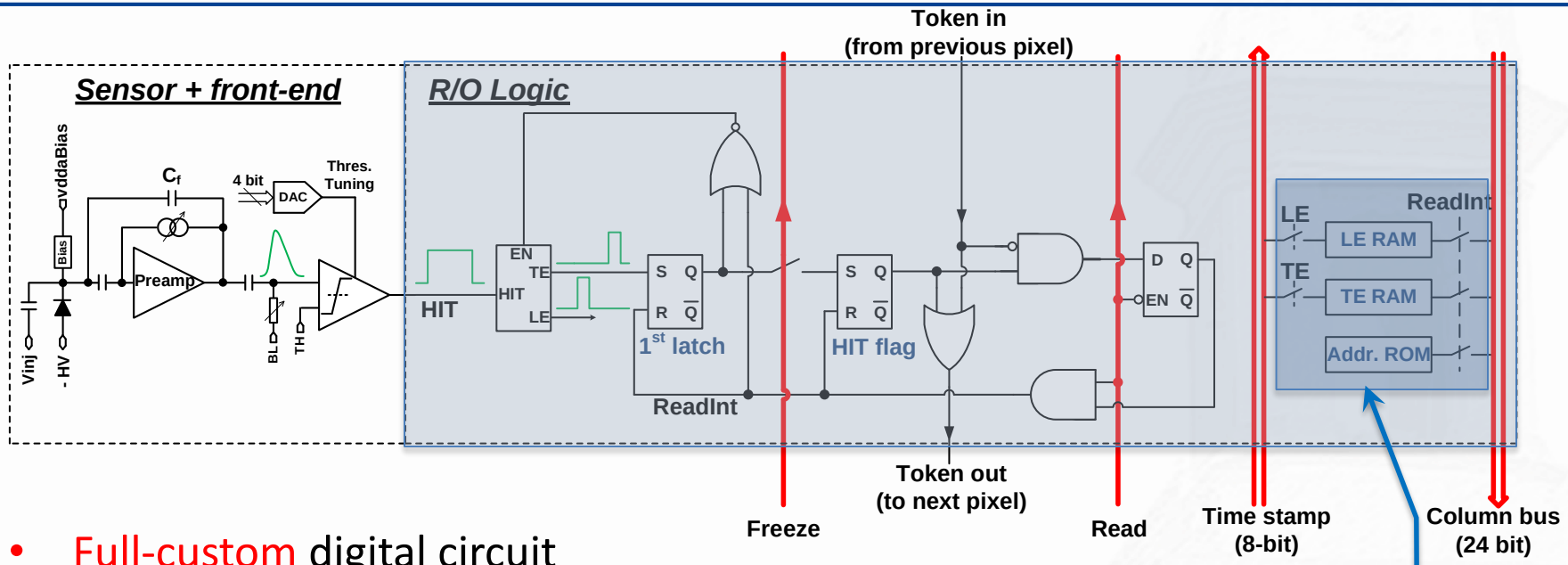


- Full-custom digital circuit
  - *Minimized area => for less C_d*
  - *Low noise circuit design for critical dig. blocks*

Token propagates while pixels are sensitive

=> Current Steering (CS) logic

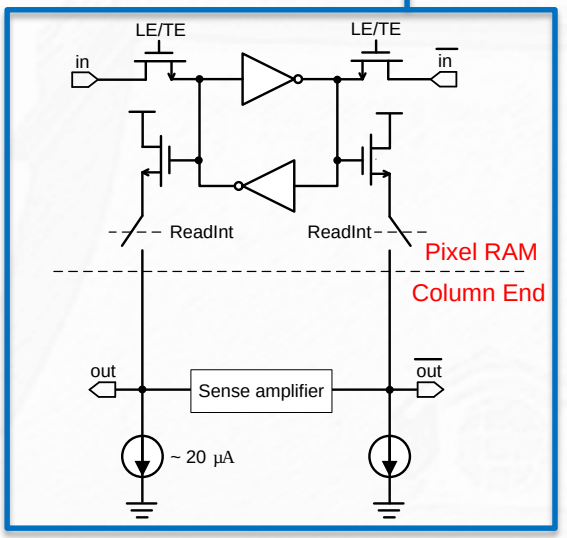
Pixel design: LF-Monopix



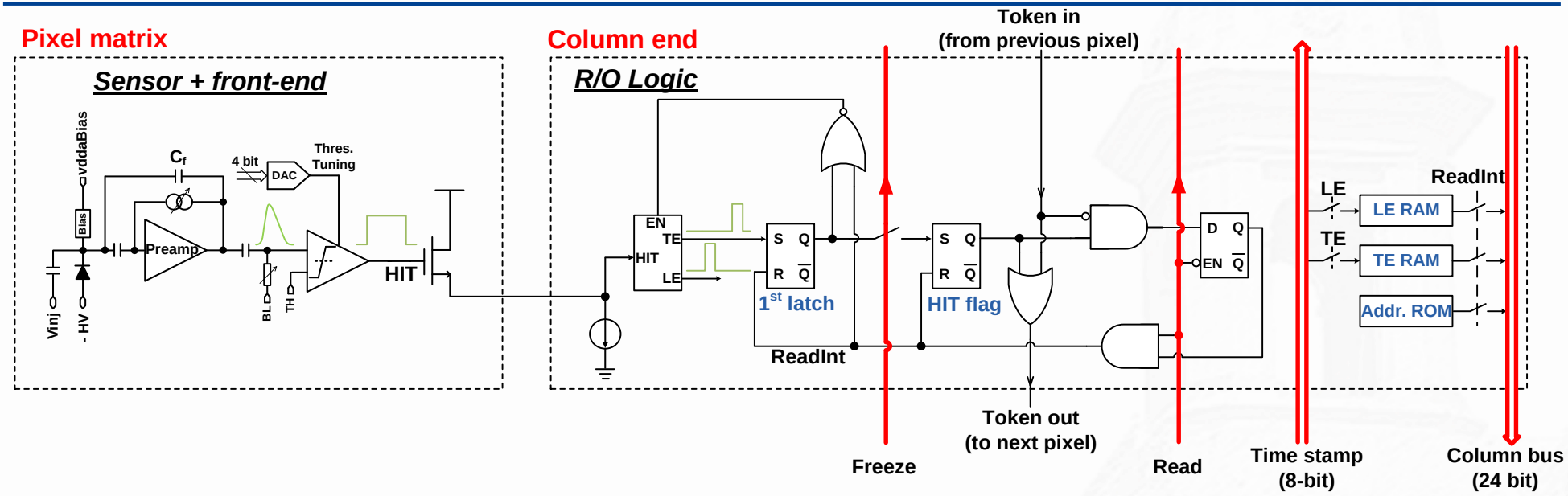
- Full-custom digital circuit
  - *Minimized area => for less C_d*
  - *Low noise circuit design for critical dig. blocks*

RAM cell R/O by source follower

=> Avoids high current injection into PW



Pixel design: LF-Monopix



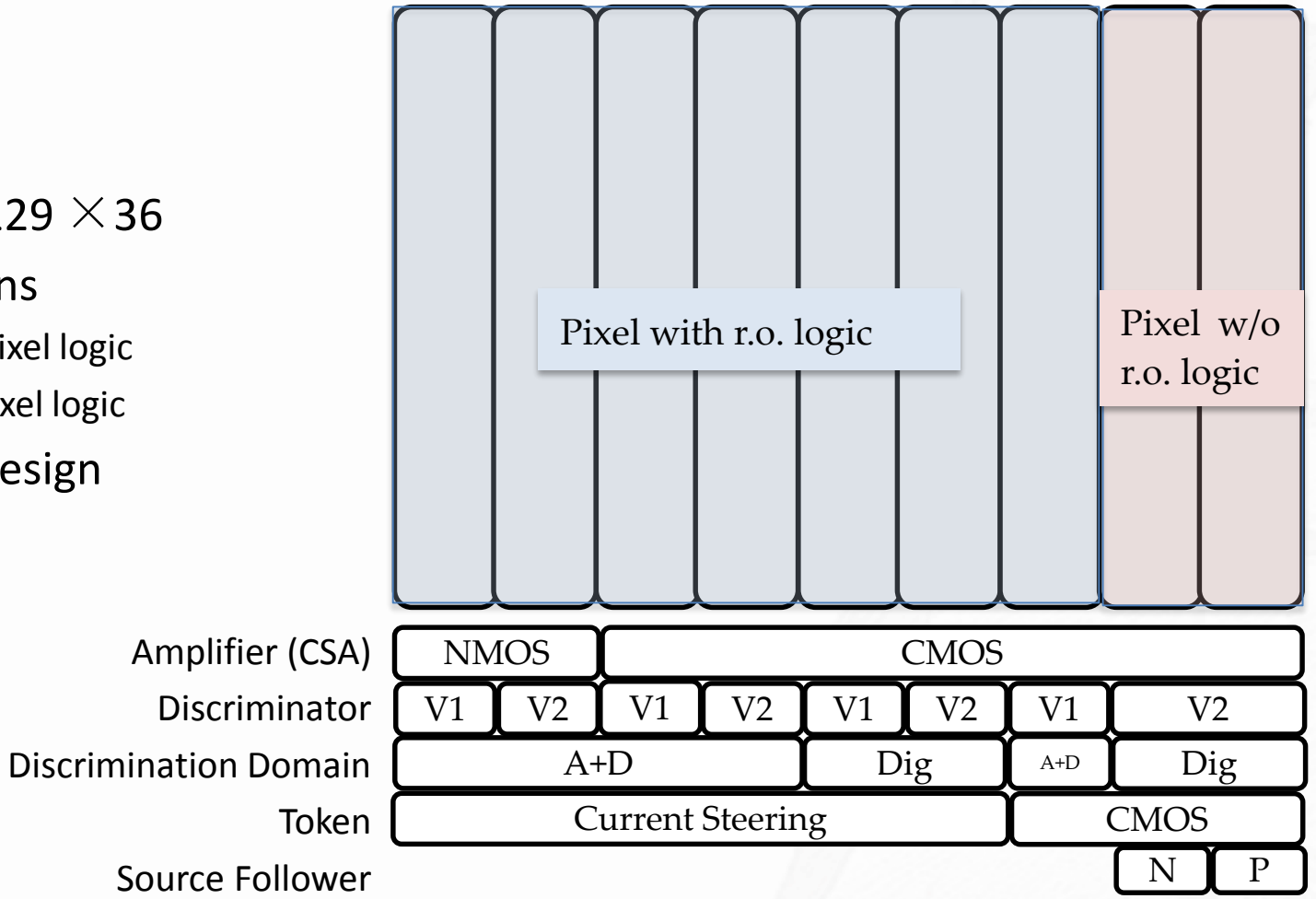
- We can move the in-pixel r.o. logic to the periphery
  - *Discriminator output r.o. by source follower*
  - *Less area needed for in-pixel electronic => less C_d*
  - *Almost no in-pixel digital transient*
  - *Almost no signal distributed in the column*

  } => *less* noise/cross talk

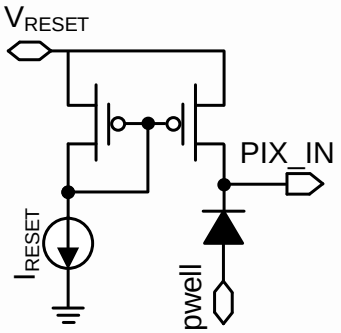
  - *One-to-one connection from pixel to R/O logic => Complex routing*

Pixel array: LF-Monopix

- Pixel array: 129 × 36
- 9 pixel designs
  - 7 with in-pixel logic
  - 2 w/o in-pixel logic
- 4 columns/design

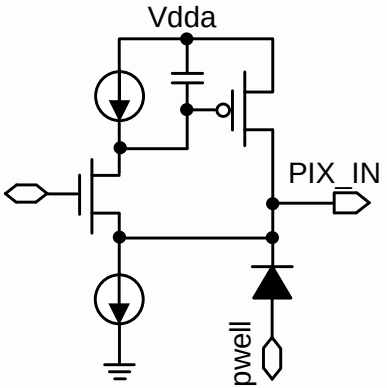


Pixel design: TJ-Monopix



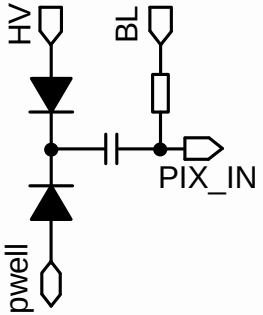
PMOS reset

- Used in previous TJ chips
- I_{RESET} should be larger than max. leakage



Adaptive PMOS reset

- Reset PMOS adaptively biased by a feedback loop
- Less sensitive to leakage increase after irradiation

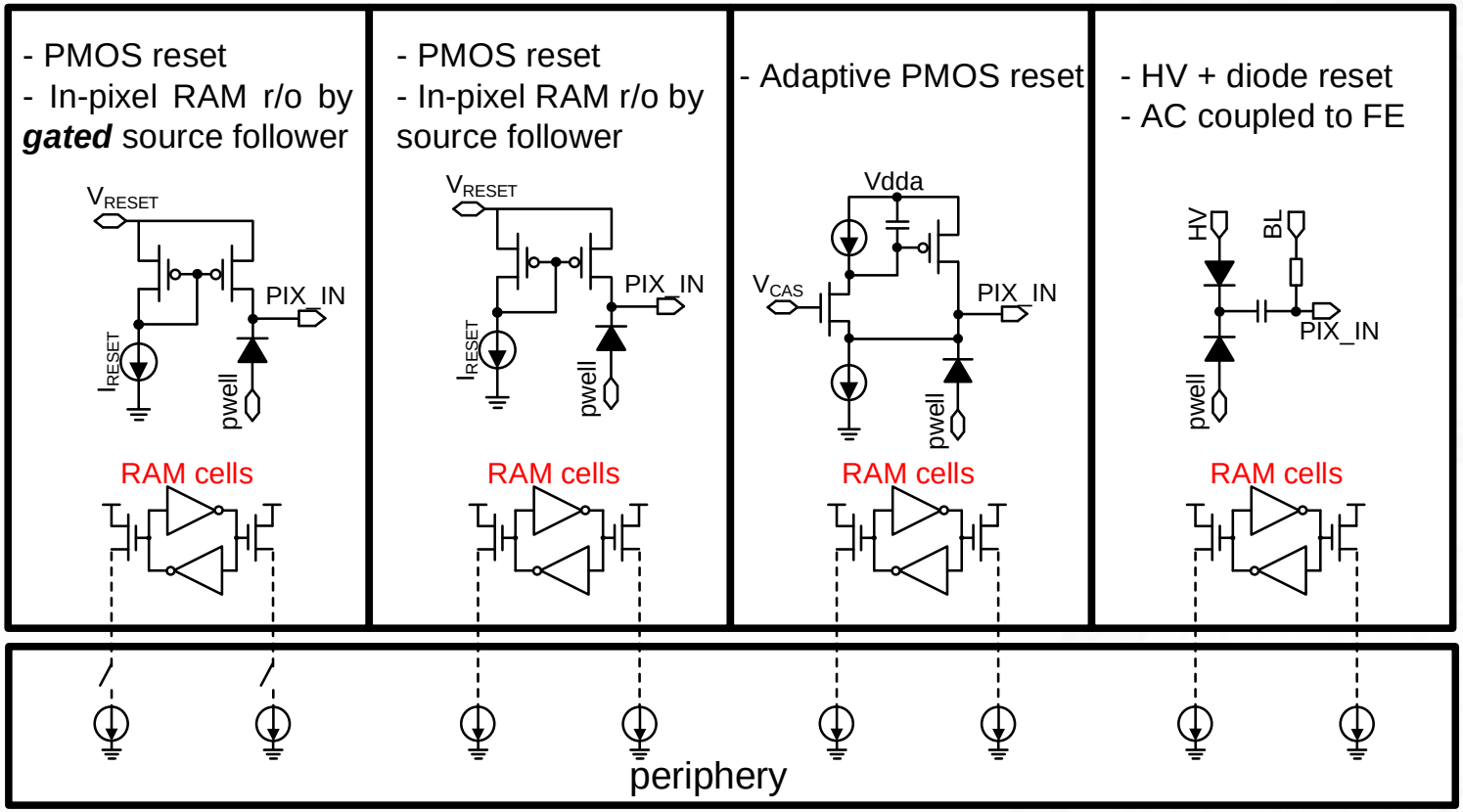


Diode reset with HV bias

- Front-side HV to further enhance the depletion
- Diode reset for HV compatibility
- Sensor AC coupled to the FE

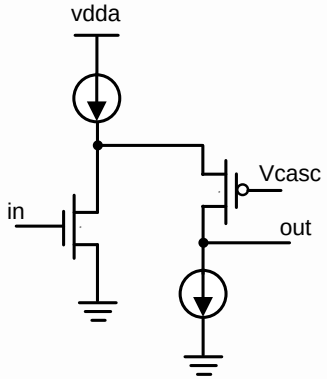
Pixel array: TJ-Monopix

- Pixel array 224 × 448, composed of equally divided 4 sub arrays

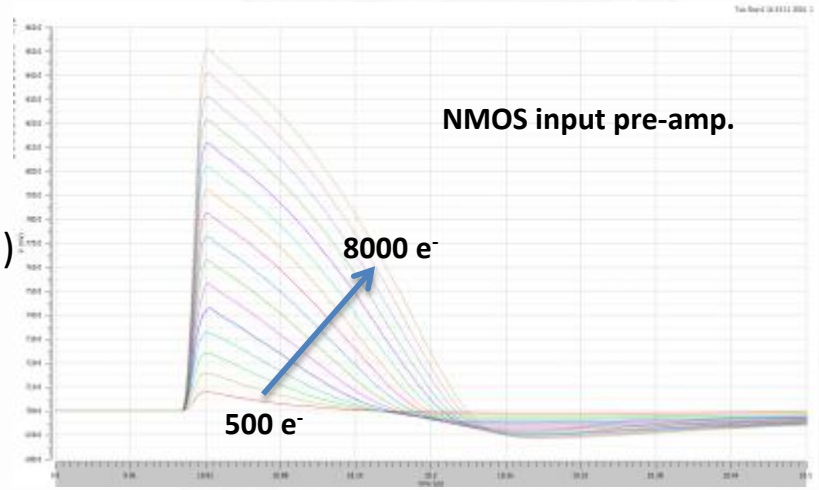


LF-Monopix: timing

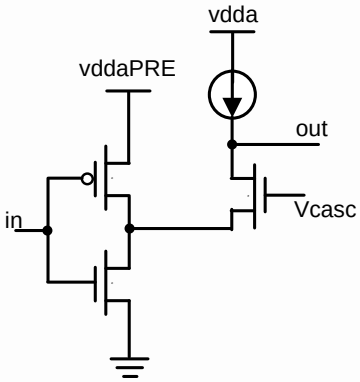
- Pre-amplifiers => aimed at peaking time $\lesssim$ 25 ns with 400 fF C_d
  - NMOS input: modified from LF-CPIX in order to deal with the increased C_d



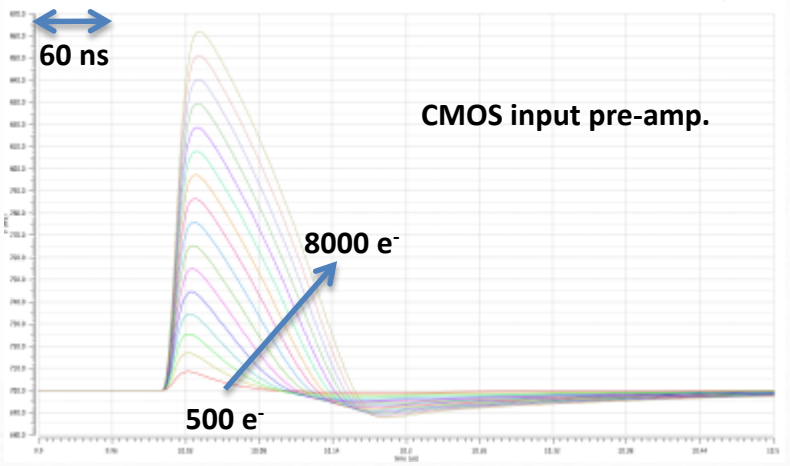
- ❑ Bias current ~ 17 µA
- ❑ peaking time ~ 20 ns (4 ke$^-$ signal)
- ❑ ENC ~ 170 e$^-$



  - CMOS input: same as LF-CPIX

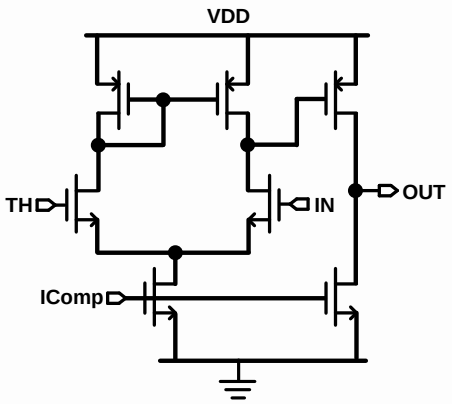


- ❑ Bias current ~ 15 µA
- ❑ peaking time ~ 25 ns (4 ke$^-$ signal)
- ❑ ENC ~ 135 e$^-$

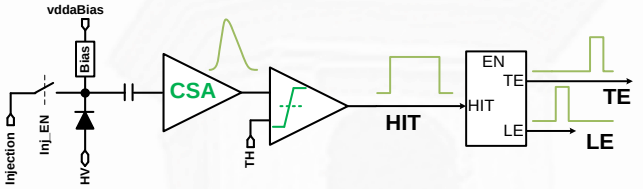


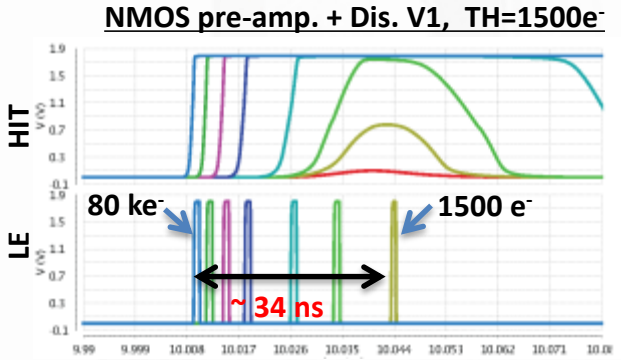
LF-Monopix – timing

- Time walk also depends on discriminator design
  - Discriminator V1: same as LF-CPIX

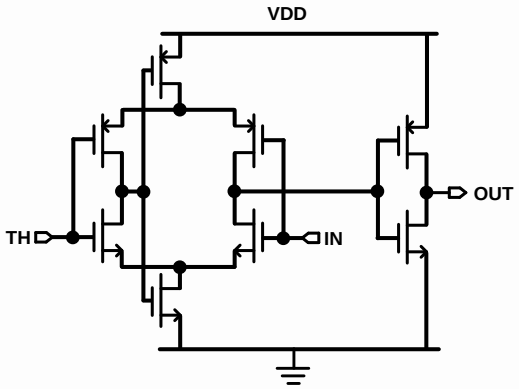


- ❑ 2-stage amplifier as comparator
- ❑ bias current: 4.5 µA
- ❑ slow at threshold edge

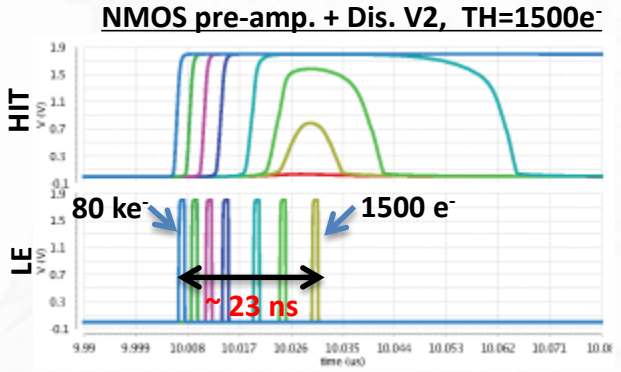




  - Discriminator V2:



- ❑ Two amplifiers load each other
- ❑ self biased: < 4µA
- ❑ CMOS inverter as 2nd stage



Front-end simulation performance

Charge threshold Q_{th}	300 e	
Equivalent Noise Charge	7.1 e	threshold/noise > 10
Channel-to-channel RMS	10.2 e	good threshold uniformity, no need for in-pixel tuning

Time-Walk