Module and Ladder Testing at MPP

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Standardized Testing Procedure: Handbook

handbook

- LaTeX document to produce PDF with step by step instructions for the testing
- starting with a description of the software versions used
- mechanical instructions for module handling, i.e. mounting to the setup
- instructions on how to perform each test, check for the results and update HephyDB
- idea: **complete set of testing instructions**
- shared as feature branch pull request in the lab_framework repository currently commented, discussed and edited by the lab groups

handbook.pdf on bitbucket

The testing procedure of the main production modules is following the instructions of the handbook. Therefore, it is the same for each module and at each testing location.

Testing Infrastructure at MPP

performing of the module tests

- two module setups: pxdtest1 and pxdtest8
- one ladder setup: pxdtest9

storage of measurement data

- first: locally on the test PCs
- later: Max Planck Computing and Data Facility (MPCDF)
  https://confluence.desy.de/display/BI/Backup+of+Characterization+data
- pcbelle21: epics archiver appliance

Test machines as well as measurement data can easily be accessed by collaboration members.

Module Testing

Phase 3 production batches:

L1	P3-1:	8	
	P3-2:	8	
	P3-3:	8	24
L2	P3-4:	18	
	P3-5:	18	36
		total	60

28 modules were already tested.
8 were identified as problematic.

6 of L2 were sorted out after probe card testing.
26 remain to be tested.

W02_IFx	W01_IB	W08_OF2	W03_OB1
W03_IFx	W02_IB	W09_OF1	W05_OB1
W05_IFx	W03_IB	W09_OF2	W06_OB1
W08_IFx	W09_IBx	W11_OF1	W08_OB1x
W32_IF	W32_IB	W11_OF2	W08_OB2
W41_IF	W41_IB	W12_OF1	W09_OB1
W42_IF	W42_IB	W32_OF1	W09_OB2x
W43_IFx	W43_IB	W32_OF2	W12_OB1
W44_IF	W44_IB	W33_OF1	W12_OB2
W45_IF	W45_IB	W33_OF2	W32_OB2
W46_IF	W46_IB	W41_OF1	W33_OB1
W47_IF	W47_IB	W43_OF1	W42_OB1
		W44_OF1	W42_OB2
		W44_OF2	W44_OB1
		W45_OF1	W44_OB2
		W45_OF2	W45_OB2
		W46_OF1	W46_OB1
		W46_OF2	W46_OB2

MPP	HLL	Göttingen	Bonn	Failed on probe card	BEAST

Module Testing

time estimation

very rough calculation:
28 modules tested in 16 weeks $\approx$ 1.75 modules per week
(including Christmas holidays and 5 weeks shutdown at MPP after switcher incident)

estimated testing capability in optimistic case:

- MPP: 2 modules per week
- Göttingen: 2 modules per week $\rightarrow$ **5 modules per week**
- Bonn: 1 module per week

The remaining 26 modules could be tested in about 5 weeks until beginning of March.
Considering the contingency modules and inefficiencies, e.g. due to transport:
A more realistic date for finishing the mass testing is **end of March**.

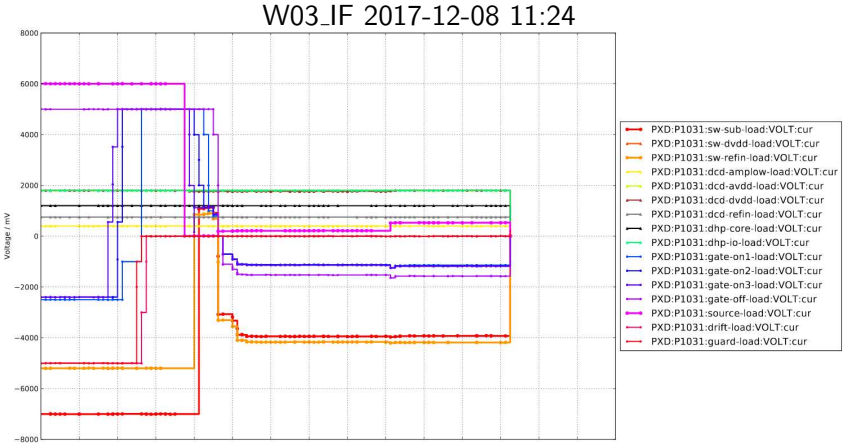
Ladder Testing

Ladders glued so far from the Phase3 modules:

- L1_014 (W45_IF & W01_IB) ✓(many unconnected pixels in IB matrix)
- L1_015 (W47_IF & W02_IB) ✓
- L1_016 (W44_IF & W47_IB) ✓
- L1_017 (W32_IF & W44_IB) ✓
- L1_018 (W41_IF & W41_IB) ✓
- L1_019 (W03_IF & W43_IB) switchers of W03_IF damaged during power down
- L1_020 (W42_IF & W45_IB) not yet tested due to switcher incident
- L1_021 (W46_IF & W32_IB) not yet tested due to switcher incident

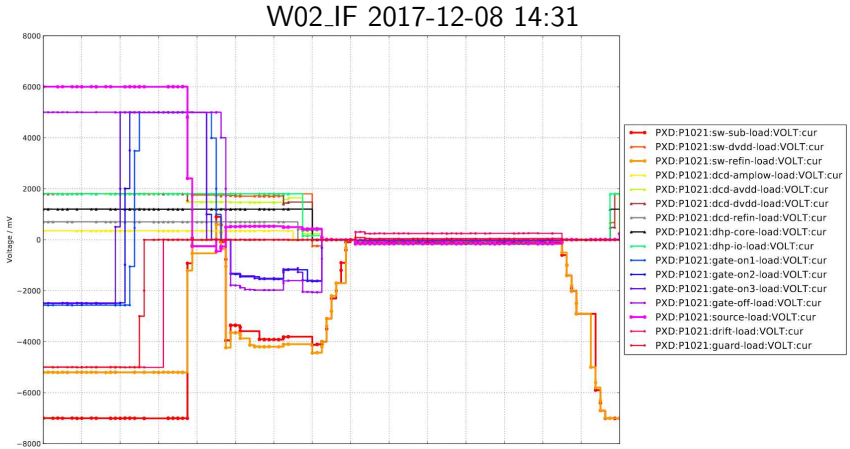
Ladders are tested after gluing to verify nothing broke.
L1_019 was working fine, but encountered a problem during power down.

Powerdown issue or switcher incident



At the step when ramping down the source voltage several lines went into the current limit and the corresponding voltages were pulled away from the nominal values.
sw-sub and sw-refin have been positive for a short time (5-6 s).

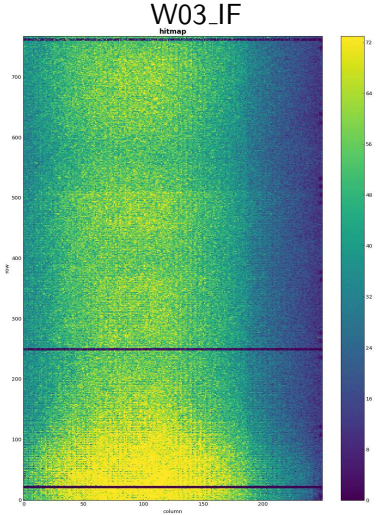
Powerdown issue or switcher incident



Only a few hours later the same behavior was seen on the module W02_IF on pxdtest8. Both modules show increased clear-on and clear-off currents after this incident.

more plots on confluence (Power Down Sequence Documentation)

Powerdown issue or switcher incident



- Source scan reveals 3 damaged gates.
- Clear currents stay at high level:

19355 mV	19003 mV	89 mA	clear-on
4690 mV	4997 mV	-67 mA	clear-off

- L1_019 is running stable for several days now. So far no degradation has been observed. Every 5 minutes pedestals are taken. Those will be analyzed if there was a change in time.

The Power Sequence was adapted by Felix to slow down the ramping of the source voltage. Also all current limits are set now at the first step to provide proper operation of the regulators.

The failure mechanism is still not known.

Failures of tested modules

W02_IF:	switcher incident (08.12.17)
W03_IF:	switcher incident (08.12.17)
W05_IF:	9 ADC channels are bad
W08_IF:	very noisy gates
W43_IF:	DCD corner broken
W09_IB:	switchers in current limit
W08_OB1:	DCD2 many broken drains
W09_OB2:	broken JTAG in the switchers