

# BELLE II PXD WORKSHOP

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## PXD9 PROBE CARD MASS TESTING

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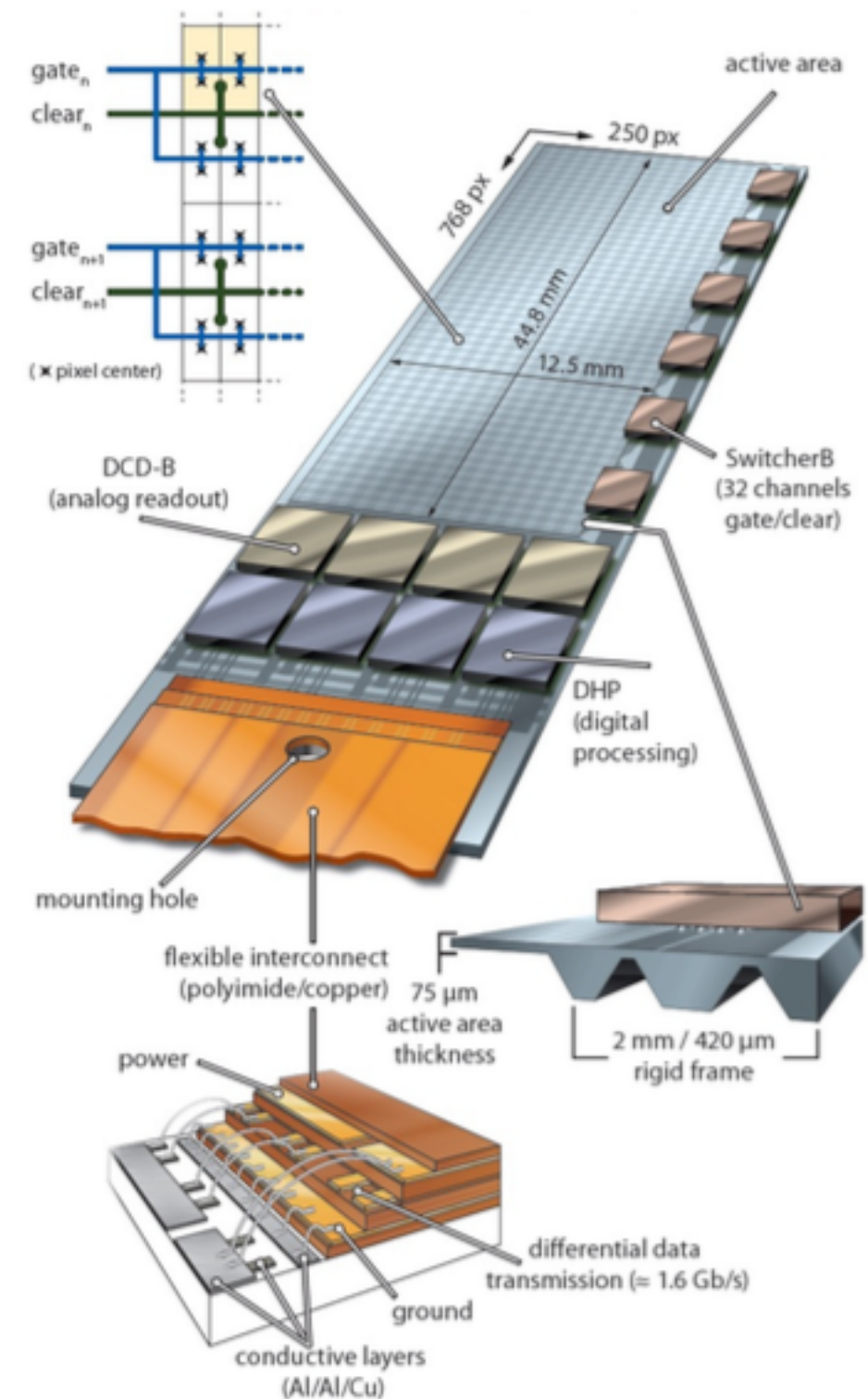
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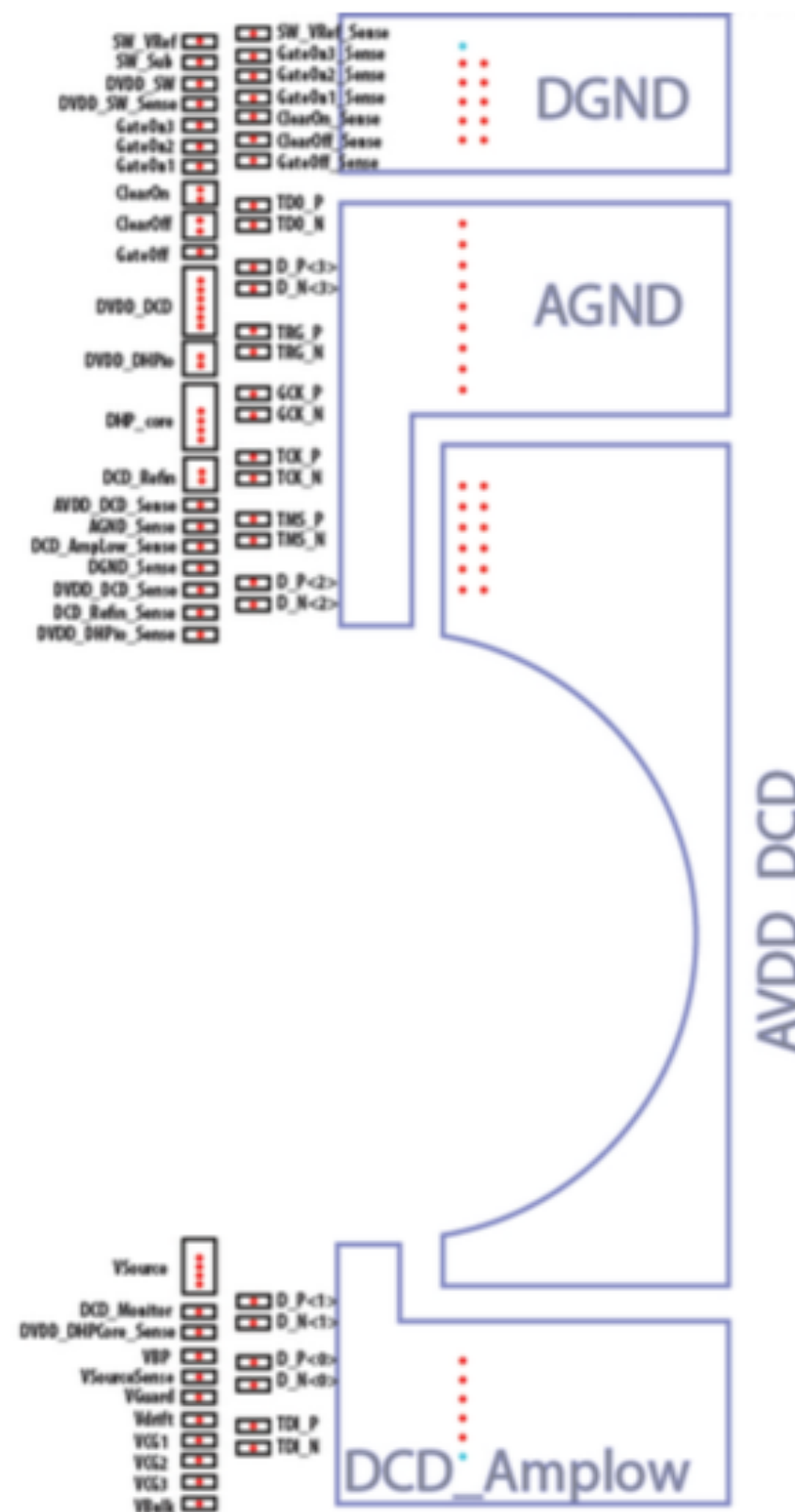
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- 1. Motivation**
- 2. Probe card: design and features**
- 3. Setup at HLL**
- 4. Testing protocol**
- 5. Output of the tests**
- 6. Results**
- 7. Overview**
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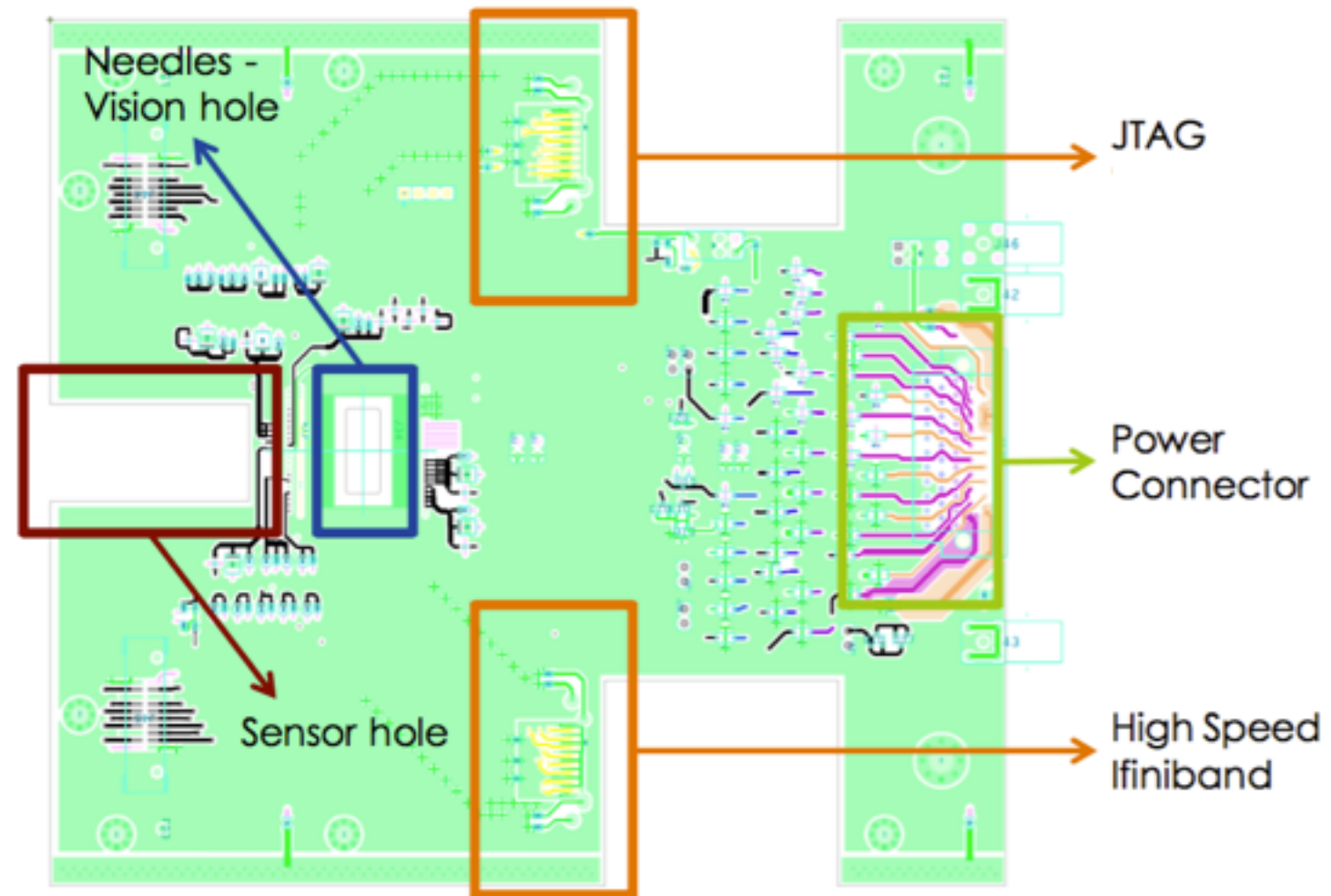
- ▶ DEPFET modules fully assembled are attached to a kapton cable.
- ▶ Pre-testing of the modules before the attachment avoids having to remove the kapton in the case that the module doesn't behave as expected, simplifying the rework procedure.
- ▶ A needle card is required for this purpose.



- ▶ The probe card directly interfaces the PXD9 modules to:
  - ▶ RJ45 cable for the slow control signals.
  - ▶ Glenair cable for power delivery.
  - ▶ Infiniband cable for HSL data transmission.
- ▶ In ideal contact, the module can be fully operated (at the lowest frequency and half rate) through the probe card.



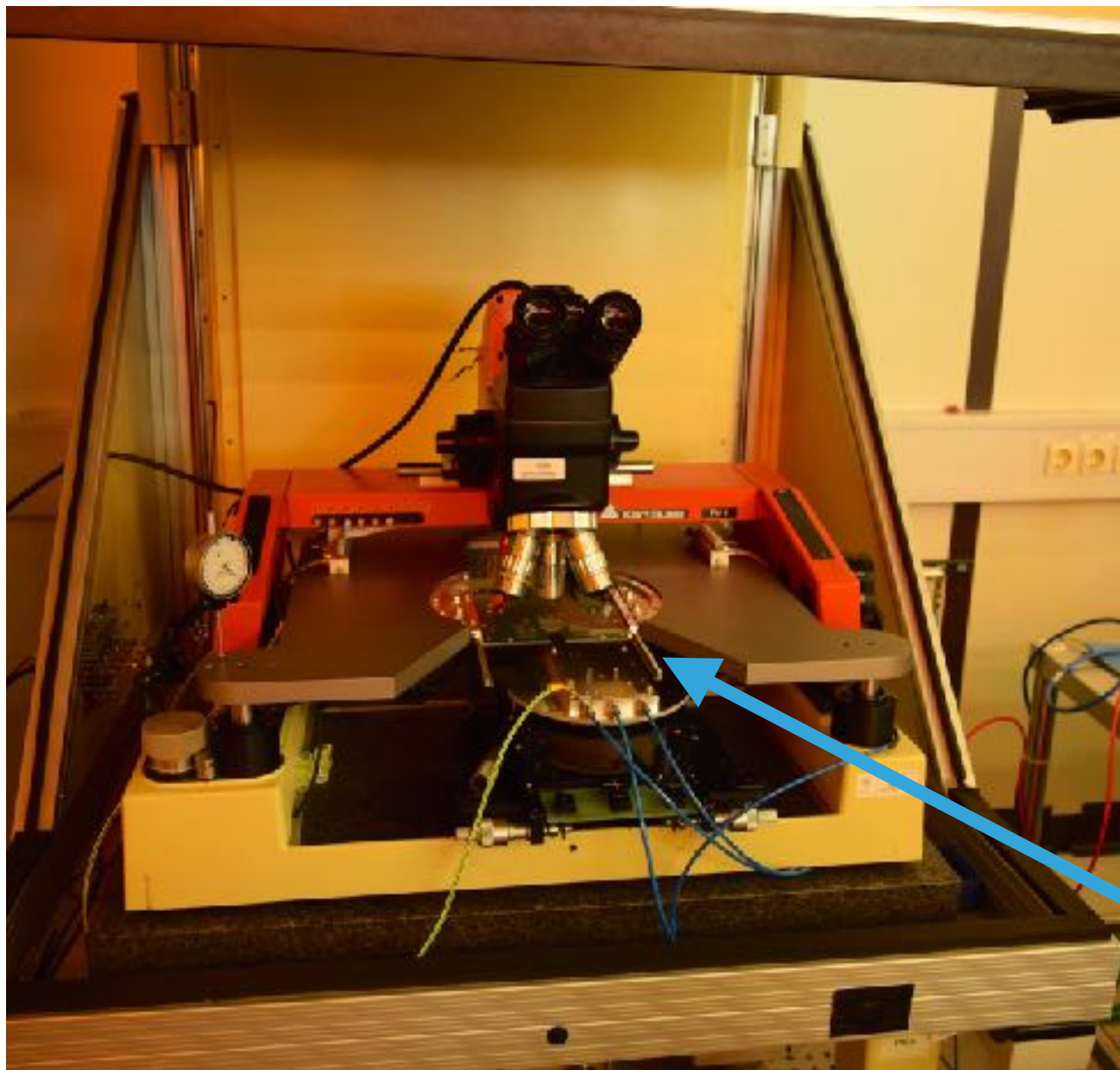
- ▶ 2 different probe card designs for the 2 different layouts of PXD9: design A for IF/OB and B for IB/OF
- ▶ Pad distribution for PXD9:
  - ▶ 59 small aluminium pads, 4 big copper pads.
  - ▶ 8 pads for high speed differential lines.
- ▶ Design considerations:
  - ▶ 114 needles (multiple needles for the big pads) are required.
  - ▶ PCB size is limited by connectors for power supply and infiniband.
  - ▶ Design priority: rather simple and passive PCB, minimizing the path length of the high speed signals.
- ▶ Many thanks to Daniel Esperante for the desing of the probe card.





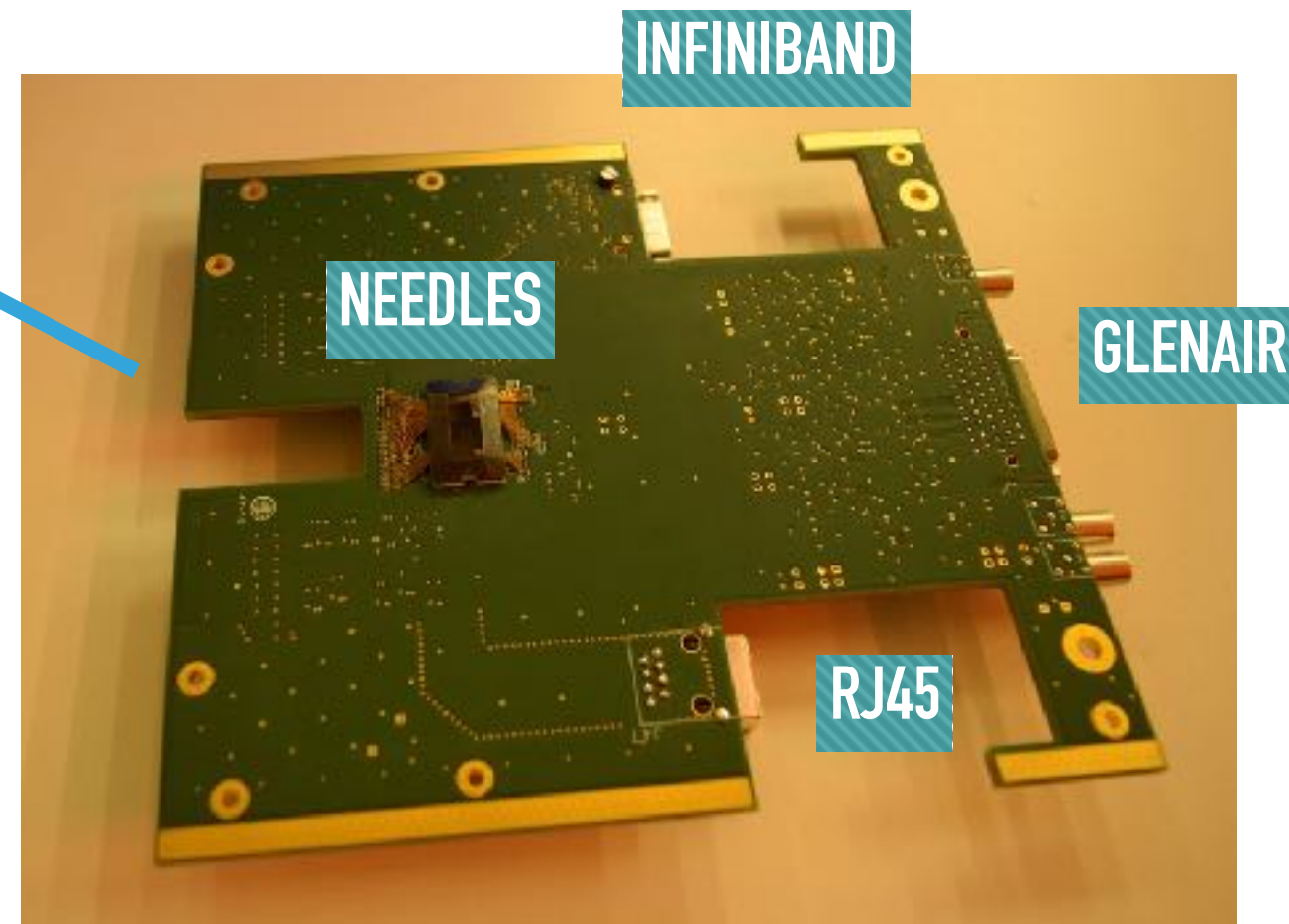
# PROBE CARD: ACTUAL HARDWARE

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- ▶ Modules are placed with their base jig on the cooling jig and secured with screws and vacuum under the probe card.
- ▶ Through the optical microscope we can align the needles with the module and calibrate at what point the touchdown is performed.

- ▶ With the help of the micrometer on the left, we apply the desired overtravel (~60 microns).

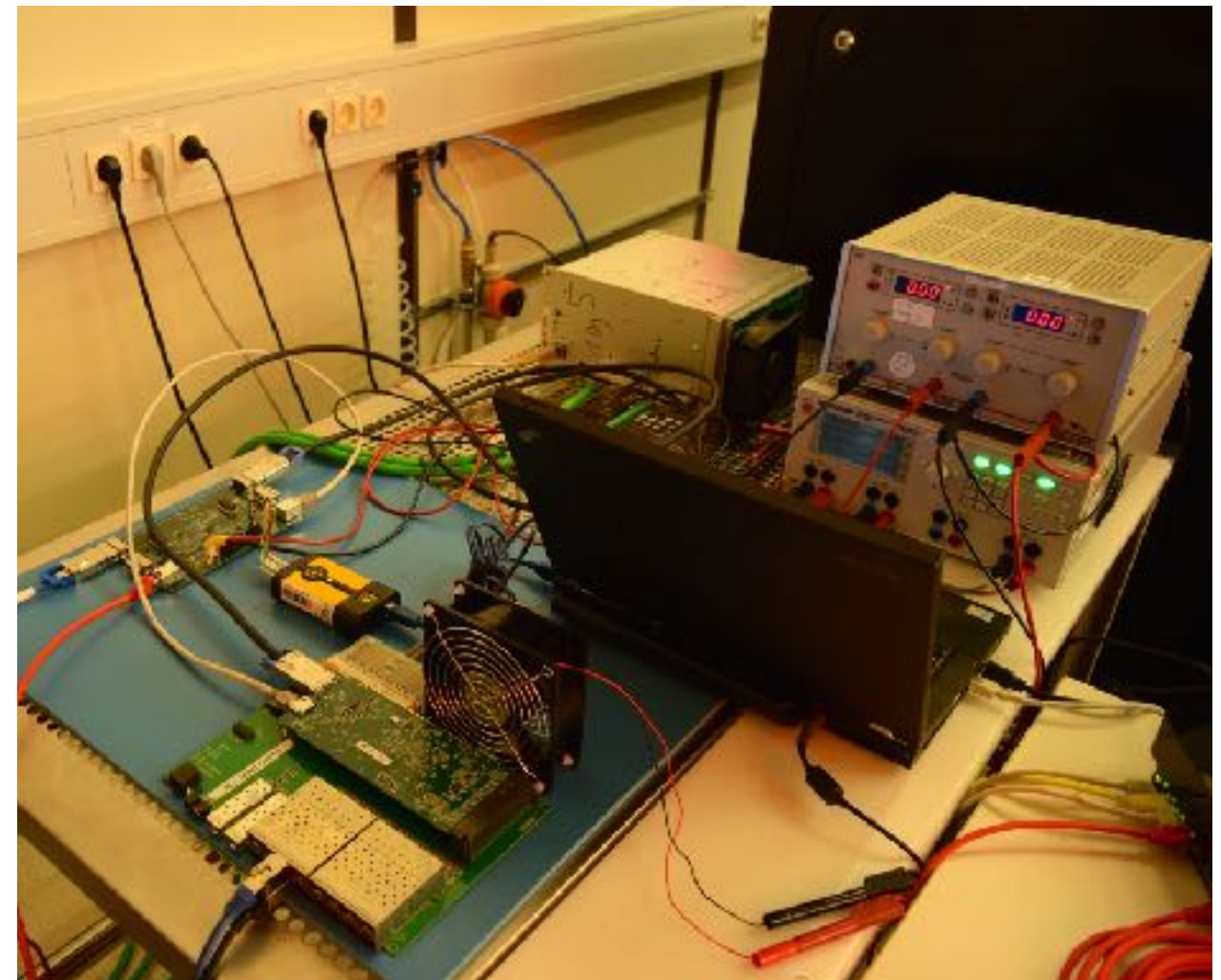
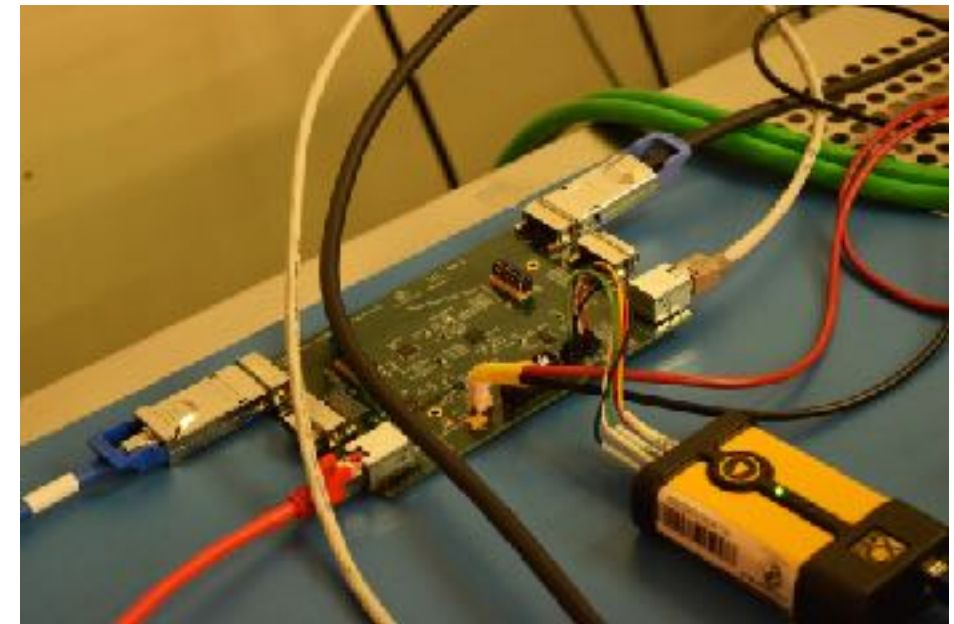




# PXDTEST6 SETUP @HLL

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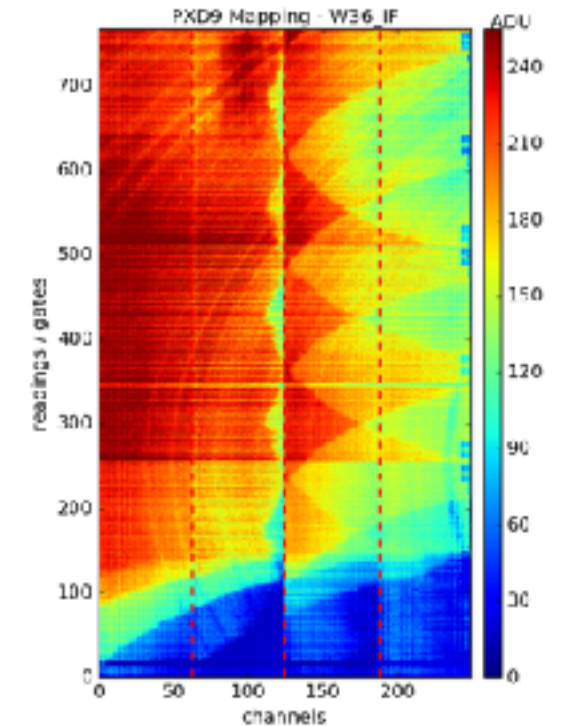
- ▶ 2 probe card A (IF/OB compatible)
- ▶ 2 probe card B (IB/OF compatible)
- ▶ 1 Power breakout board (LMU\_BB-04)
- ▶ 1 LMU power supply (LMUPS-05)
- ▶ 1 DHH carrier card (DHHCCv0.03)
- ▶ 1 DHE (DHE S/N: 0081)
- ▶ 1 JTAG breakout board
- ▶ 1 XJLink2 controller
- ▶ 1 DAQ PC
- ▶ 1 Archiver PC (only PS archived)
- ▶ Cables and services



1. Visual inspection.
2. Check of voltages & currents for DHP, SW and DCD-digital.
3. Chip configuration: JTAG write & read. Retrieving the IDCODEs, uploading and reading SW sequence, ...
4. Boundary scan.
5. Getting the HSL connections.
6. Retrieve the testpattern from the DCDB.
7. Enable DCD-analog and check voltage & currents.
8. Enable and check of DEPFET voltages & currents.
9. Read DEPFET pedestals.
10. Illuminate the matrix with a laser source.

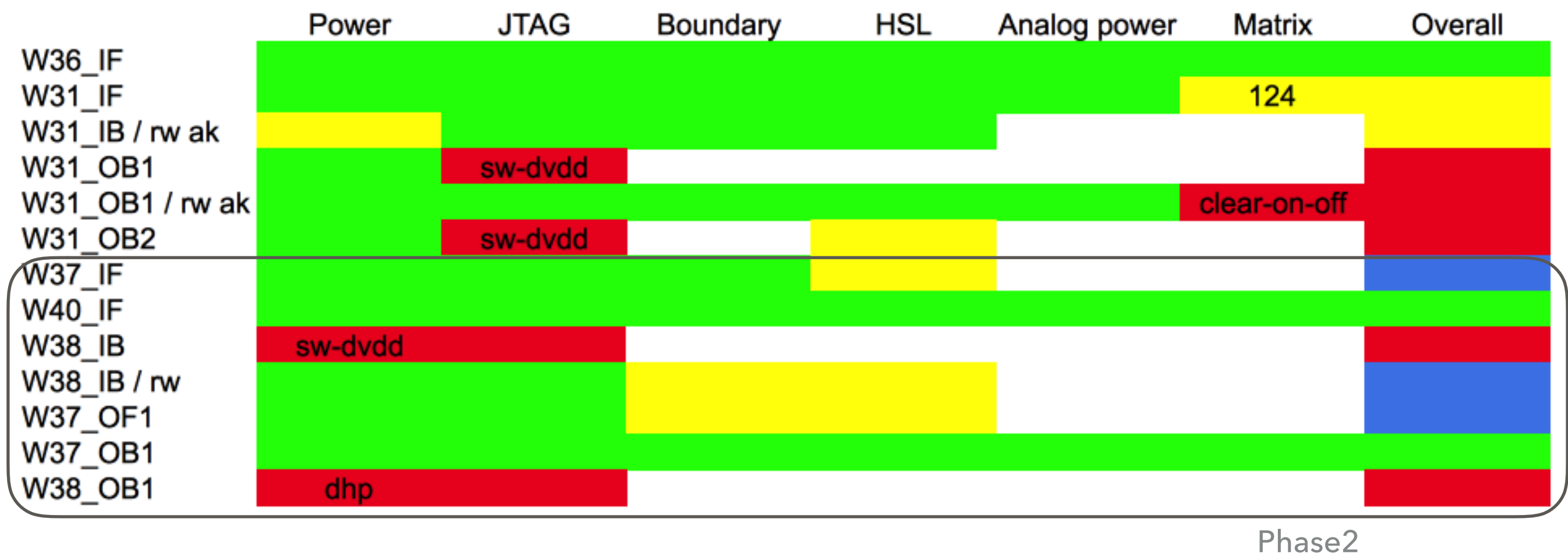


- ▶ One complete report of each of modules with all the details available at <http://elog.mpp.mpg.de/DEPFET/>
- ▶ A copy of the entry is available also at <https://elog.belle2.org/elog/PXD-Mass-Testing/>
- ▶ A check list section into each one of the modules listed at the HephyDB: <http://hephy.at/hephydb/hephydb/>



|                     |                                    |  |   |                     |  |
|---------------------|------------------------------------|--|---|---------------------|--|
| 2017-05-10 14:23:10 |                                    |  |   |                     |  |
| 3                   | Probecard digital tests            | Basic health checks with a probecard. Used to decide if the module continues to kapton attachment.   | ✓ | 2017-05-10 14:23:47 | gomis action repeated 1 times. Second try after the reflow at I2M.   |
| 3.1                 | Check voltages and currents        | Tests if the connections between ASICs and power supply work.  | ✓ | 2017-05-10 14:22:52 | gomis  |
| 3.2                 | JTAG write and read                | Configure the chips, use automatic configuration script. Change, write and read some parameters. Tests the proper slow control connection and ASIC response. | ✓ | 2017-05-10 14:23:01 | gomis  |
| 3.3                 | Boundary scan                      | Tests proper boundary scan structure, chip ID & communication with JTAG controller, check of the digital connections between boundary cells.                 | ✓ | 2017-05-10 14:23:11 | gomis  |
| 3.4                 | High speed link stability          | DHE software to establish the links, IIBERT & Random pattern to debug Tests quality of the data transfer connection  | ✓ | 2017-05-10 14:23:47 | gomis Links were extremely stable with eye diagrams of ~30 for all DHPTs.  |
| 4                   | Probecard analog tests             | Basic health checks with a probecard. Used to decide if the module continues to kapton attachment.   | ✓ | 2017-05-10 14:40:28 | gomis action repeated 1 times. Repeating to change the fail in the voltages and currents to "skip". Fail doesn't let you continue with the steps.  |
| 4.1                 | Check voltages and currents        | Tests if the connections between sensor and power supply work.   | ✓ | 2017-05-10 14:38:52 | gomis  |
| 4.2                 | Read DCD pedestals                 |  | ✓ | 2017-05-10 14:39:02 | gomis  |
| 4.3                 | Check matrix voltages and currents |  | ⚠ | 2017-05-10 14:39:21 | gomis There seem to be some shorts in between DEPFET voltages: as soon as you power up clear on (12 V), gate off and clear off gain (2.5V) even though they should remain powered off. Also, as soon as you power up clear off (5V), gate on ramps up to 4.8 V (2.3 V on top of the previous 2.5V from the clear on), and gate-on2, gate-on3 also ramp up to 2.2 V. Even with this shorts, we could power all the DEPFET matrix and take some pedestals. |
| 4.4                 | read matrix pedestals              |  | ⚠ | 2017-05-10 14:40:28 | gomis The matrix was illuminated with a flashlight and the pedestal showed response from all the matrix except the SW3 area.   |

# RESULTS: PREPROD. AND PHASE2 MODULES



## TEST RESULTS COLOR CODE:

**PERFECT** | **PASSED** | **MINOR ERRORS / POSSIBLE TOUCHDOWN PROBLEMS** | **SHOW STOPPER**

## YIELD (AFTER REWORKS):

IF: 4/4 | IB: 2/2 | OF: 1/1 | OB: 1/4 | TOTAL: 8/11 (72%)

# RESULTS: PHASE3 IF MODULES

|        | Power | JTAG | Boundary | HSL | Analog power | Matrix | Overall |
|--------|-------|------|----------|-----|--------------|--------|---------|
| W02_IF |       |      |          |     |              |        |         |
| W03_IF |       |      |          |     |              |        |         |
| W05_IF |       |      |          |     |              |        |         |
| W08_IF |       |      |          |     |              |        |         |
| W32_IF |       |      |          |     |              |        |         |
| W41_IF |       |      |          |     |              |        |         |
| W42_IF |       |      |          |     |              |        |         |
| W43_IF |       |      |          |     |              |        |         |
| W44_IF |       |      |          |     |              |        |         |
| W45_IF |       |      |          |     |              |        |         |
| W46_IF |       |      |          |     |              |        |         |
| W47_IF |       |      |          | 34  |              | 34     |         |

TEST RESULTS COLOR CODE:  
PERFECT | PASSED | MINOR ERRORS / POSSIBLE TOUCHDOWN PROBLEMS | SHOW STOPPER

YIELD:  
IF: 12/12 (100%)



# RESULTS: PHASE3 IB MODULES

|        | Power   | JTAG   | Boundary | HSL | Analog power | Matrix | Overall |  |
|--------|---------|--------|----------|-----|--------------|--------|---------|--|
| W01_IB | Perfect | Passed | Boundary | 123 |              |        | Passed  |  |
| W02_IB |         |        |          |     |              |        |         |  |
| W03_IB |         |        |          | 12  |              |        |         |  |
| W09_IB |         |        |          | 234 |              |        |         |  |
| W32_IB |         |        |          |     |              |        |         |  |
| W41_IB |         |        |          |     |              | 24     |         |  |
| W42_IB |         |        |          | 123 |              | 123    |         |  |
| W43_IB |         |        |          | 1   |              |        |         |  |
| W44_IB |         |        |          |     |              |        |         |  |
| W45_IB |         |        |          |     |              |        |         |  |
| W46_IB |         |        |          |     |              |        |         |  |
| W47_IB |         |        |          | 123 |              |        |         |  |

TEST RESULTS COLOR CODE:  
PERFECT | PASSED | MINOR ERRORS / POSSIBLE TOUCHDOWN PROBLEMS | SHOW STOPPER

YIELD:  
IB: 12/12 (100%)

# RESULTS: PHASE3 OF MODULES

|         | Power   | JTAG | Boundary | HSL | Analog power | Matrix | Overall |
|---------|---------|------|----------|-----|--------------|--------|---------|
| W08_OF2 |         |      |          | 13  |              | 13     |         |
| W09_OF1 |         |      |          | 13  |              | 13     |         |
| W09_OF2 |         |      |          |     |              |        |         |
| W11_OF1 |         |      |          |     |              |        |         |
| W11_OF2 |         |      |          | 13  | dcd-avdd     |        |         |
| W12_OF1 |         |      |          | 12  |              | 12     |         |
| W32_OF1 |         |      |          | 123 |              | 12     |         |
| W32_OF2 |         |      |          | 12  |              |        |         |
| W33_OF1 |         |      |          |     |              | 124    |         |
| W33_OF2 |         |      |          |     |              | 123    |         |
| W41_OF1 |         |      |          | 123 |              | 123    |         |
| W43_OF1 | sw-dvdd |      |          |     |              |        |         |
| W44_OF1 | sw-dvdd |      |          |     |              |        |         |
| W44_OF2 | sw-dvdd |      |          |     |              |        |         |
| W45_OF1 |         |      |          |     |              | 124    |         |
| W45_OF2 | dhp     |      |          |     |              |        |         |
| W46_OF1 |         |      |          | 12  |              |        |         |
| W46_OF2 |         |      |          | 12  |              |        |         |

TEST RESULTS COLOR CODE:  
PERFECT | PASSED | MINOR ERRORS / POSSIBLE TOUCHDOWN PROBLEMS | SHOW STOPPER

YIELD:  
OF: 11/16 (69%)

# RESULTS: PHASE3 OB MODULES

|         | Power   | JTAG | Boundary | HSL | Analog power | Matrix | Overall |
|---------|---------|------|----------|-----|--------------|--------|---------|
| W03_OB1 |         |      |          |     |              |        |         |
| W05_OB1 |         |      |          |     |              |        |         |
| W06_OB1 |         |      |          |     |              |        |         |
| W08_OB1 |         |      |          |     |              |        |         |
| W08_OB2 |         |      |          |     |              |        |         |
| W09_OB1 | sw-dvdd |      |          |     |              |        |         |
| W09_OB2 |         |      |          |     |              |        |         |
| W12_OB1 |         |      |          |     |              |        |         |
| W12_OB2 |         |      |          |     |              |        |         |
| W32_OB2 |         |      |          |     |              |        |         |
| W33_OB1 |         |      |          |     |              |        |         |
| W42_OB1 |         |      |          |     |              |        |         |
| W42_OB2 |         |      |          |     |              |        |         |
| W44_OB1 |         |      |          |     |              |        |         |
| W44_OB2 |         |      |          |     |              |        |         |
| W45_OB2 |         |      |          |     |              |        |         |
| W46_OB1 |         |      |          |     |              |        |         |
| W46_OB2 |         |      |          |     |              |        |         |

TEST RESULTS COLOR CODE:  
PERFECT | PASSED | MINOR ERRORS / POSSIBLE TOUCHDOWN PROBLEMS | SHOW STOPPER

YIELD:  
OB: 15/16 (94%)



- ▶ The yield (modules without show stoppers, and including reworks) of all the probe card tests performed to the date is accounted in the following table:

|          | IF              | IB              | OF             | OB             |
|----------|-----------------|-----------------|----------------|----------------|
| Preprod. | 2/2             | 1/1             | 0              | 0/2            |
| Phase2   | 2/2             | 1/1             | 1/1            | 1/2            |
| Phase3   | 12/12           | 12/12           | 11/16          | 15/16          |
| Total    | 16/16<br>(100%) | 14/14<br>(100%) | 12/17<br>(71%) | 16/20<br>(80%) |

- ▶ A total of 67 modules were tested, with 9 of them showing errors which were catalogued as show stoppers. Out of this 9 errors: 6 are switcher related, 2 dhp related, 1 dcd related and 1 DEPFET matrix related.
- ▶ Modules like W38\_IB (the one with the rotated switcher) could be debugged with the probe card and repaired before kapton attachment.

- ▶ In some of the modules the needles are able to make a really good contact, and a really stable connection is achieved (W31\_OB1 ran without losing any HSL for almost an hour). Whereas in others getting the HSL was really difficult (ie. W37\_IF).
- ▶ In most of the cases, testing an IF/OB module with the probe card A was straightforward, meanwhile IB/OF modules used to take more of an effort.
- ▶ For an optimal contact, planarity between the probe card and the module is crucial. In this sense, the jig used to house the module can really affect the measurement.
  - ▶ Instead of using a unique jig for each of the modules (as it was intended), we found jigs that worked fairly for each type of modules and kept using those for all the measurements.

- ▶ To improve the contact between the needles and the pads, we perform consecutive touchdowns in the same spot in order to scratch a bit the surface on the pad and allow for better contact.
- ▶ Regularly cleaning and polishing the needles of the probe card also helped with their performance.
- ▶ Occasionally, when the performance was really deteriorated and cleaning didn't help, they were shipped to the manufacturer (PTSL) for a refurbishment.



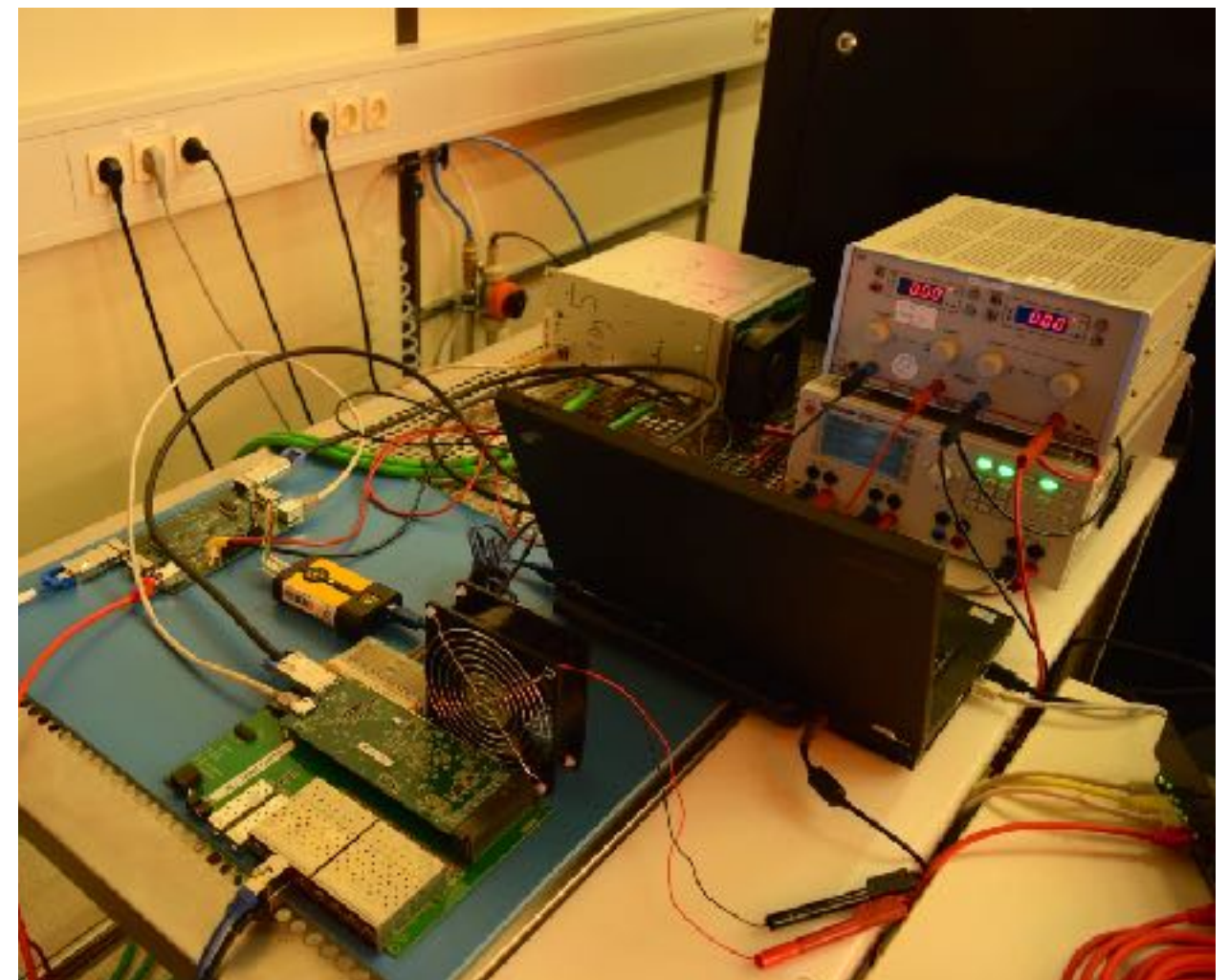
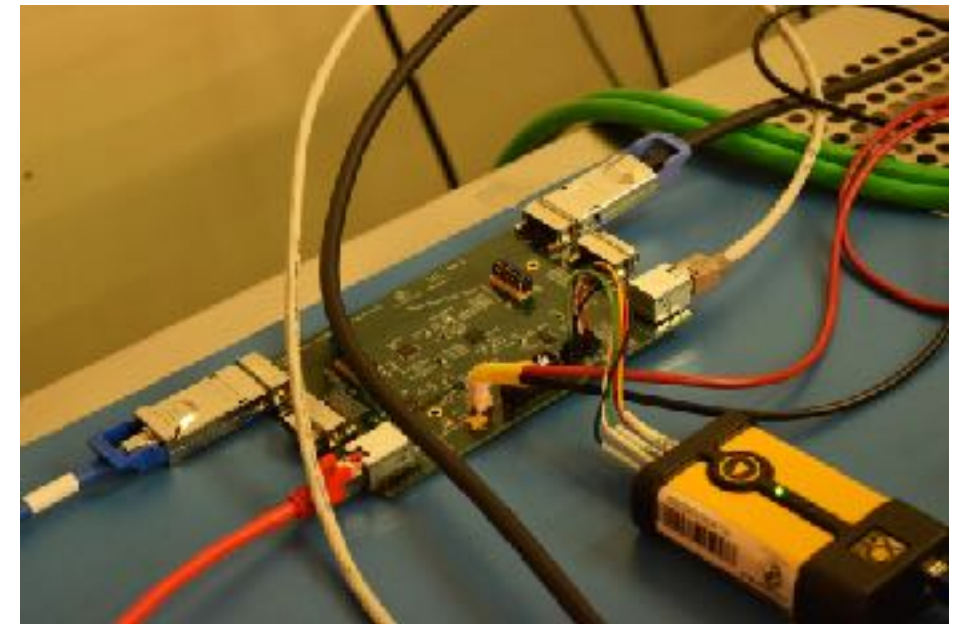
- ▶ Two probe card designs to test the PXD9 modules have been produced and are in operation.
- ▶ A testing protocol for the mass production was developed and tested with real modules.
- ▶ Ideally we can fully operate all the modules before kapton attachment.
  - ▶ Unfortunately, not all the touchdowns are optimal, and sometimes we can't operate the module fully.
- ▶ In total we were able to test 67 modules, spotting show stopper errors in 9 of them. And allowing for the refurbishment of one of the modules.

**THANKS FOR  
YOUR ATTENTION**

# BACKUP



- ▶ 2 probe card A (IF/OB compatible)
- ▶ 2 probe card B (IB/OF compatible)
- ▶ 1 Power breakout board (LMU\_BB-04)
- ▶ 1 LMU power supply (LMUPS-05)
- ▶ 1 DHH carrier card (DHHCCv0.03)
- ▶ 1 DHE (DHE S/N: 0081)
- ▶ 1 JTAG breakout board
- ▶ 1 XJLink2 controller
- ▶ 2 Bench power supplies



- ▶ 2 Infiniband cables, 2 green power cables, a glenair cable, RJ45 cables and banana cables
- ▶ 2 SFP adaptors
- ▶ 2 Fans to cool the DHE and the LMU PS
- ▶ 1 Cooling block (water cooled) with a vacuum pipe
- ▶ 2 Network switchers
- ▶ pxdtest6 SL7 pc: using the latest software release available at mid november 2016 (for stability/feature reasons), steering the modules with ini files (no DB)
- ▶ pxdtest5 SL7 pc: up-to-date software release, compatible with the DB
- ▶ edet2 SL7 pc: set up as archiver