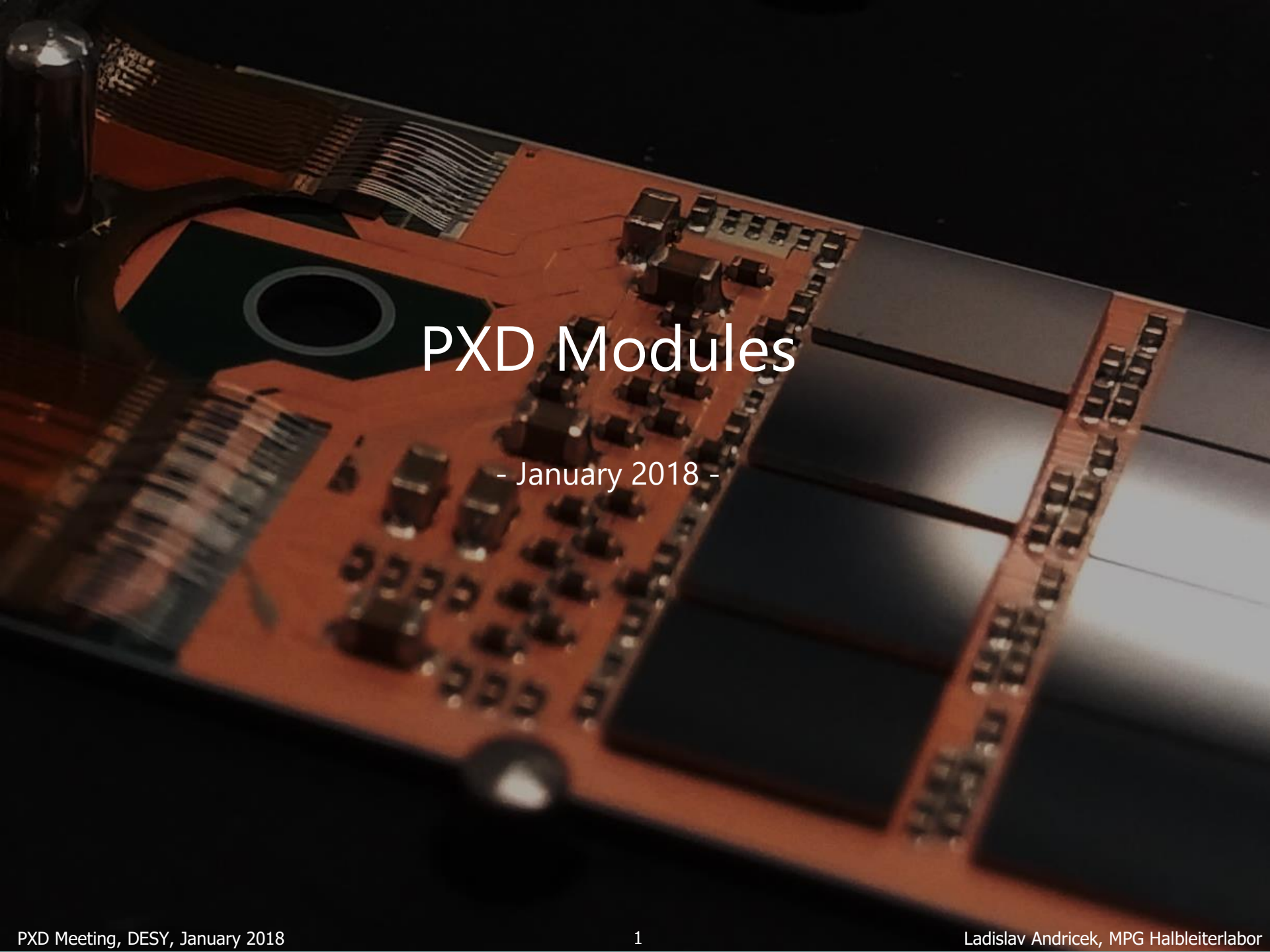


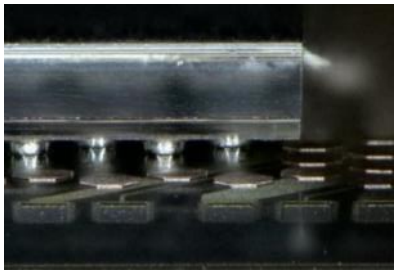
PXD Modules

- January 2018 -

module and ladder assembly – in a nutshell

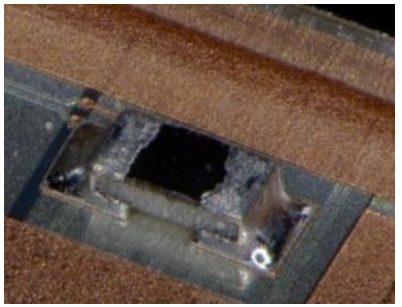
1. Flip Chip of ASICs (~240°C) at IZM, Berlin

- Bumped ASICs have the solder balls (SAC305 and AgSn)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ SWB bumping on chip level at IZM Berlin



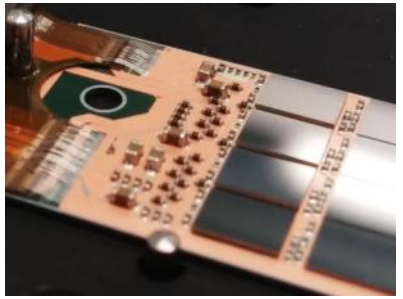
2. SMD placement (~200°C) at HLL, Munich

- Passive components (termination resistors, decoupling caps)
- Dispense solder paste/jetting of solder balls, pick, place and reflow
- **First module tests** on probe station possible at this stage already



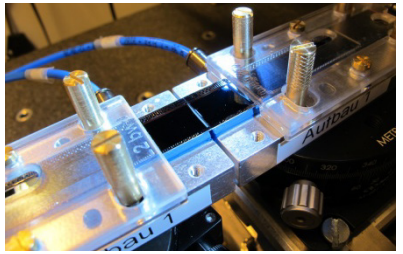
3. Kapton attachment (~170°C), wire bonding at MPP, Munich

- 4-layer flex/rigid technology with SMDs, ~40 cm long, Kaupke/MOS
- Solder paste printing on kapton, soldering
- Wire-bond, wedge-wedge, 32 µm Al bond wires
- **Full module characterization**



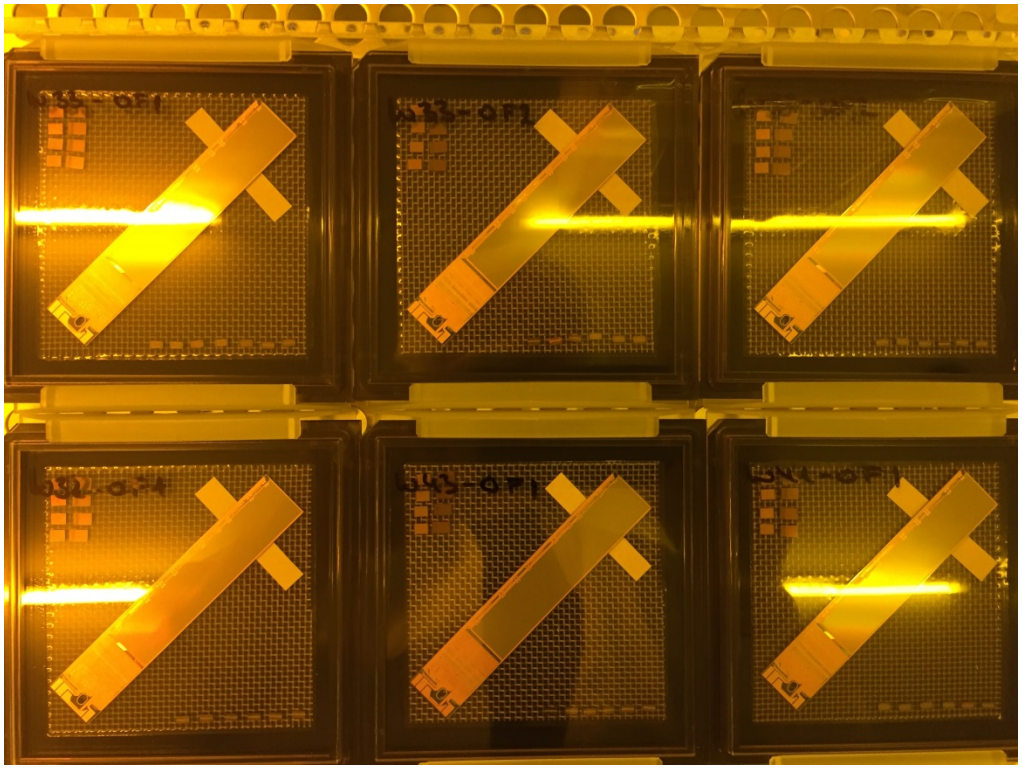
4. ladder gluing (RT) at MPP, Munich

- Dispense adhesive, align two modules, join two modules to ladder
- **ladder tests (verification of the functionality)**



Flip chip I

- pre-tested components assembled gel-paks for transport to IZM
  - ↳ after initial problems with UPS, all production modules by personal transport
- Many initial problems, solved “on the fly” mostly
  - ↳ biggest source of trouble: Switcher bumping, quality of bumps
- for the future: **change to bumping on wafer level**



Flip Chip II – Report from IZM

BELLE II – Sensor Assembly

22. November 2017, München

Prozessablauf

Ausrichtung des Moduls

- Eingangsinspektion (mittels Lichtmikroskop)
- Manuelle Reinigung (falls Partikel vorhanden)
- HCOOH-Reinigung im Ofen
- Platzierung auf dem Sensor (Switcher, DHP, DCD)
- Transfer in den Ofen
- Löten unter reduktiver Atmosphäre
- Ausgangsinspektion (mittel Röntgenmikroskop)

Folie 2

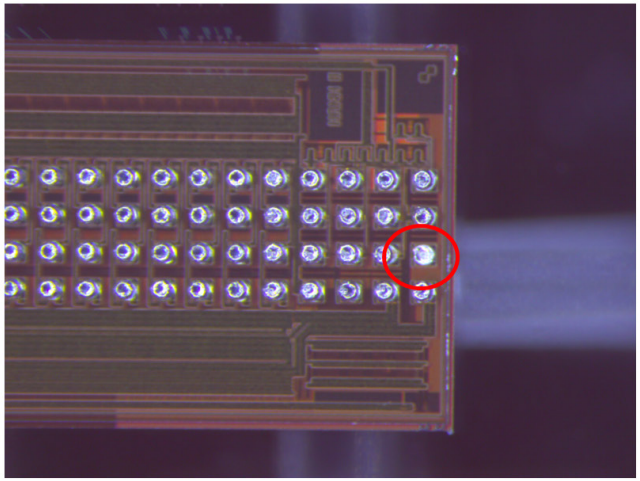
Abt.: Wafer Level System Integration
Gruppe: Interconnect Metallurgy and Processes (IMP)
Mario Rothermund

Fraunhofer IZM

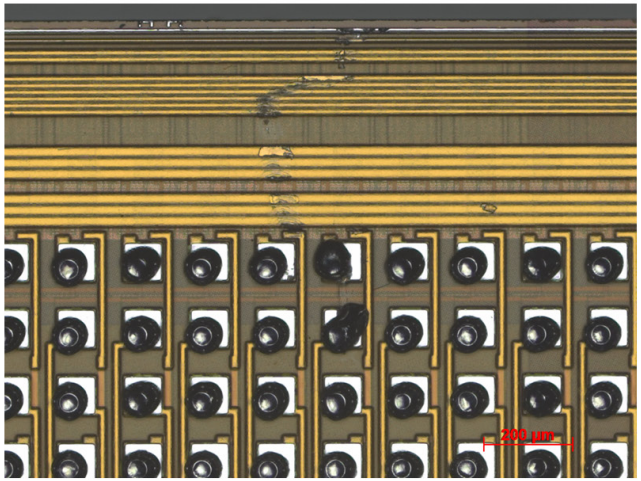
Confidential!

Technische Universität Berlin
Forschungsschwerpunkt
Technologien der Mikroperipherik

Flip Chip II – Report from IZM



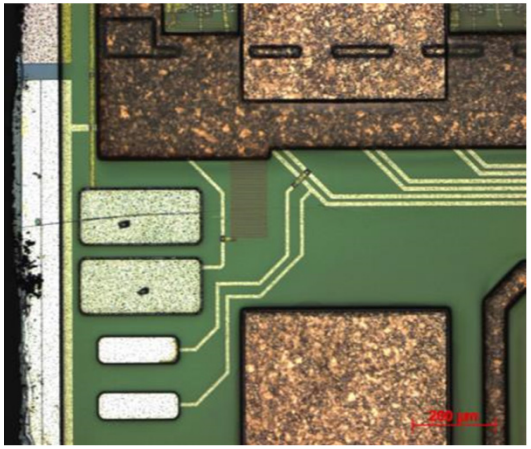
Fehlender Bump auf eienem Switcher



Paddefekt und Kratzer auf einem Switcher

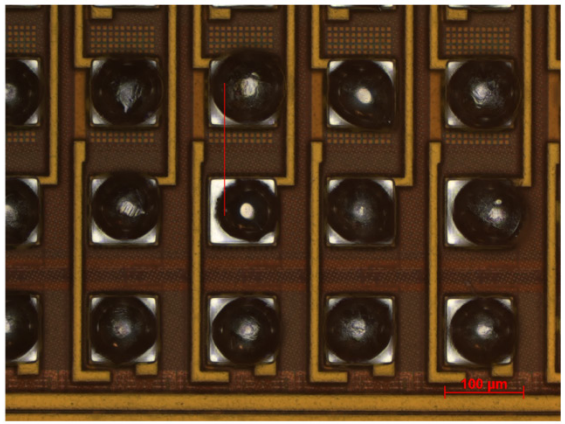
Eingangsinspektion

Modul W31-IB

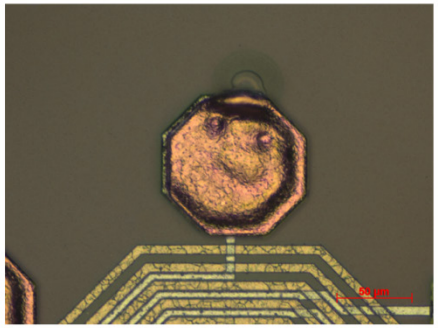


Folie 5

Eingangsinspektion



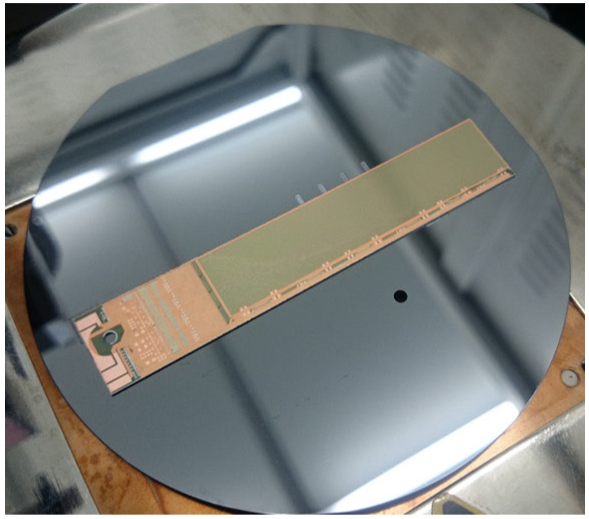
Höhendifferenz zwischen Balls: bis zu 25µm

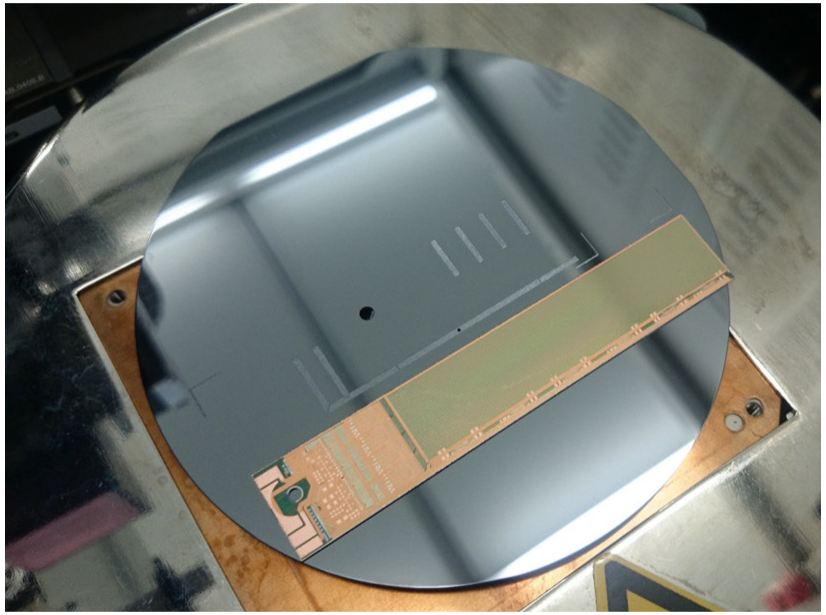


evtl. Lackrest unter dem Pad

22. November 2017, München

Montageadapter





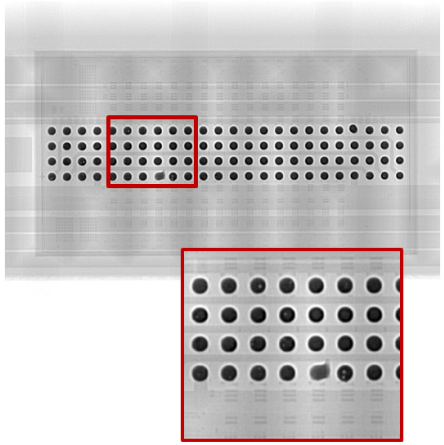
- Träger aus Silizium
- Geätzte Strukturen
- Vakuumgräben
- Belüftungsgräben (für gedünnten Bereich)
- Alignmentmarken (Sensorpositionierung)

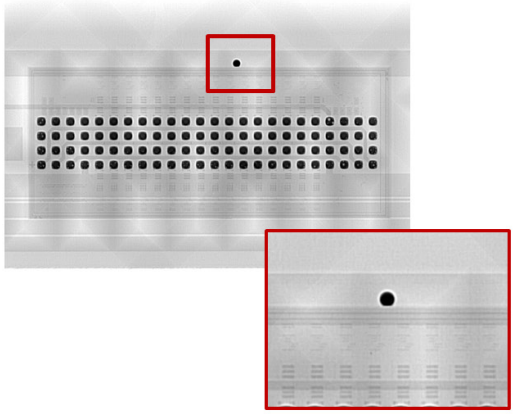
Folie 6

Flip Chip II – Report from IZM

Ausgangsinspektion

22. November 2017, München

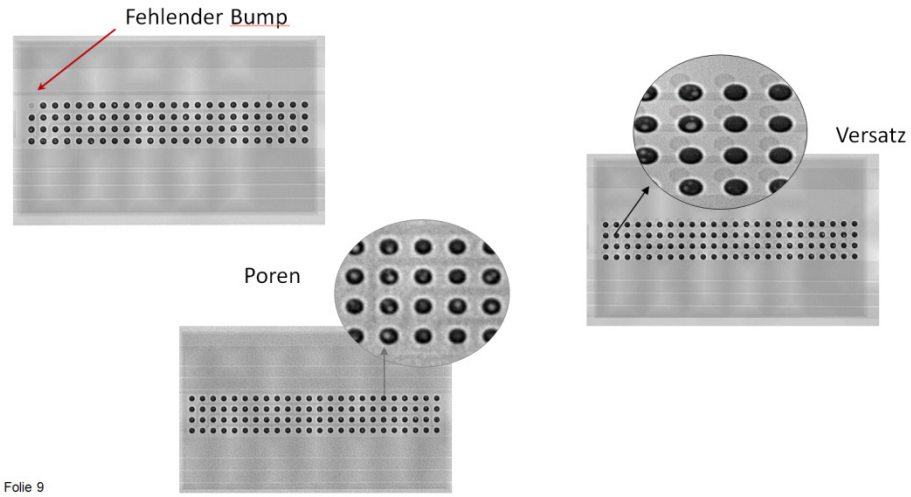




Bump wahrscheinlich
nicht verbunden

22. November 2017, München

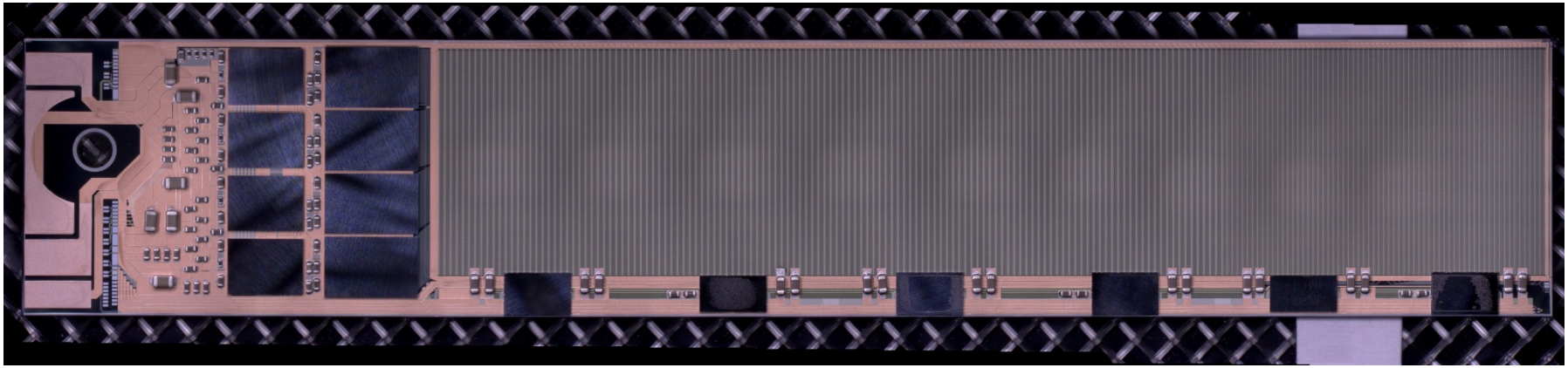
Ausgangsinspektion



Folie 9

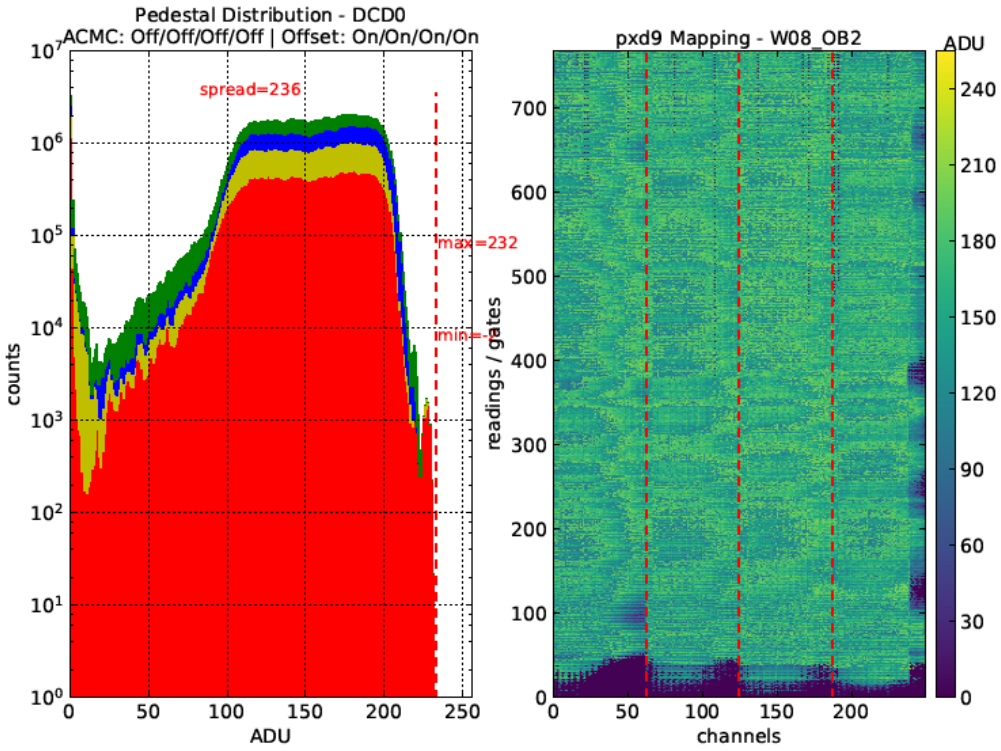
SMD at HLL

- personal transport of modules to HLL
- incoming inspection (optical and x-ray)
- SMD process installed and qualified (dispense, pick-and-place, reflow)
- outgoing inspection (optical)



a lot of x-ray inspection … too much?

- inhomogeneous rad damage due to x-rays
  - ↳ shields/masks used, but the alignment of the mask was not ideal
- deltaVth in damaged area ~150mV, ~few tens of krad (tbc)



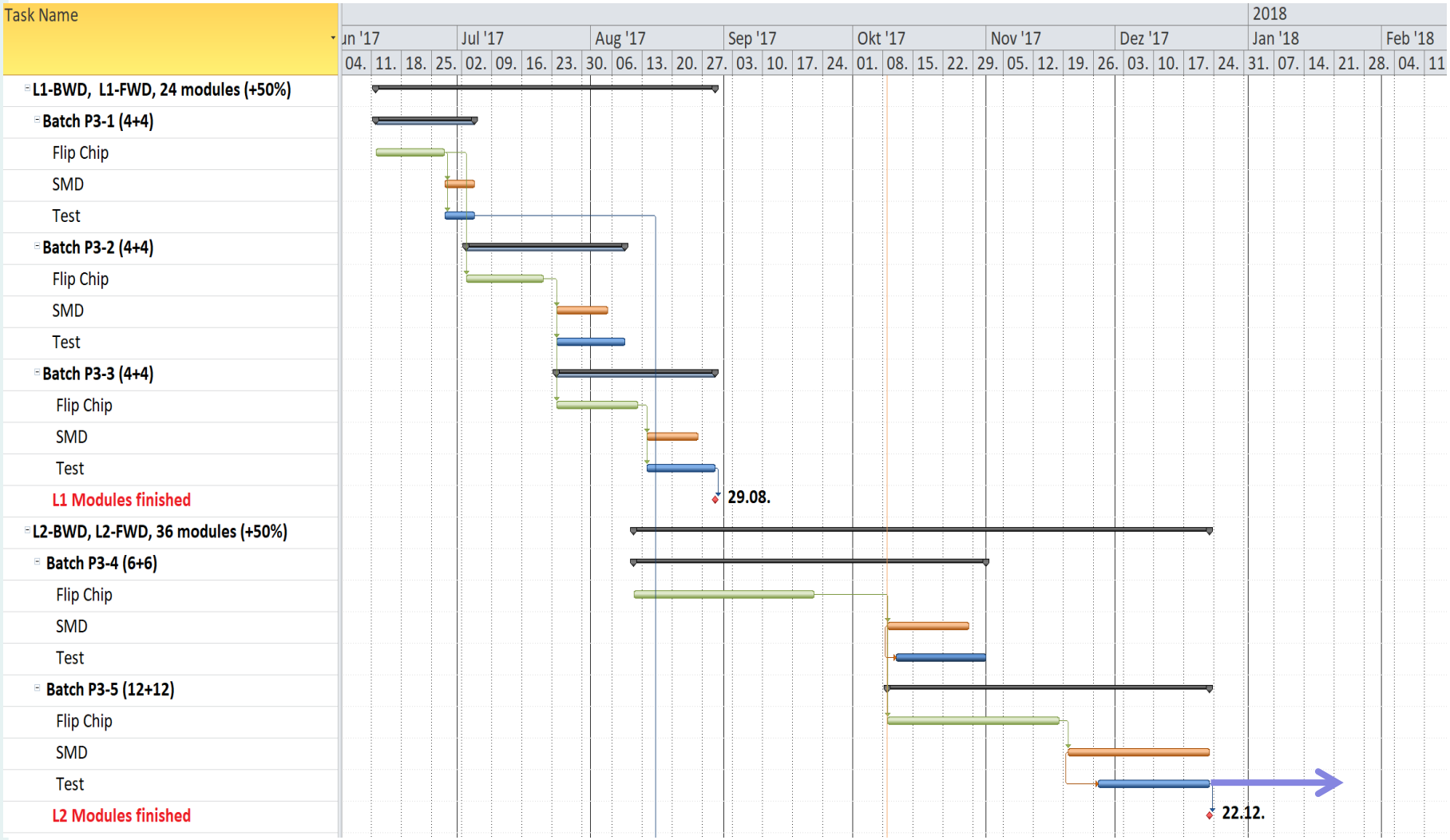
production strategy and status

- Start with smaller batches of L1 modules, then larger batches of L2, **50% contingency**
  - P3-1: Layer 1 - 4+4 modules (lower quality sensors first)
  - P3-2: Layer 1 - 4+4 modules
  - P3-3: Layer 1 – 4+4 modules
  - P3-4: Layer 2 – 6+6 modules
  - P3-5: Layer 2 – 12+12 modules
  - P3-6: Layer 1 – replacement of damaged modules, two IB and three IF, starts this week
  - P3-7: Layer 2 - ???

Module overview

IB	Batch	Quality	comment	IF	Batch	Quality	comment	OB	Batch	Quality	comment	OF	Batch	Quality	comment
W32	P3-3	G100	L1_021	W32	P3-3	G100	L1_017					W32-1	P3-5	G99.5	
								W32-2	P3-5	G100		W32-2	P3-5	G100	
								W33-1	P3-5	G99.5		W33-1	P3-5	G100	
												W33-2	P3-5	G100	
W41	P3-3	G100	L1_018	W41	P3-3	G99.5	L1_018					W41-1	P3-5	G99.5	
W42	P3-3	G100		W42	P3-3	G99.3	L1_020	W42-1	P3-5	G99.5		W42-1		M100	
								W42-2	P3-5	G100		W42-2		M100	
W43	P3-2	G100	L1_019	W43	P3-2	G100	DCD corner chip	W43-2		M99.9		W43-1	P3-5	G100	
W44	P3-2	G100	L1_017	W44	P3-1	G100	L1_016	W44-1	P3-5	G99		W44-1	P3-5	G100	
								W44-2	**P3-5**	**G100**		W44-2	P3-5	G100	
W45	P3-2	G100	L1_020	W45	P3-1	G100	L1_014					W45-1	P3-5	G99.5	
								W45-2	P3-5	G100		W45-2	P3-5	G100	
W46	P3-1	G99.5	BEAST phase2	W46	P3-1	G99.5	L1_021	W46-1	P3-5	G99.5		W46-1	P3-5	G100	
								W46-2	P3-5	G100		W46-2	P3-5	G99.9	
W47	P3-1	G99.5	L1_016	W47	P3-1	G99.5	L1_015					W47-1		G98.1	
W01	P3-1	G94.4	L1_014					W01-1		G100???		W01-1		G99.6???	
W02	P3-1	M99	L1_015	W02	P3-2	G99	--> swb kill					W02-1		G99	
W03	P3-2	G100		W03	P3-2	G99	L1_019 --> swb kill	W03-1	P3-5	G99					
												W03-2		G99.4	
W04	P3-6	M99.5		W04	P3-6	G99		W04-1		M99		W04-1		G99.3	
W05		G98.4		W05	P3-2	G99.3 - 1DS Shorts	9ADC chan. bad, HLL	W05-1	P3-5	G99		W05-1		G99.5	
												W05-2		G99.3	
W06		M99.5		W06		G98.8 - 6DS shorts		W06-1	P3-4	G99	GOE-MUC	W06-1		G98.9	
												W06-2		G97.9	
				W08	P3-3	G99.5	very noisy gates, HLL	W08-1	P3-4	G99	DCD2 many broken drains				
								W08-2	P3-4	G99	GOE-MUC	**W08-2**	**P3-4**	**G99.5**	GOE
W09	P3-3	G100	sw curr limit, HLL	W09	P3-6	G99		W09-1	P3-4	G99		**W09-1**	**P3-4**	**G99**	BN
								W09-2	P3-5	M99.5	broken JTAG	W09-2	P3-4	G99.5	
				W10		G99		W10-1		G98.4		W10-1		G98.4	
												W10-2		G98.4	
W11		M98.7 2DS shorts repaired		W11		G99.3 1DS short repaired						**W11-1**	**P3-4**	**G99**	GOE
												W11-2	**P3-4**	**G99**	GOE
								W12-1	P3-4	G99.5	instable links, do it later	**W12-1**	**P3-4**	**G99**	BN
								W12-2	P3-4	G99		W12-2		M98.9	
W13	P3-6	G99		W13	P3-6	G99.5						W13-1		G97.9	
								W13-2		G98.4					

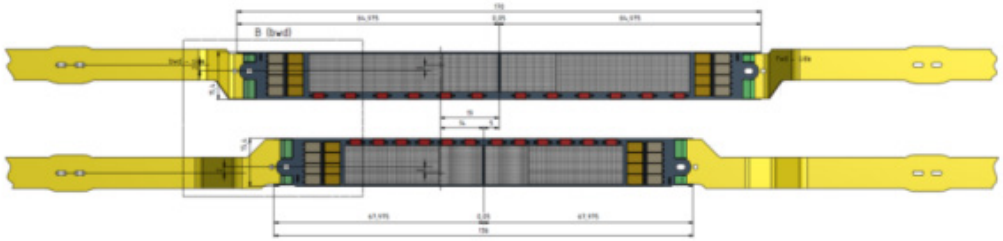
How long it took

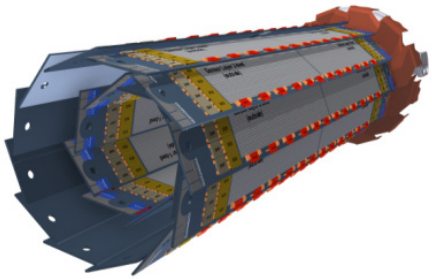


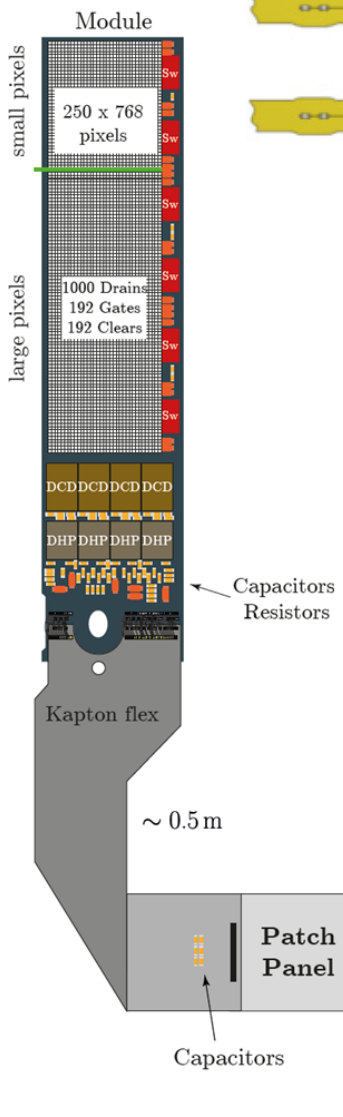
Summary

- Main module production close to be finished
  - kapton attachment of final batch ongoing
  - supplemental production batch launched
- Testing critical, yield (after SMD and after kapton attachment) to be determined
  - **need to speed up!!!!!!**
- Failure modes of the modules still to be understood, the results are too fresh
  - most often it is the SWB part that fails
  - two modules show problems with DHPT
  - have to collect the data and analyze
- plans for replacement
  - very little ….
    - thinner modules: 525µm → 450 µm
    - Switcher bumping on wafer level
    - thinner Switchers: 400µm → 100µm
    - more diagnostics on the module, dedicated probe pads where ever possible

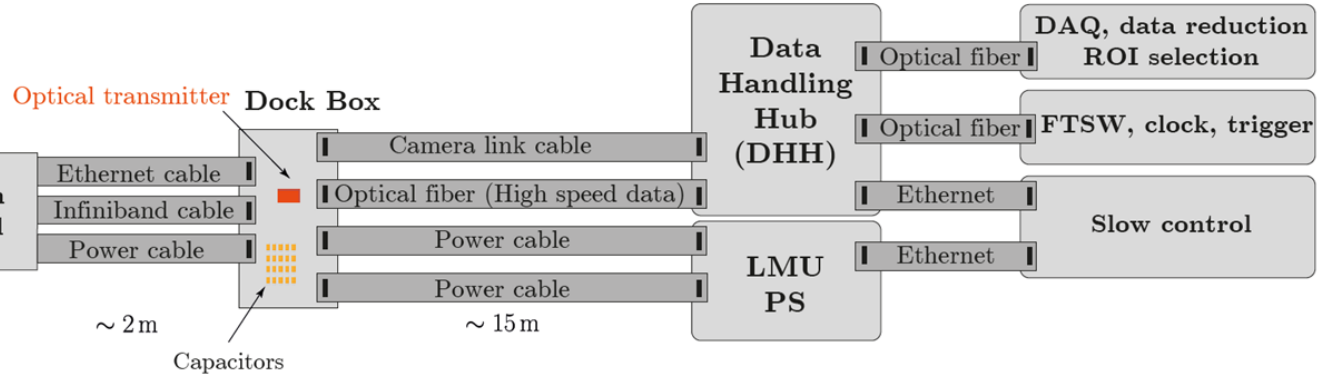
PXD system overview





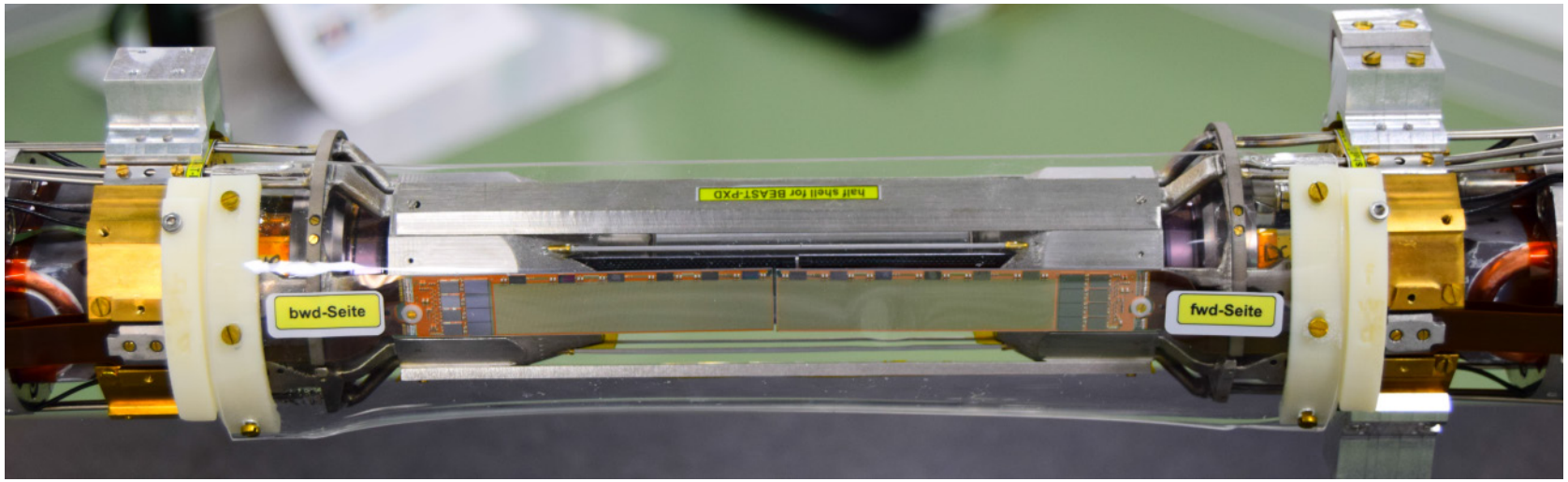


	Belle II PXD	
Radii	14, 22	mm
Sensitive length	90 (L1), 122 (L2)	mm
Sensitive width	12.5 (L1-L2)	mm
Number of ladders	8, 12	
Pixel size	55x50 & 60x50 (L1), 70x50 & 85x50 (L2)	μm^2
r/o time per frame	20	µs
Number of pixels	8	Mpix

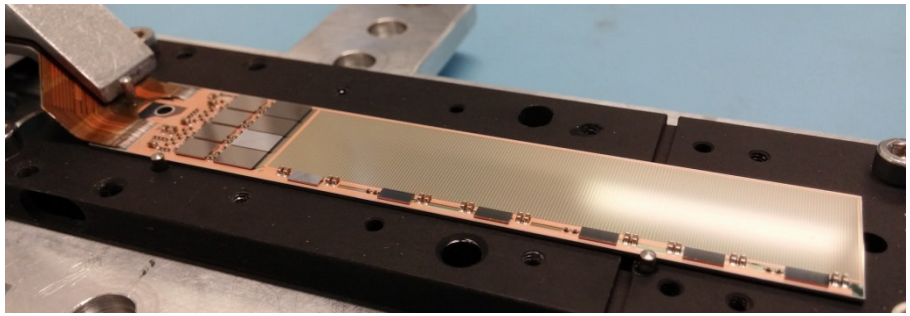


main activities in the past four months

- Phase 2 preparations: module testing, infrastructure, services, DAQ, installation …
  - ↳ **huge effort!! see Carlos' talk**



- **Main module and ladder production for Phase3**



x (40+20 contingency)

DEPFET PXD all-silicon module

DCDB (Drain Current Digitizer)

Analog front-end

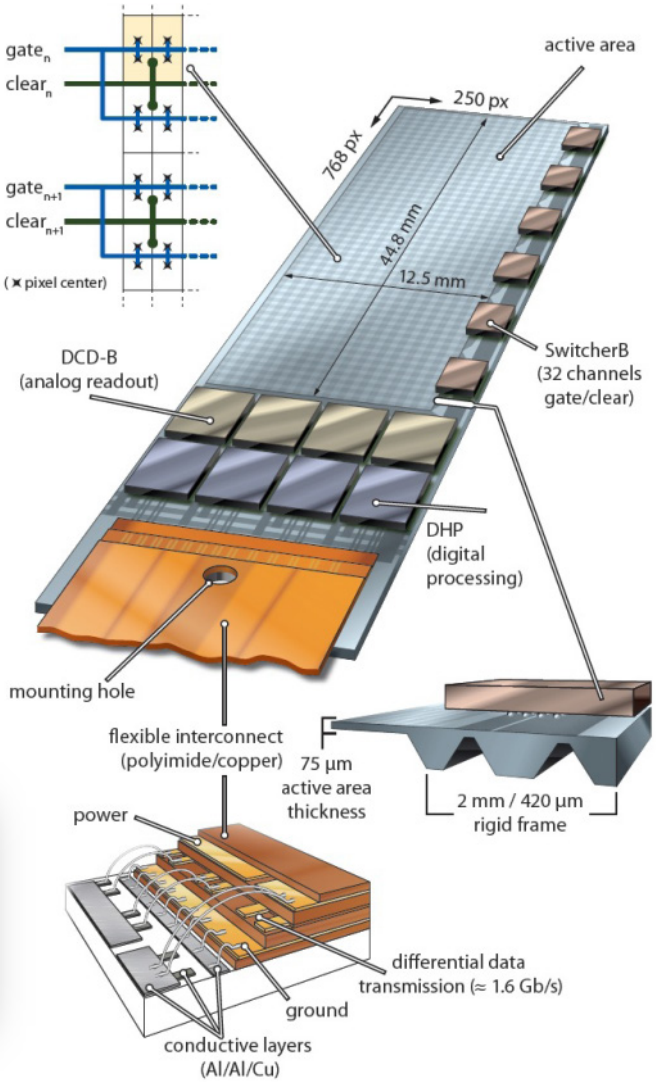
Amplification and digitization of DEPFET signals.

- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- UMC 180 nm
- Rad hard design

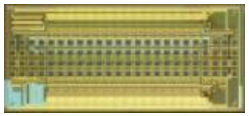
all components are available

sensors, DCD, DHP, Switcher, kapton

pre-tested before assembly



SwitcherB - Row Control

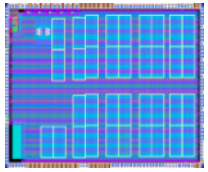


AMS/IBM HVCMOS 180 nm

- Size 3.6 × 1.5 mm^2
- Gate and Clear signal
- 32x2 channels
- Fast HV ramp for Clear
- Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)

First data compression



TSMC 65 nm

- Size 4.0 × 3.2 mm^2
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)