Initiation of dealitispills of PAD:



Outline

Beamspills What could happen? A) Sensor

common discussion B) Sensor in connection with Switcher and DCD Precautions?



beam spill/beam loss - known from old LEP days

beam is out of control, hits the beam pipe ... and detectors

generates huge amount of charge, diodes are getting low ohmic, voltage breakdown

AC coupled strip detectors oxide damage, since full bias voltage drops across integrated coupling capacitors



Initiative coming from SVD



They do:

Power shut down (at least HV) if charge corresponding to 1nC / per strip is accumulated in a diamond sensor -> 50nC /cm²

Question -> PXD: possible common reactions!

PXD: situation a bit easier (less HV)

but much more complicated, no experience about possible damage mechanisms



We probably cannot protect the PXD against a total beam loss directly hitting the detector

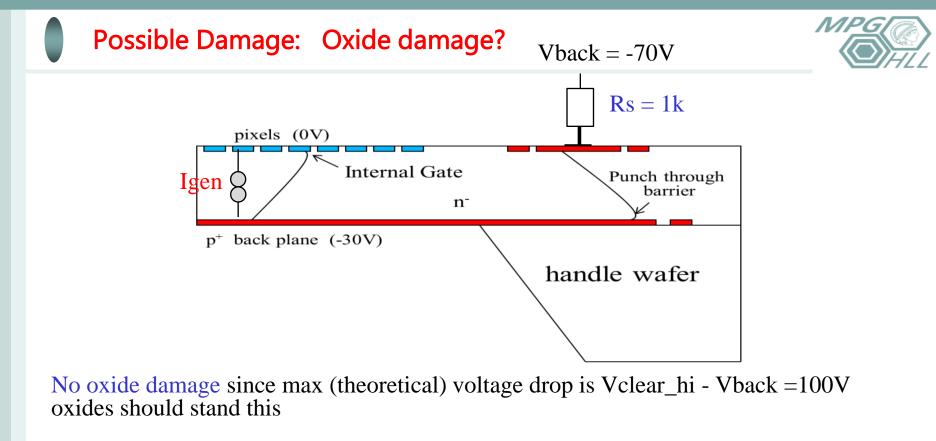
But we should be prepared at least for milder showers ...

Since we don't know neither the total amount of generated charge nor the time structure

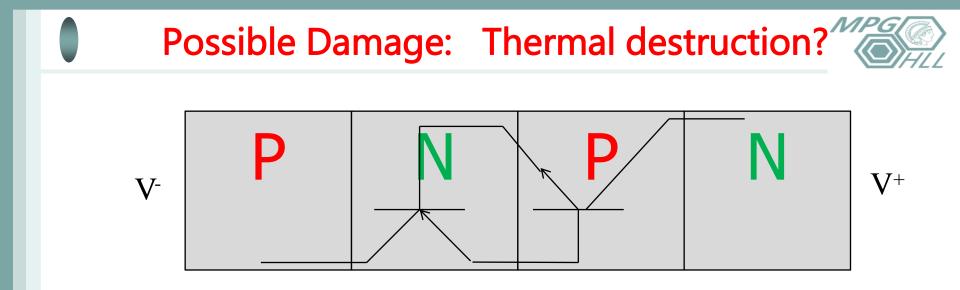
General reasonings and speculations \otimes



A) damage mechanisms in the sensor



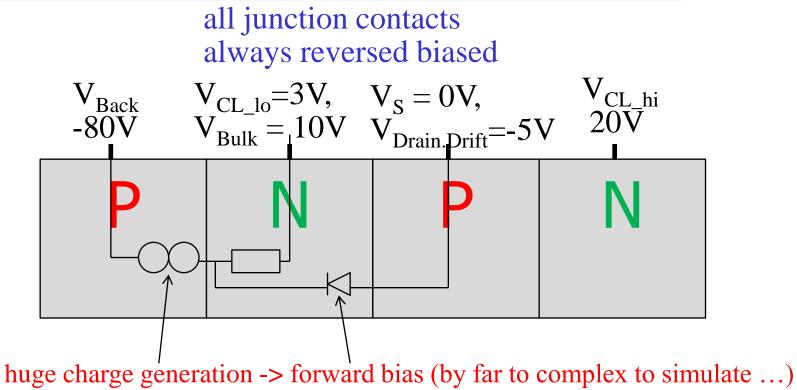
Even relaxed: max voltage drop cannot occur in the matrix, for instance: Igen = $70mA \rightarrow all$ the voltage drops over Rs In addition: Rs >> Ron (Clears) all in parallel, matrix will be kept at frontside potentials



Forward bias of base emitter diodes The by intention -> thyristor ov parasitically -> latch up as in CMOS chips get destructive (thermal) and non destructive latch up possible device switchs off if voltage drops and current falls below holding current

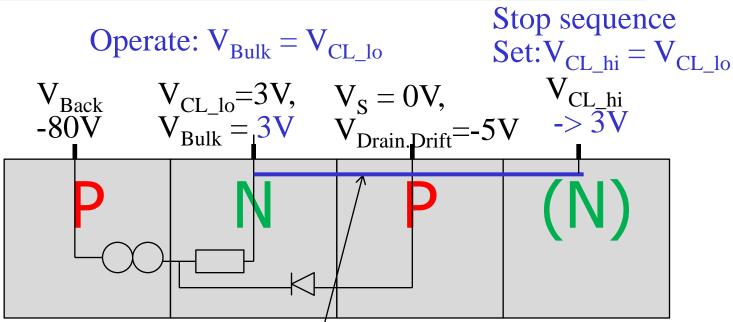
The hole device is swammed over with carriers getting very low ohmic





What would help in case of beam spill





Thyristor becomes a pnp bipolar transistor with partially ,floating' gate. Part of the generated electrons will be amplified other part extracted N - contacts.



B) damage mechanisms within Switcher and DCD in connection with sensor





His main concern: all DEPFET Drains in the matrix are shorten to Source DCD inputs at 7V, DCD breaks

my question? If DCD power lines are switched off in time (current limits) it shouldn't harm ... Can this be realized?





Switcher ouputs have very high driving capability

all out puts in parallel ... it helps

Any mechanism possible theta Vsub is getting to positive ?

Reactions



A) Same as Strips, controlled bias ramp down? response time?
B) Gated Mode ?
C) Exceeding the current limits ...
D) Emergency power shut down?
E) Nothing?