Berlin/Zeuthen Powerboard shielding

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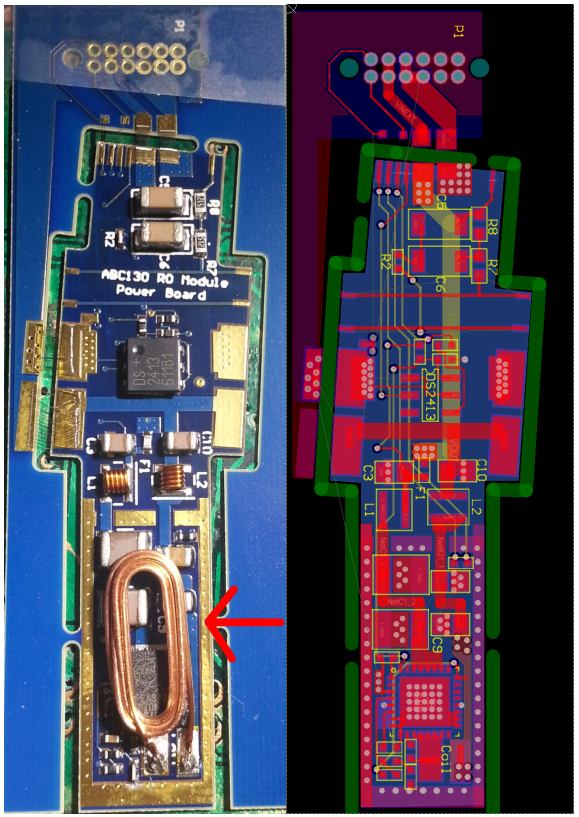
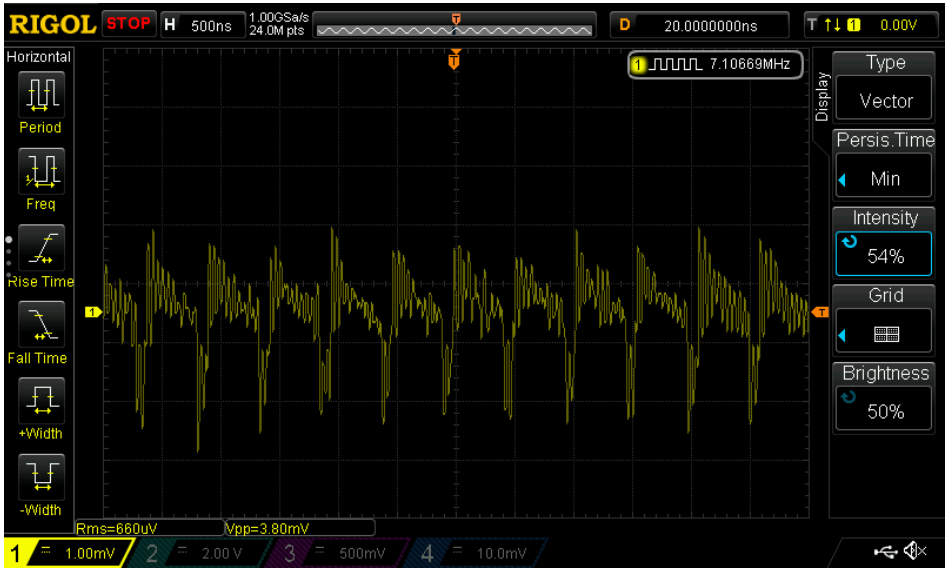
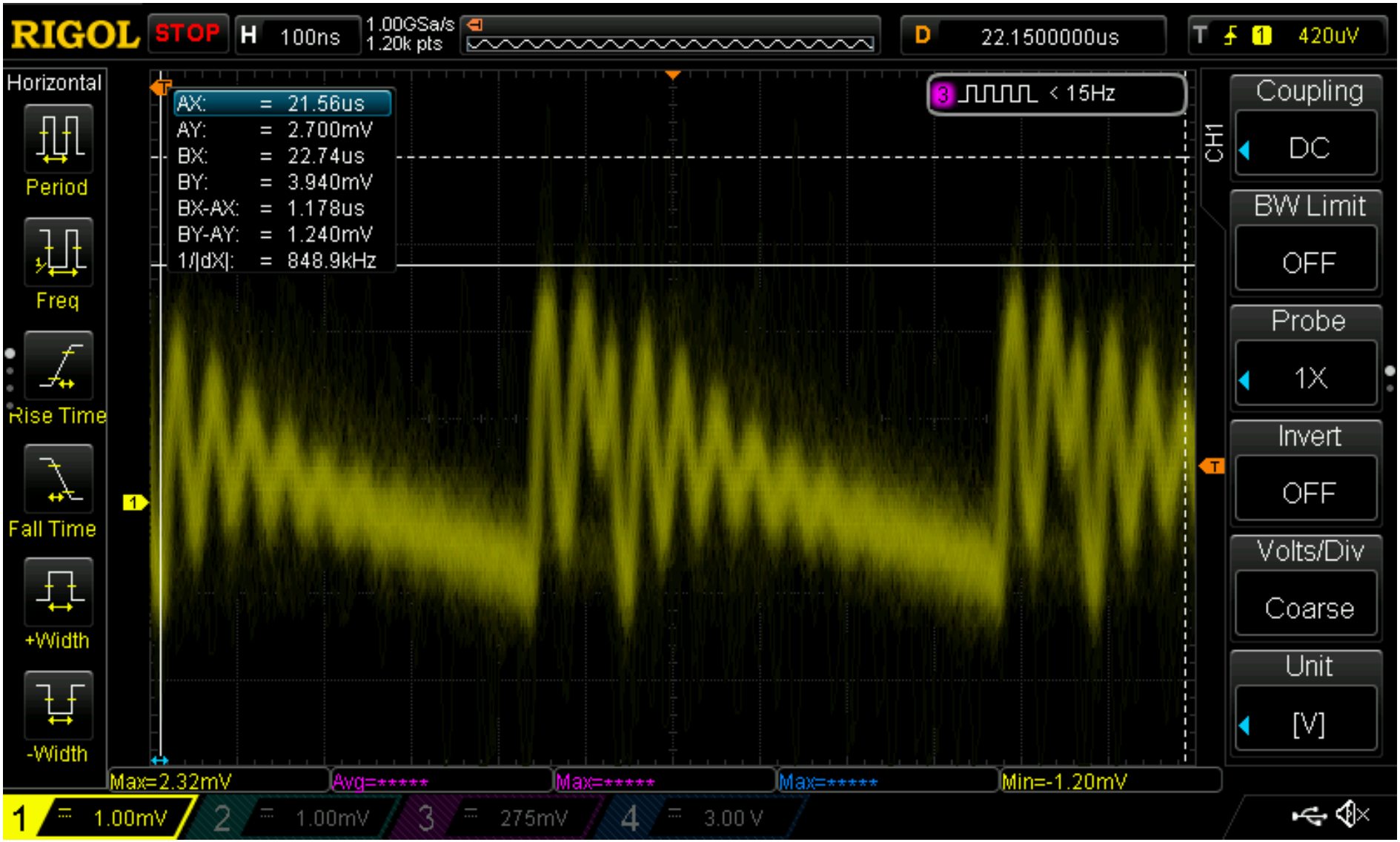
know situation

- all R0 powerboards i checked leak at indicated spot
- definitely properly seam solderd box - especially at this spot
- leakage seems independent of load
- small changes with input voltage
- only thing there is vias of internal trace of pre pi filter output
  - ground vias don't shield internal layer there in this version of powerboard
  - internal trace is longer than leak

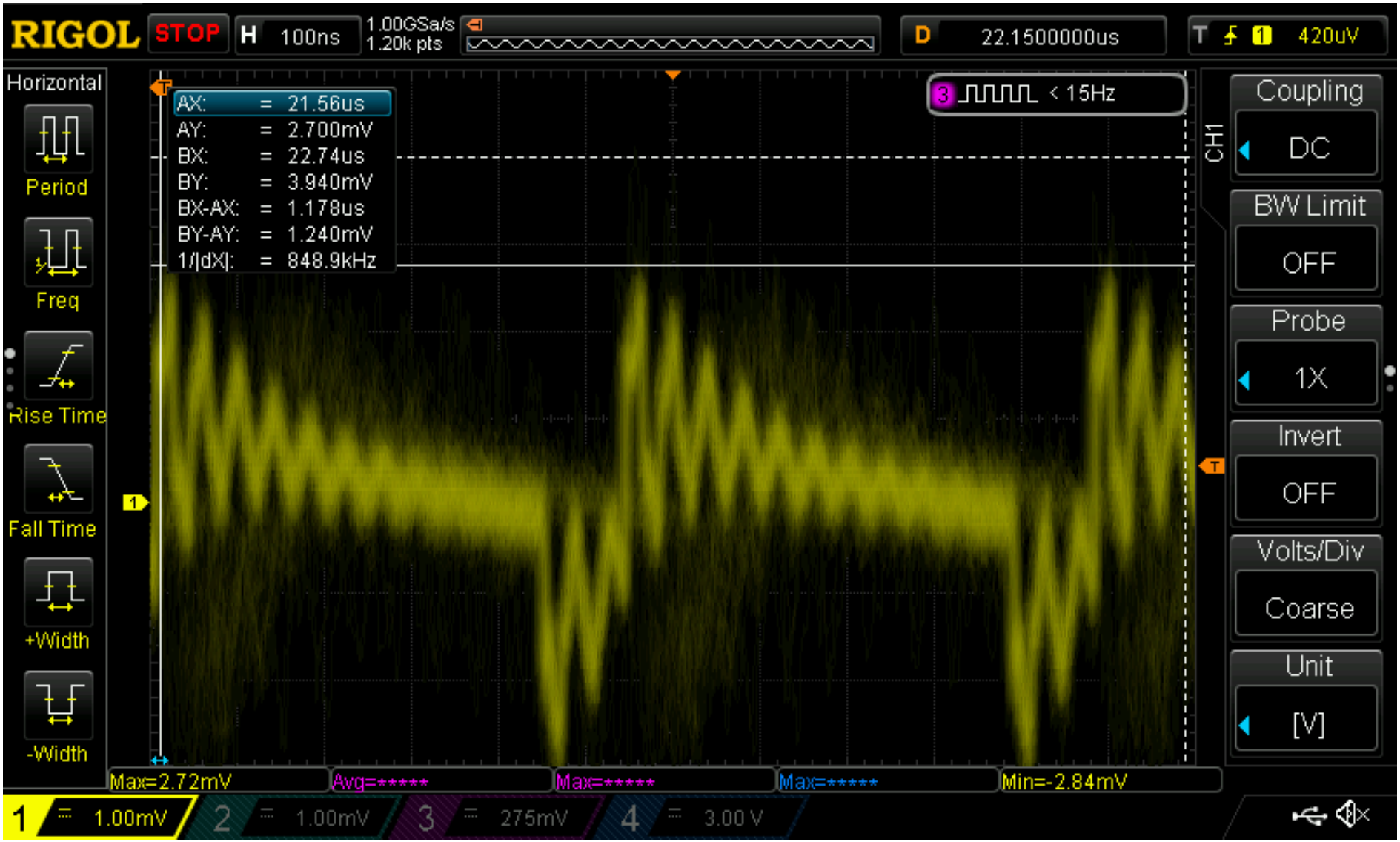




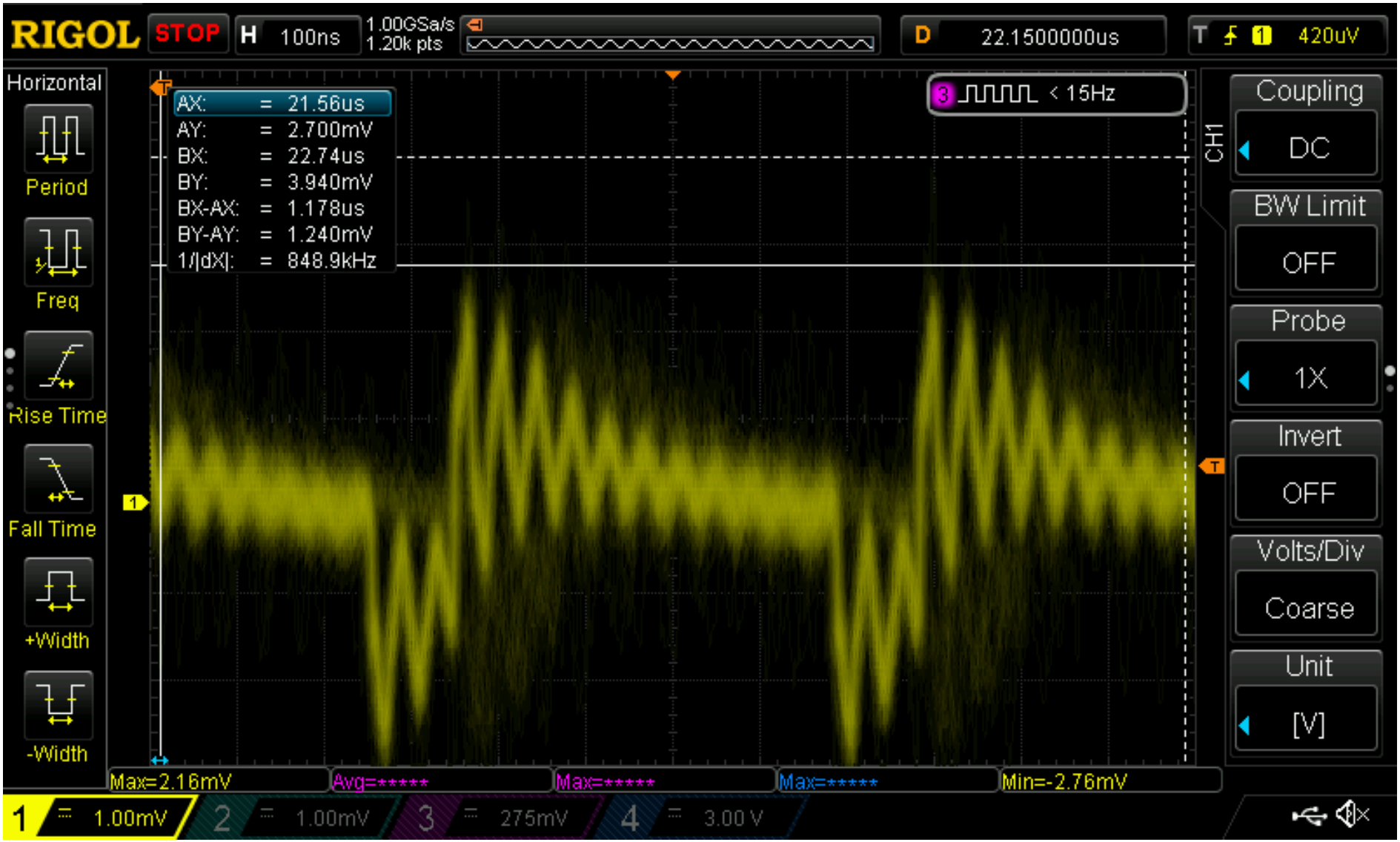
0.1mm copper + SnBi solder



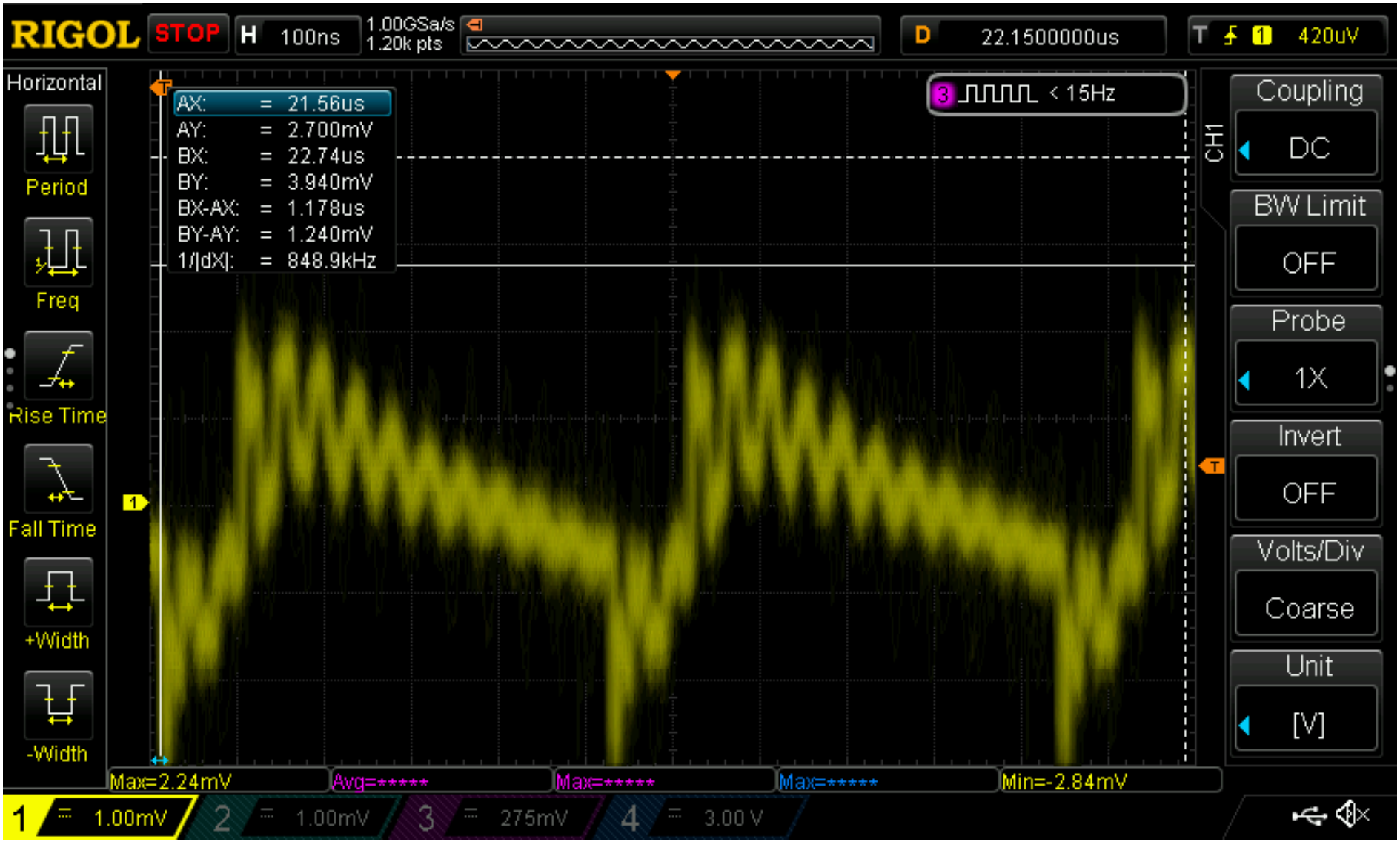
0.1mm copper + Sn solder



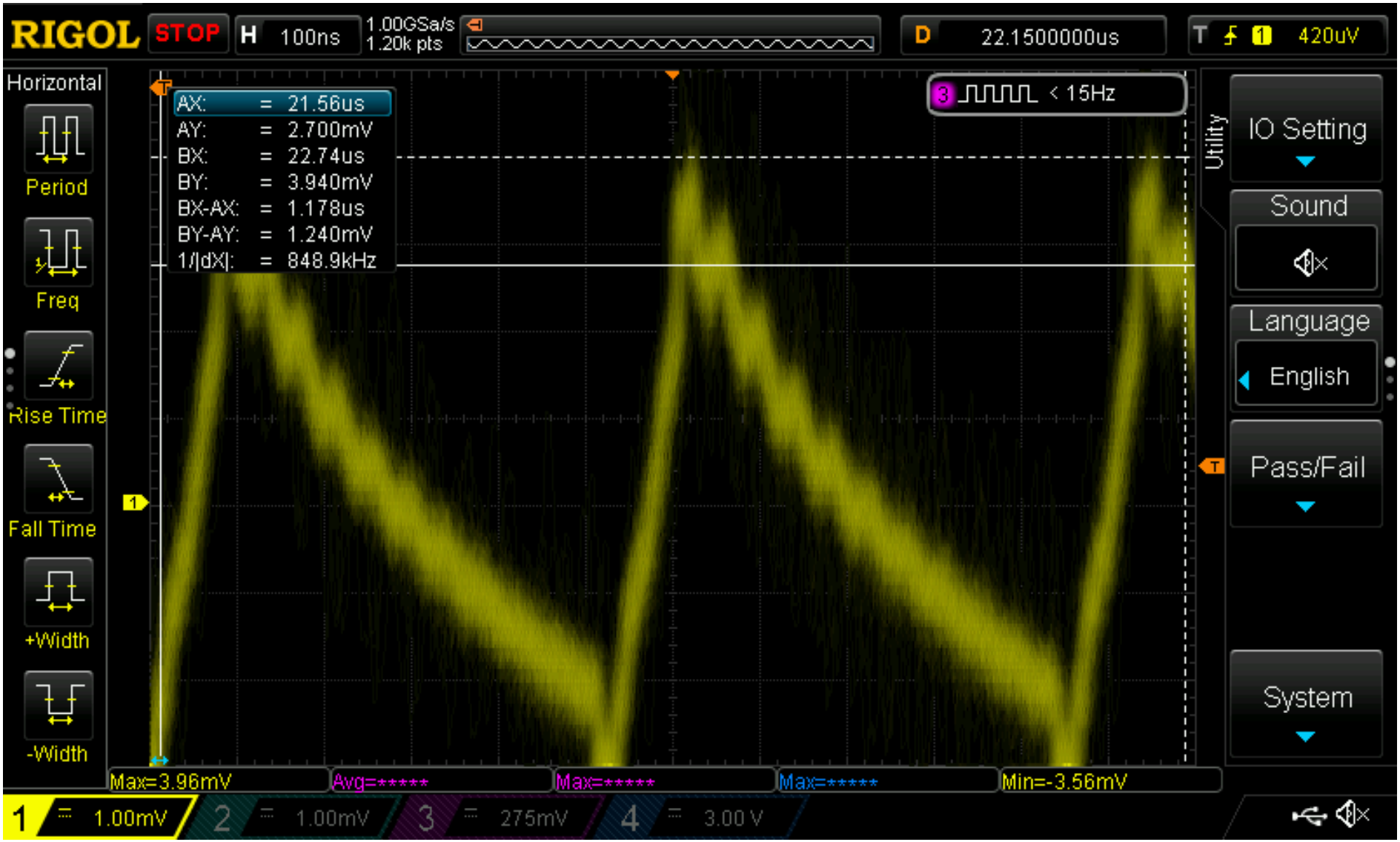
0.1mm copper + SnPb solder



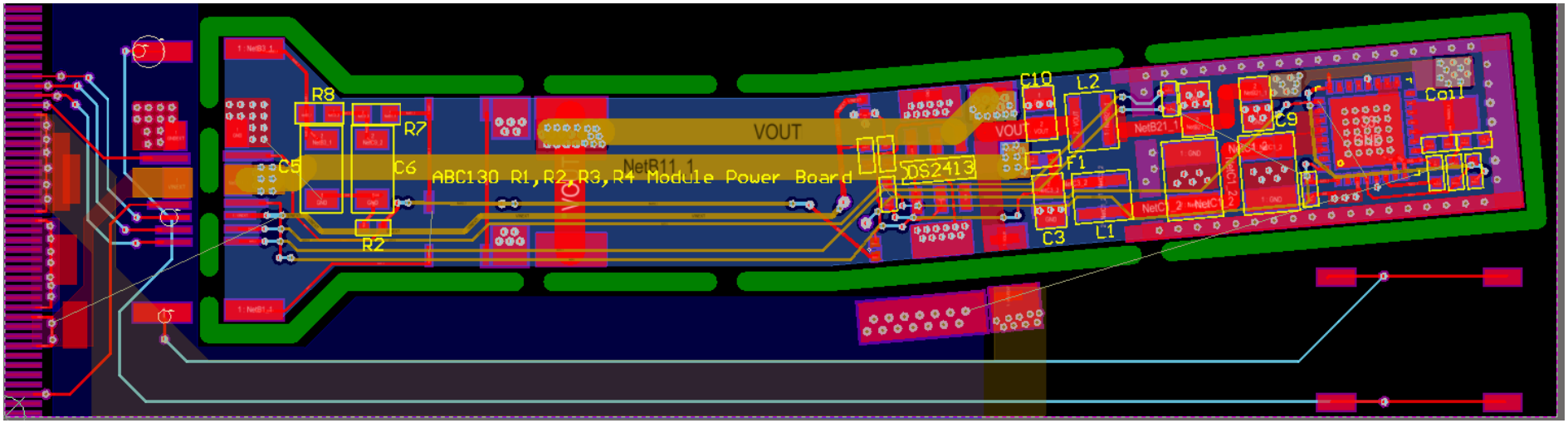
0.2mm copper + SnBi solder



Ash's box + SnBi solder

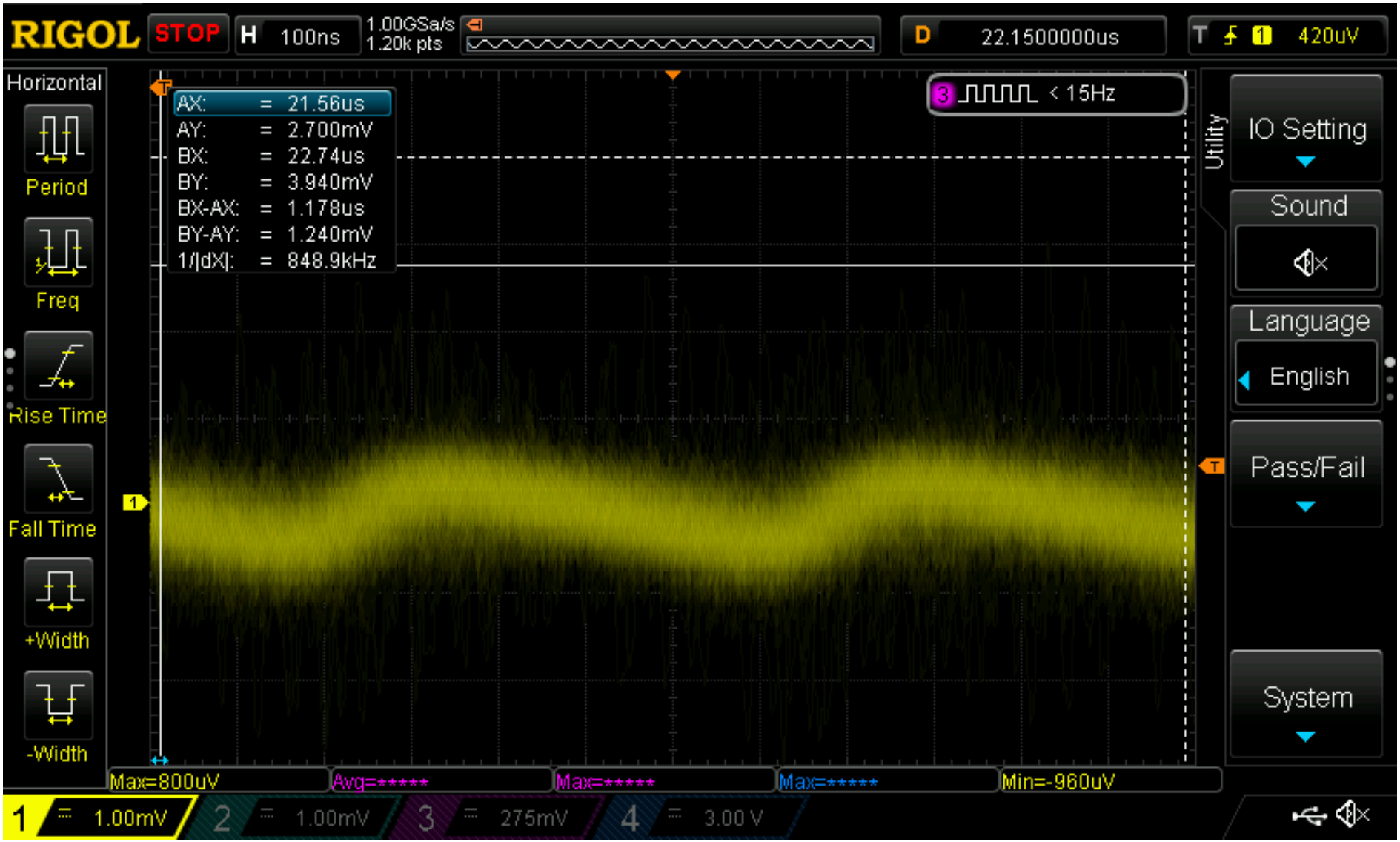


R1 to R4 powerboard for electrical petal



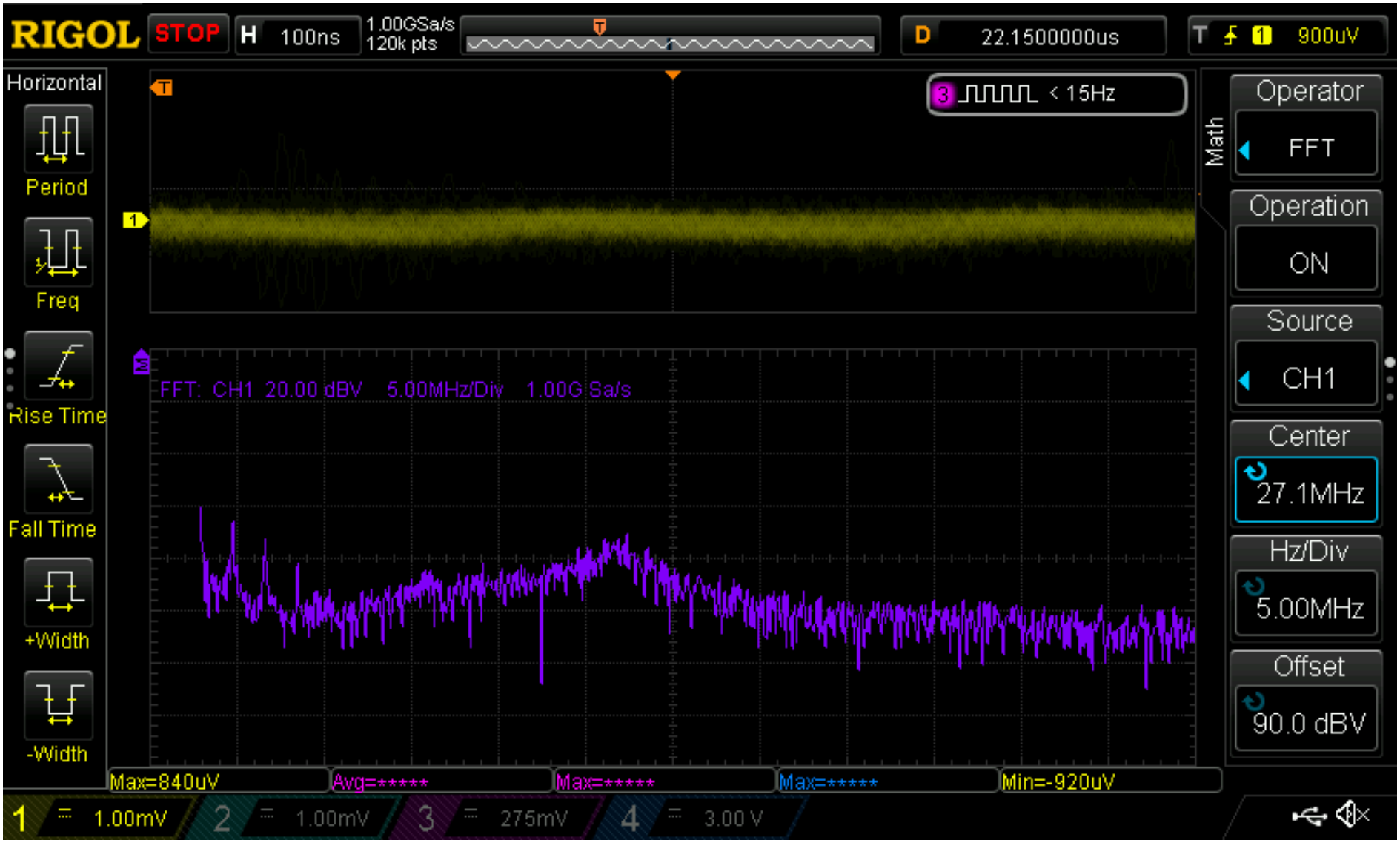
- vias in shieldbox area + below FEAST through all instead of just to second layer
- rest mostly exactly the same design as R0 powerboard

R1-R4 – 0.1mm copper + SnBi solder



R0 with fft

RIGOL
STOP
H 100ns
1.00GSa/s
120k pts
D 22.1500000us
T 400uV
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
< 15Hz
FFT: CH1 20.00 dBV 5.00MHz/Div 1.00G Sa/s
Math
Operator
FFT
Operation
ON
Source
CH1
Center
27.1MHz
Hz/Div
5.00MHz
Offset
90.0 dBV
Max=2.72mV
Avg=*****
Max=*****
Max=*****
Min=-2.88mV
1 2.00mV
2 1.00mV
3 275mV
4 3.00 V

R0 with Ash's box with fft

R1-R4 with fft