Future of Silicon Trackers (at LHC and beyond)

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With many thanks to my colleagues who kindly provided material
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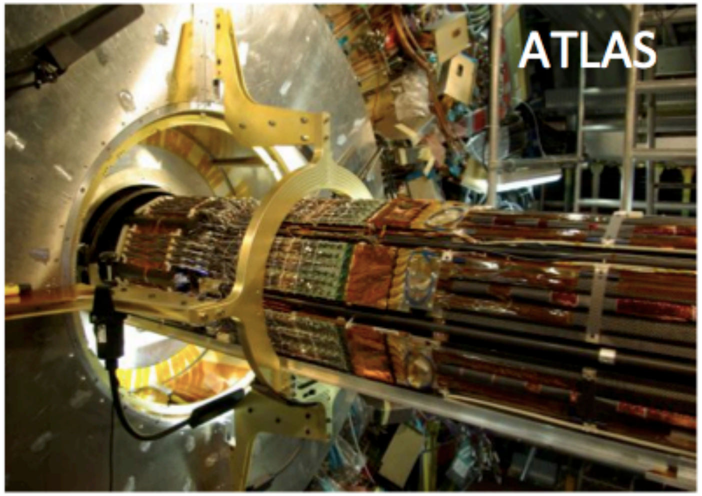
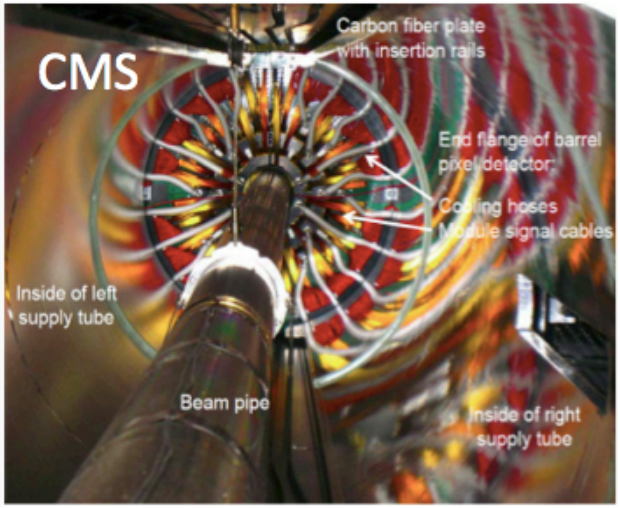
Outline

- Silicon Tracker Upgrades towards the High-Luminosity LHC
- Developments for hybrid and monolithic pixel detectors
- Silicon tracker combined with timing capabilities
- Future in silicon to module integration

Large Hadron Collider at CERN

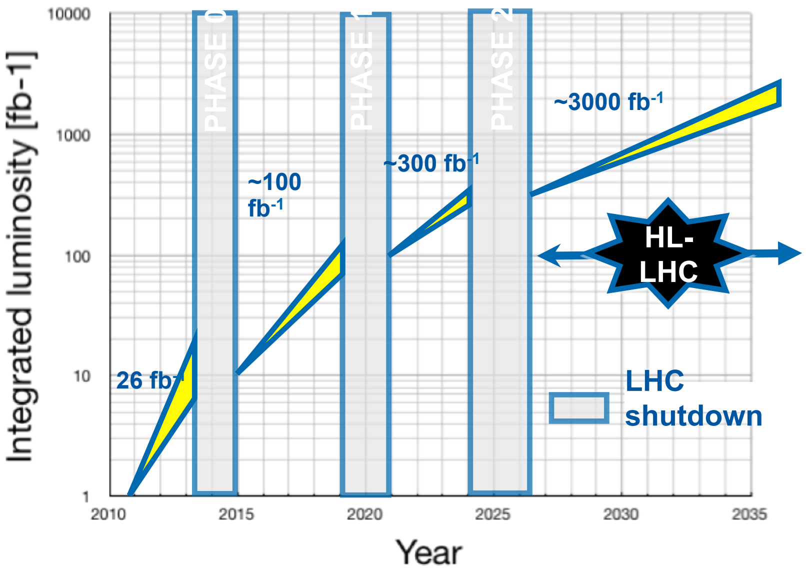
Our starting point – LHC Silicon Trackers in operation

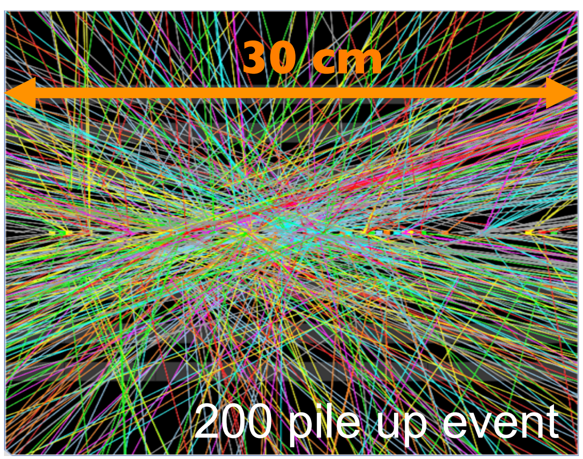




Current silicon tracking detectors at LHC are composed of Silicon Strip and / or Silicon Hybrid Pixel detectors

High Luminosity - LHC





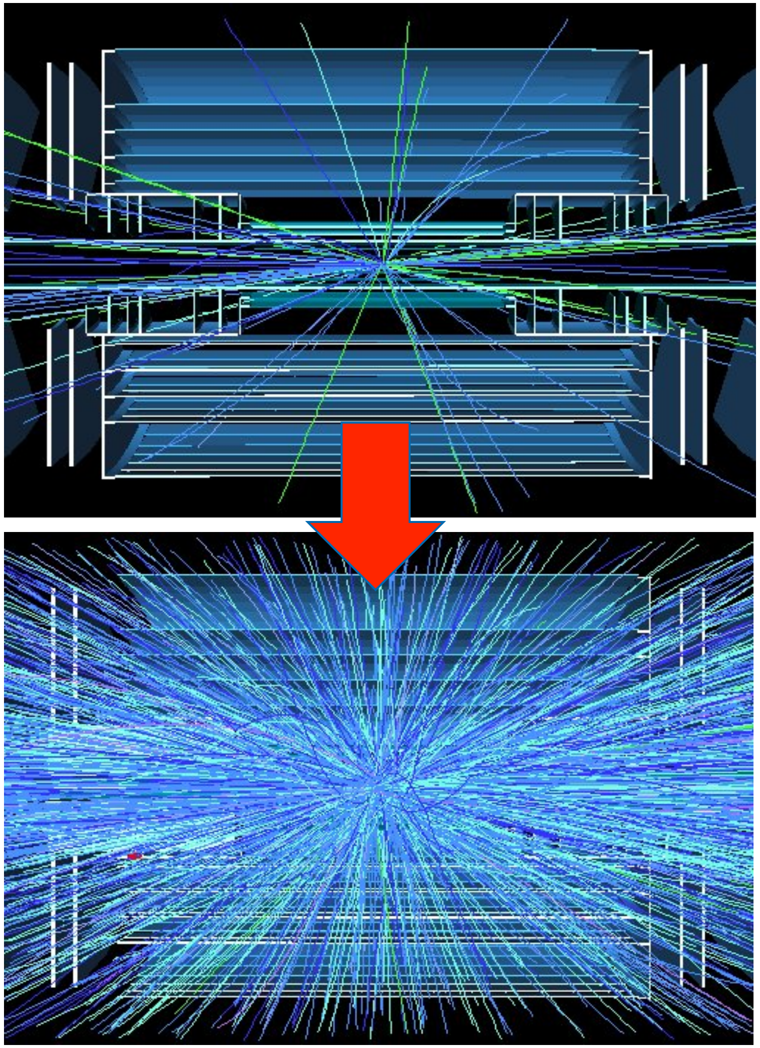
HL-LHC (High Luminosity LHC)

- Collisions to start mid-2026
- Maximum leveled instantaneous luminosity of 7.5 x 10^{34} cm^{-2} s^{-1}
  - Currently exceeed >1 x 10^{34} cm^{-2} s^{-1}
- ~3000 fb^{-1} Integrated luminosity to ATLAS/CMS over ten years
- 200 (mean number of) interactions per bunch crossing.
  - Original design for 25 interactions per bunch crossing

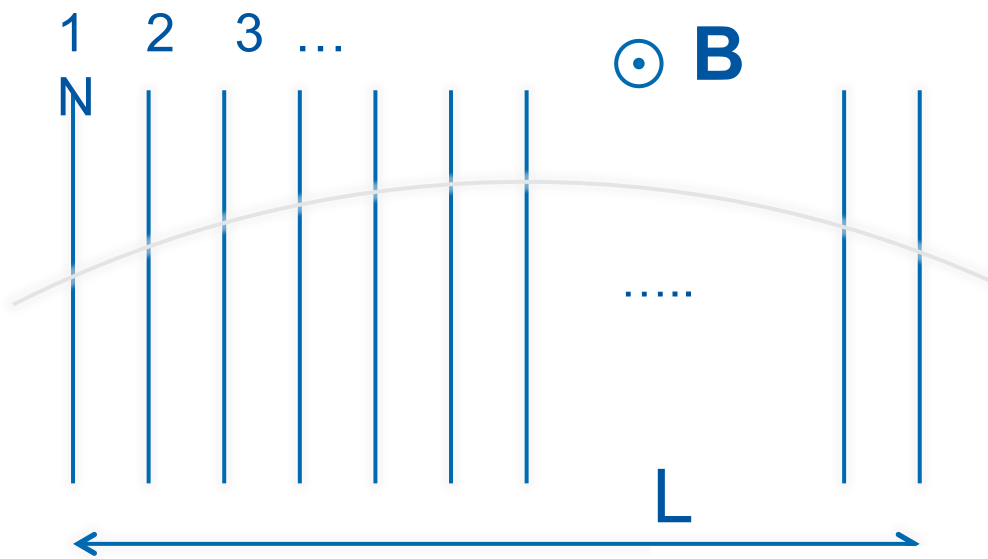
Challenges for the future

- Increased luminosity requires
  - Higher hit-rate capability
  - Higher segmentation
  - Higher radiation hardness
  - Lighter detectors

- Radiation hardness improvement compared to now
  - Phase-2 approx. factor 10



Tracking - momentum resolution



σ … point resolution/plane

X_{tot}/X_0 … total material budget

Position Resolution

Pixel = high spatial resolution
O(10μm) on hybrid and down to O(1-3μm) on MAPS

$$\frac{\Delta p_t}{p_t} = \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720\,(N-1)^3}{(N-2)\,N\,(N+1)\,(N+2)}}$$

$$\approx \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720}{N+4}}$$

Multiple Scattering

Pixel = light detectors
Thin detectors on light carbon fibre supports O(1-2%/0.2% X/X0 per layer)

$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}\,\frac{12+(N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

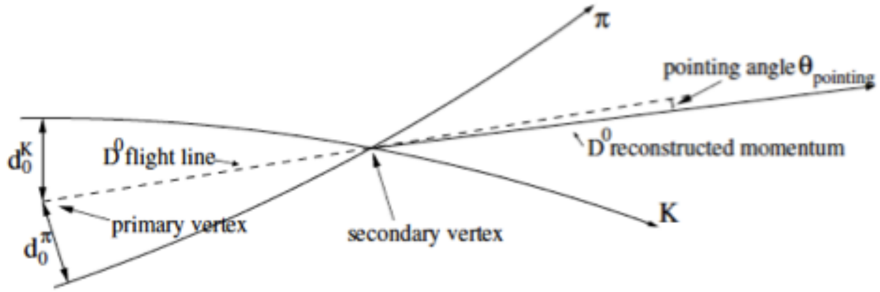
$$\approx \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}}$$

$$\approx \frac{0.0542}{\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}}$$

W. Riegler

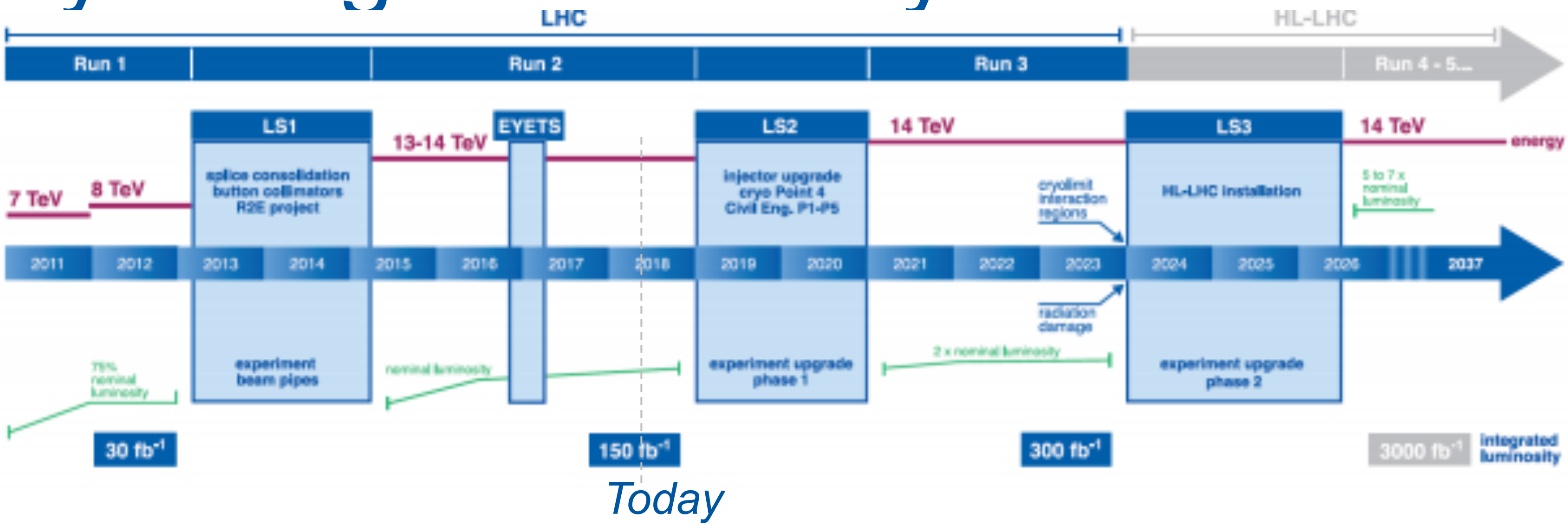
Impact parameter

- Secondary vertices reconstruction strongly depends on impact parameter resolution
  - d0 in r/phi (bending plane)
  - Z0 alone beam direction



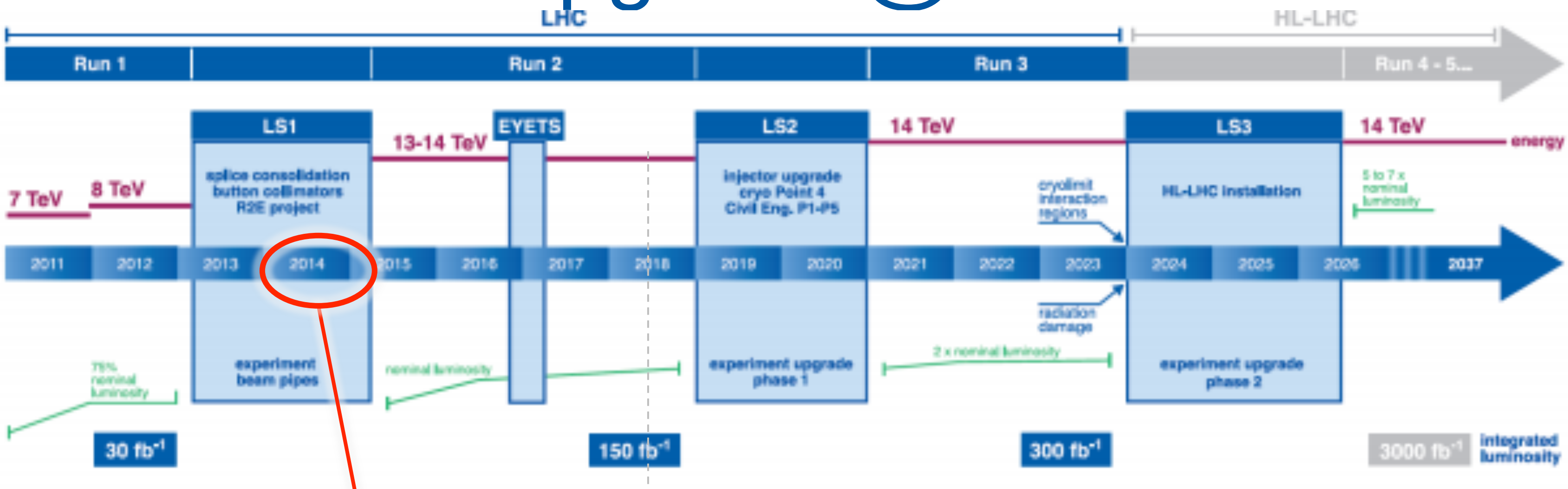
- Impact parameter resolution is strongly effected by
  - **Intrinsic point resolution** and alignment at higher momentum
  - **Multiple scattering in detector material** (in particular for low pt tracks)
- Look for tracking solutions which combine **small pixels** with **thin detectors (particular on the innermost layers)**
- They need to be **radiation hard** and include complex readout architectures to cope with **high hit rates**

Way to High Luminosity

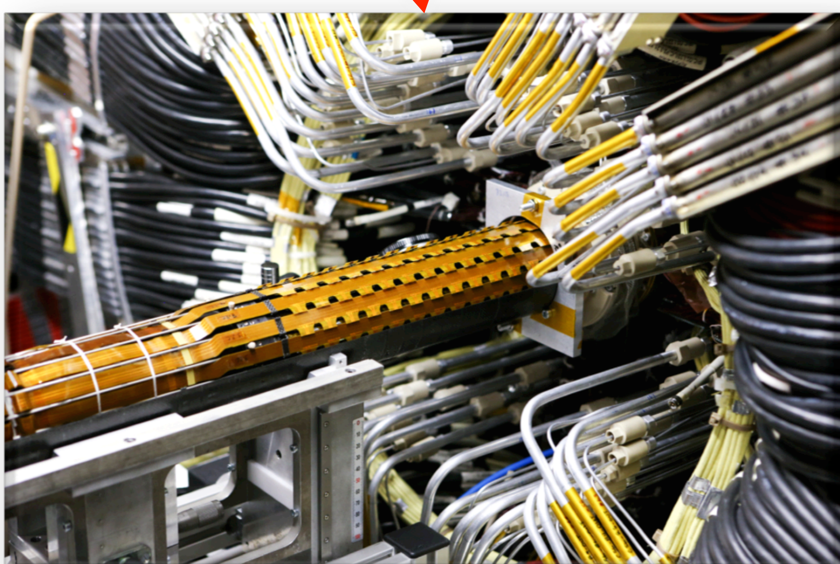


- Upgrade of Accelerator System to achieve high beam intensity
- Upgrade of Experiments:
  - Tracker will be replaced for better precision and high rates & radiation
  - New Trigger systems are essential to select rare events & new physics
  - New DAQ system & Reconstruction software to cope with enormous data volume

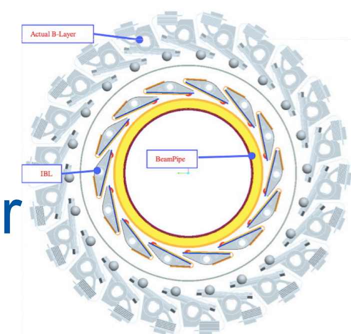
Pixel Detector Upgrade @ LHC



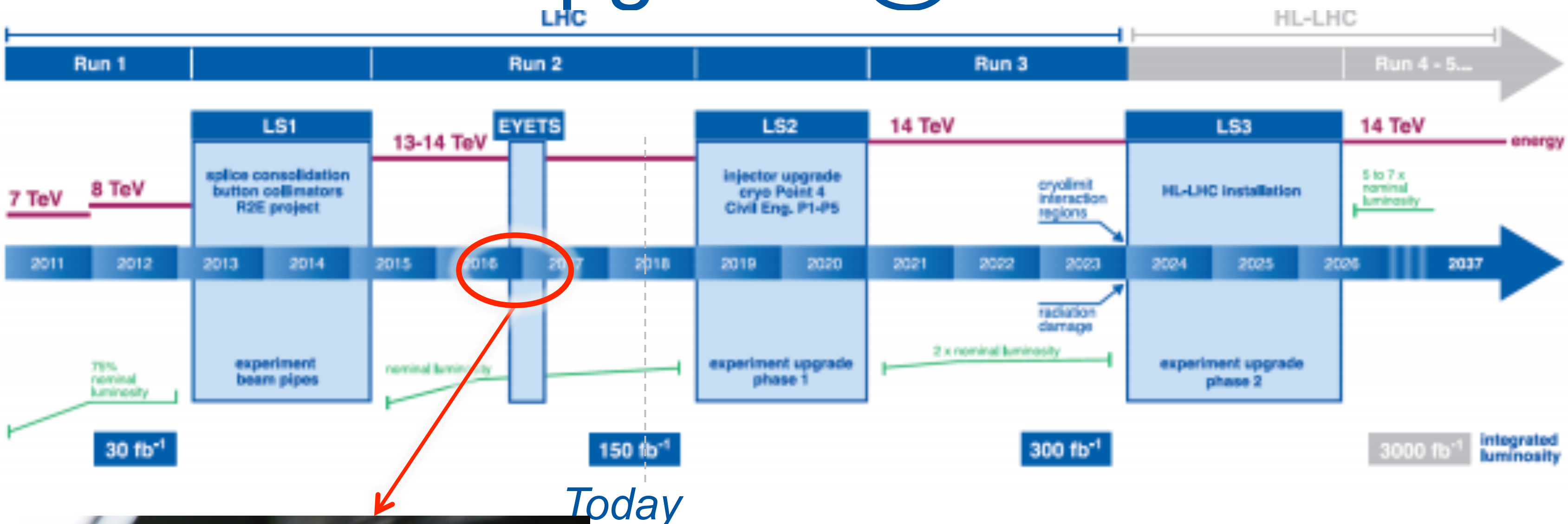
Today

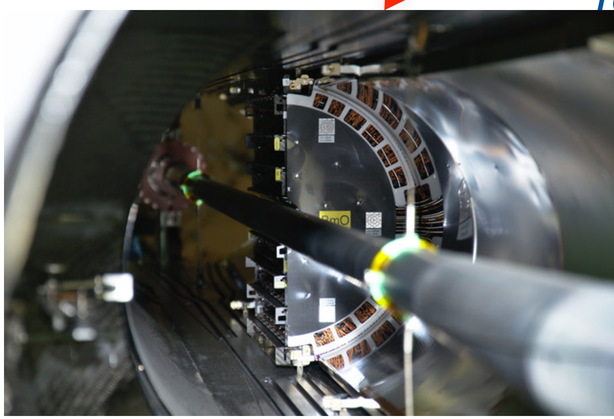


- **2014: ATLAS**
- Installation of IBL "Insertable-B-Layer " system
- ATLAS 4 Layer Pixel detector system

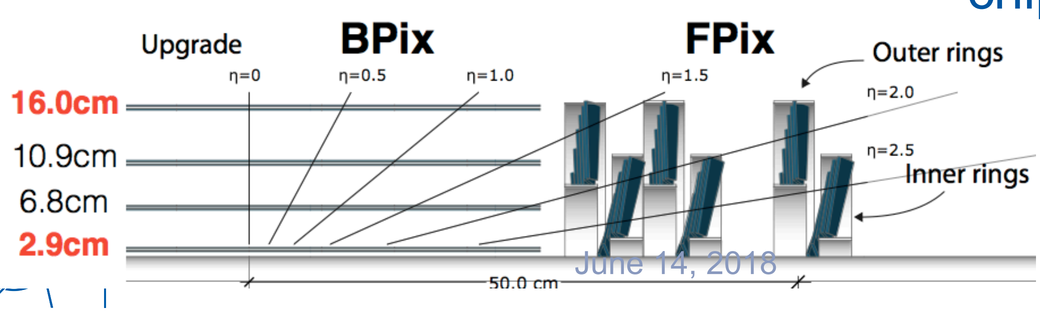


Pixel Detector Upgrade @ LHC

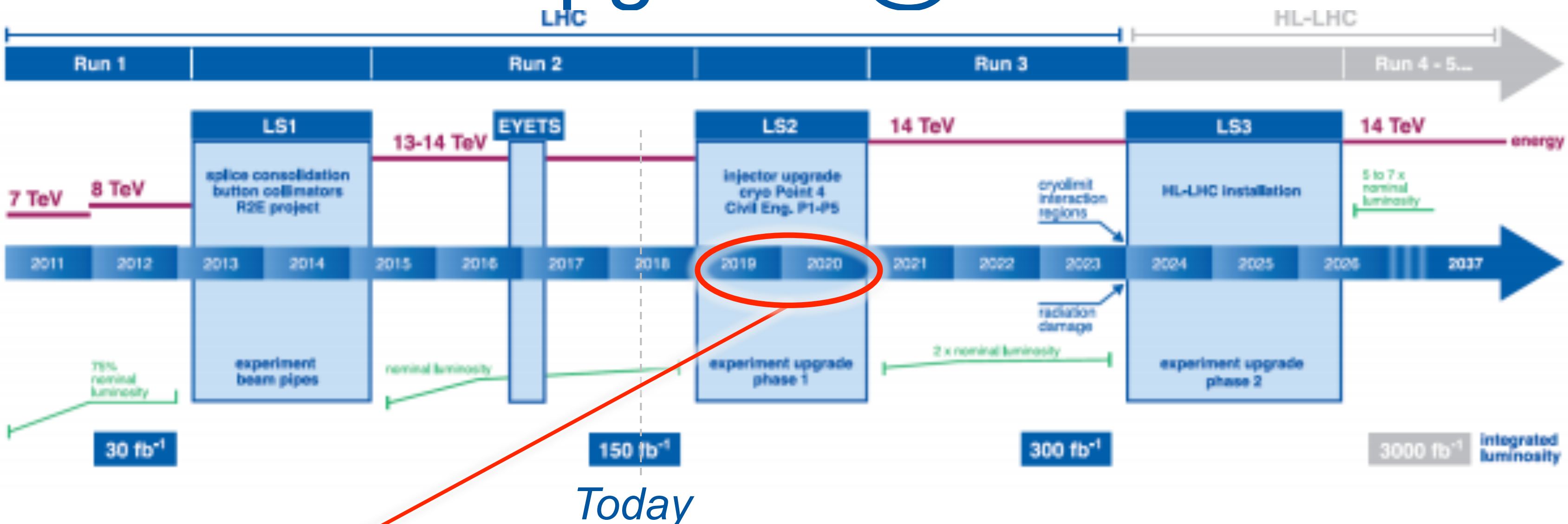


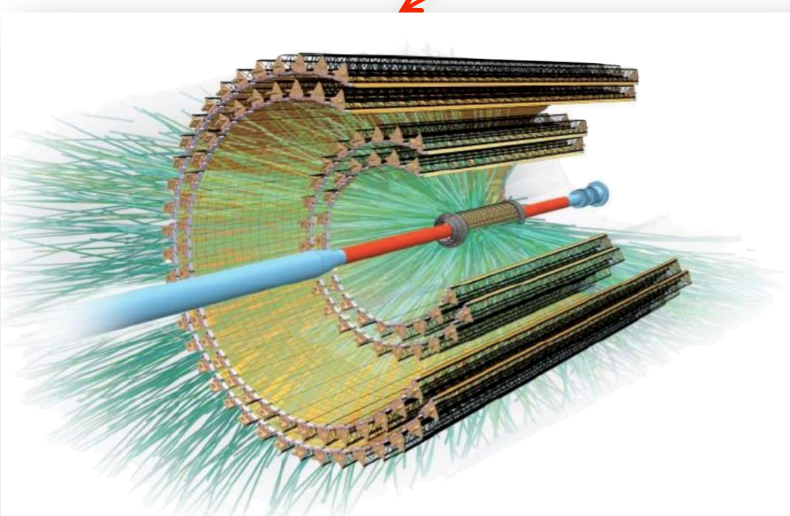


- **2016/17: CMS**
- Installation of new 4-Layer Pixel Detector for CMS
- Complete replacement for better performance with new sensors, FE-chips, mechanics, services



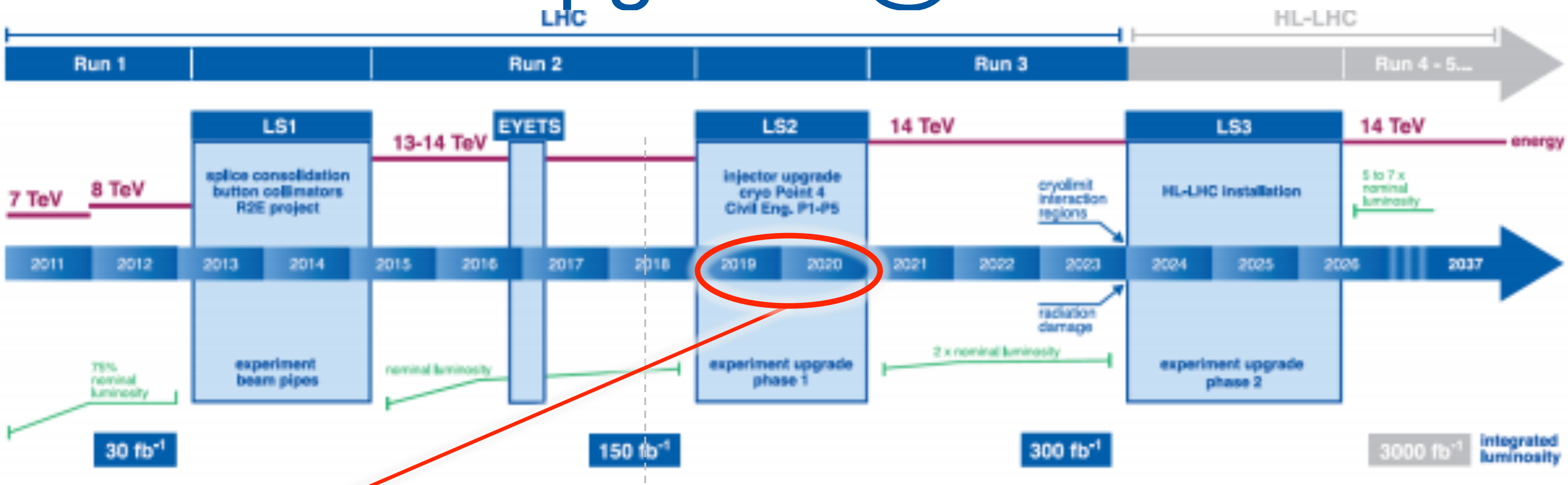
Pixel Detector Upgrade @ LHC



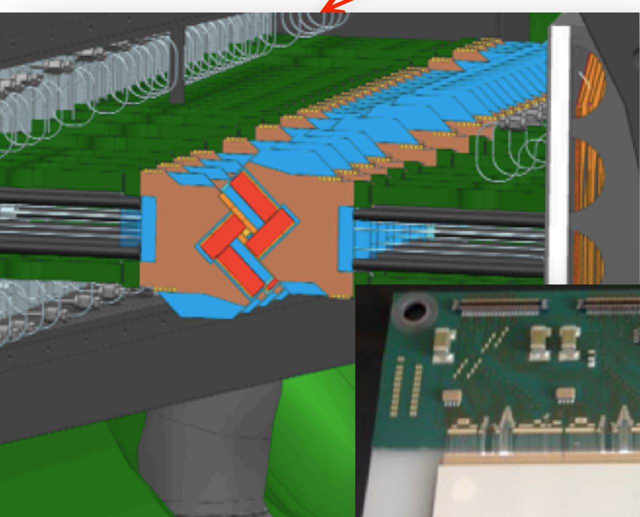


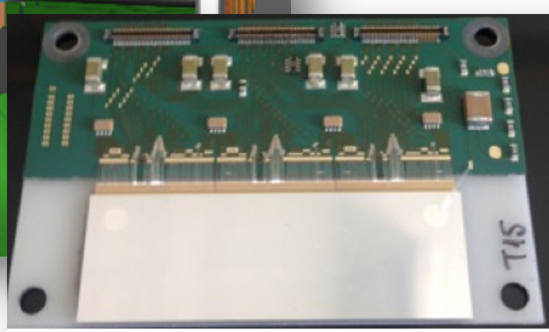
- **2019/20: ALICE ITS**
- First LHC Tracker based on CMOS monolithic sensors
- 7 layer/10m^2 system of CMOS sensors will replace hybrid pixel+silicon-drift+strip ITS
- Better tracking and & vertexing performance combined with high readout rate

Pixel Detector Upgrade @ LHC



Today

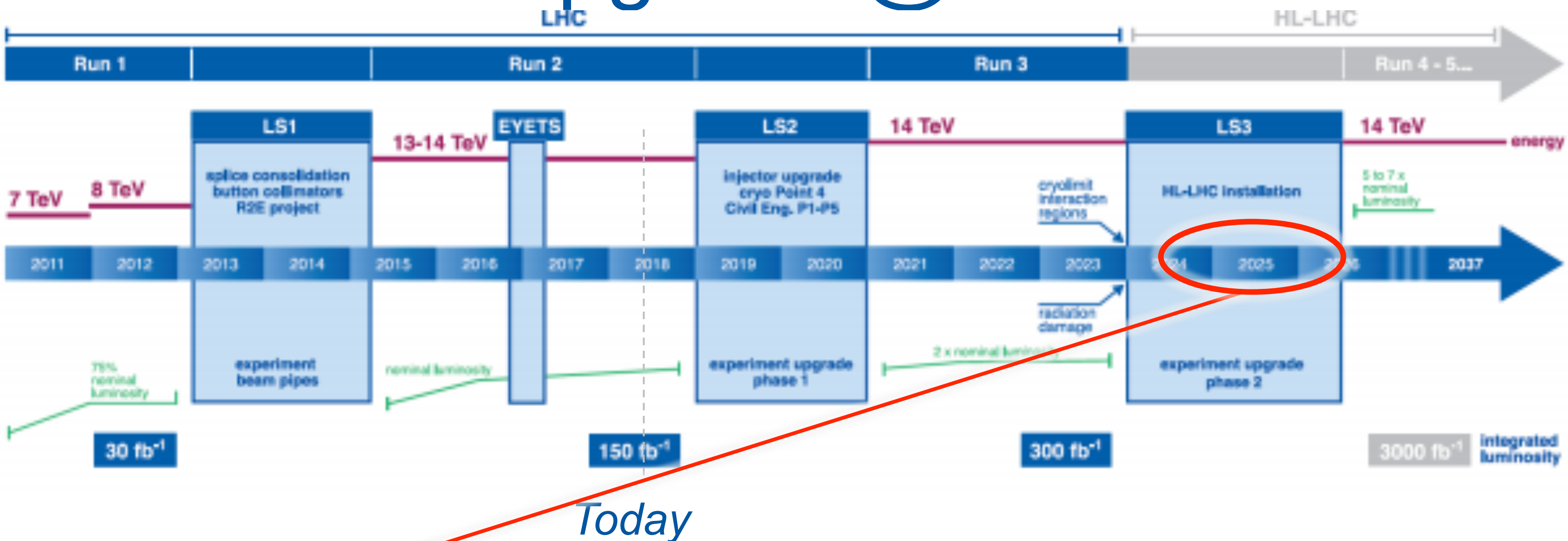


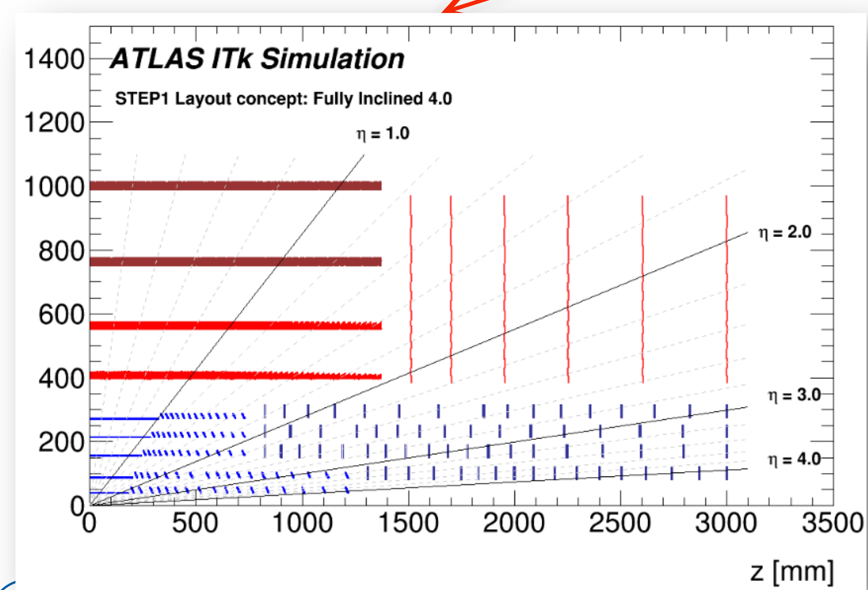


Prototype triple sensor bump bonded to a TimePix3 ASIC (predecessor of VeloPix)

- **2019/20: LHCB VeloPix**
- New VeloPix Pixel Detector replaces strip detector
- Improve sensitivity to very rare decays
- High data rate capability!
  - Readout @ 40MHz

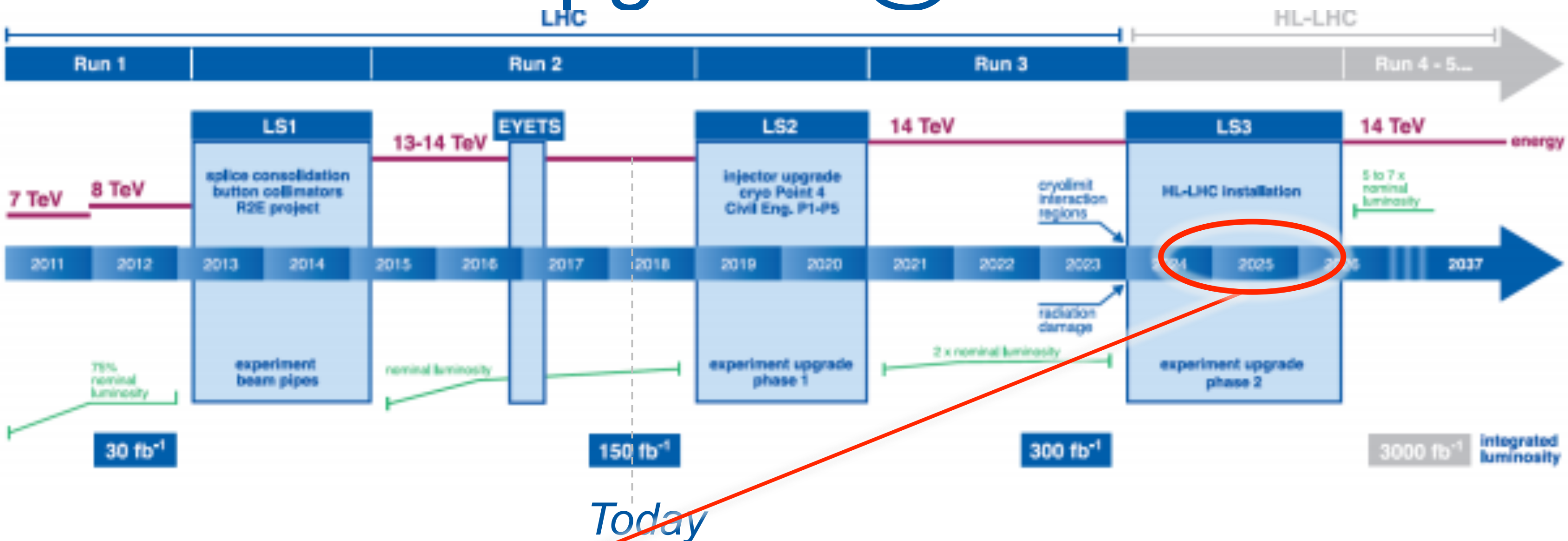
Pixel Detector Upgrade @ LHC

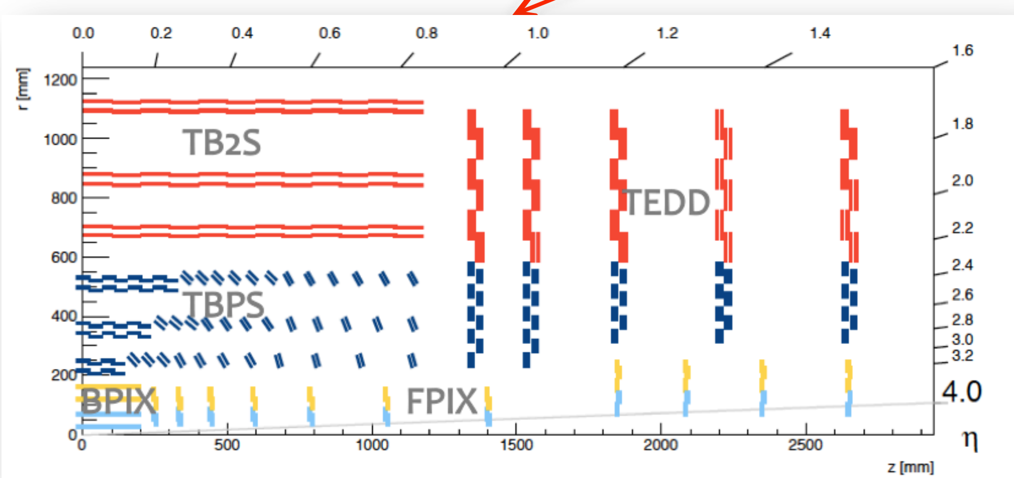




- **2024/25: Phase 2 ATLAS**
  ATLAS completely replace its trackers
- ~ 160 m^2 silicon strips
- ~10 m^2 silicon pixel

Pixel Detector Upgrade @ LHC

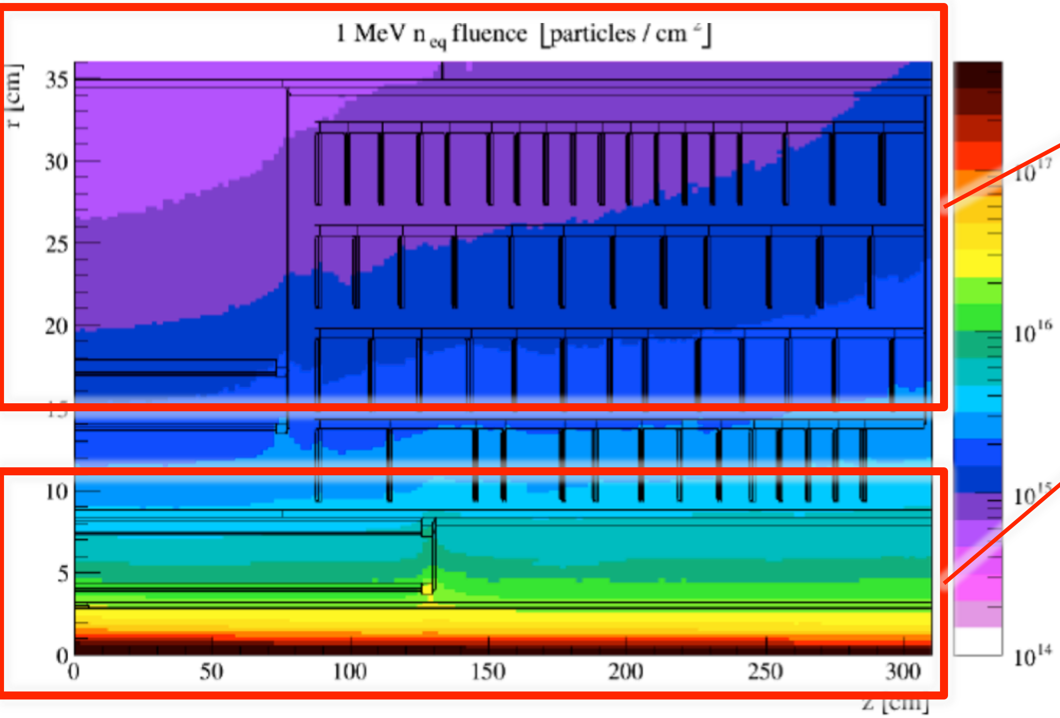




- **2024/25: Phase 2 CMS**
  CMS completely replace its trackers
  - Based on double layers including track trigger

The environment at HL-LHC

- Radiation level, hit rates and bunch structure for silicon detector dominate the development of sensors and Front-end electronics
  - 25ns BC
  - L1 trigger rate (e.g. ATLAS 4MHz)

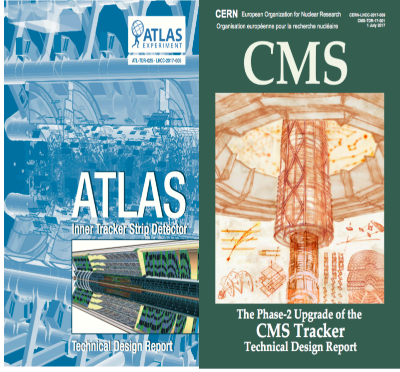


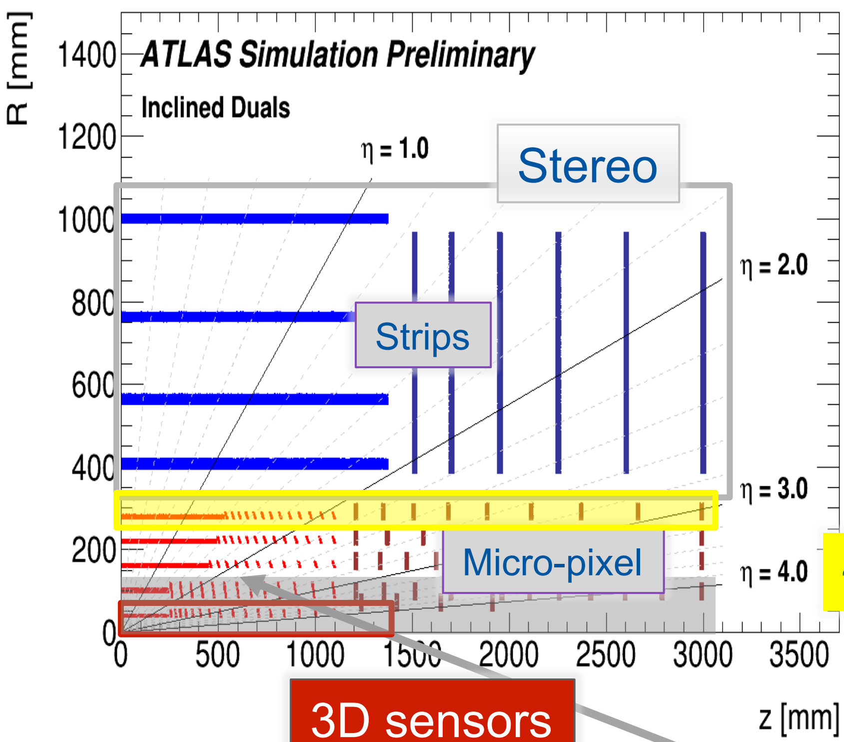
- Strip layers
  - NIEL ~ 10^{14} neq/cm^2
  - TID ~ 10Mrad
  - Larger area O(100m^2)
- Outer pixel layers
  - NIEL ~ 10^{15} neq/cm^2
  - TID ~ 50Mrad
  - Larger area O(10m^2)
- Inner layers
  - NIEL ~ 5x10^{15} to 10^{16} neq/cm^2
  - TID ~ 1Grad
  - Smaller area O(1m^2)

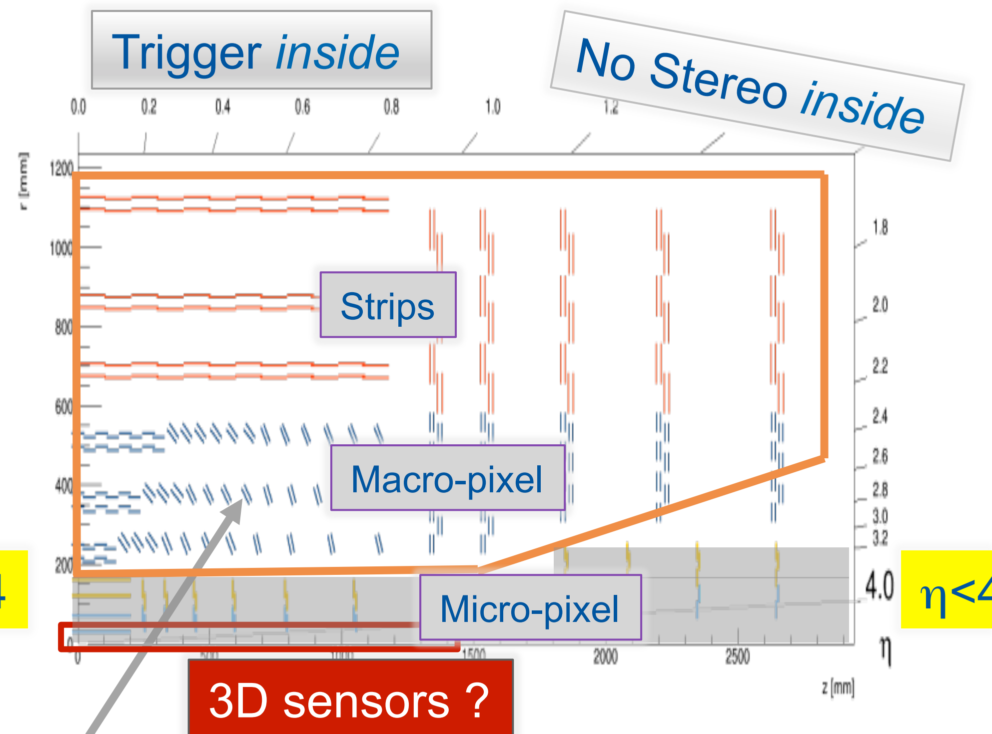
Future Trackers at ATLAS and CMS

Sensor active thickness 100 - 300 μm

CERN-LHCC-2017-021 ; ATLAS-TDR-030
Technical Design Report for the ATLAS Inner Tracker Pixel Detector
Einsweiler, Kevin; Pontecorvo, Ludovico
Collaboration, ATLAS
CERN. Geneva. The LHC experiments Committee ; LHCC
(technical design report)
k_einsweiler@lbl.gov on 23 Sep 2017
Detectors and Experimental Techniques
This is a placeholder for the final document.







Easy Extraction

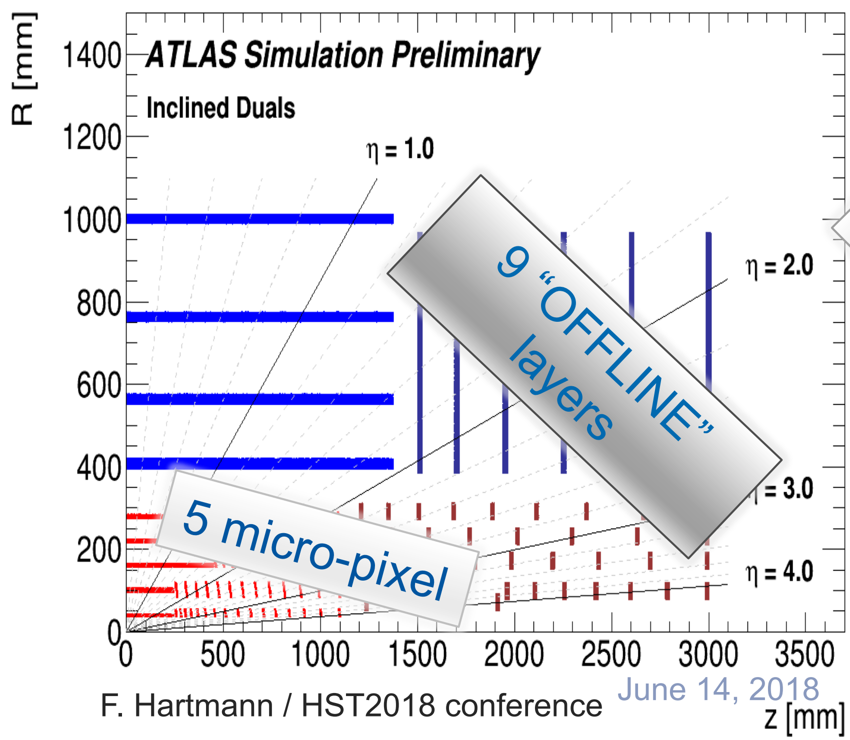
Inclined

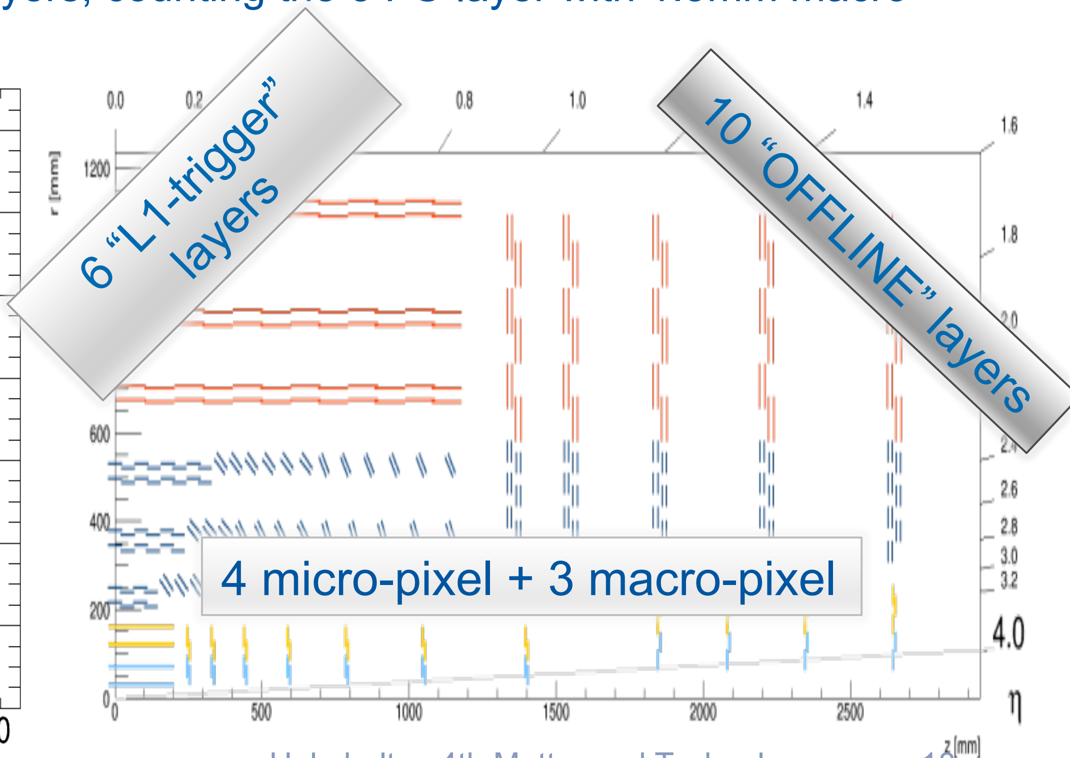
F. Hartmann / HST2018 conference

All n-in-p sensors *inside* with different thicknesses

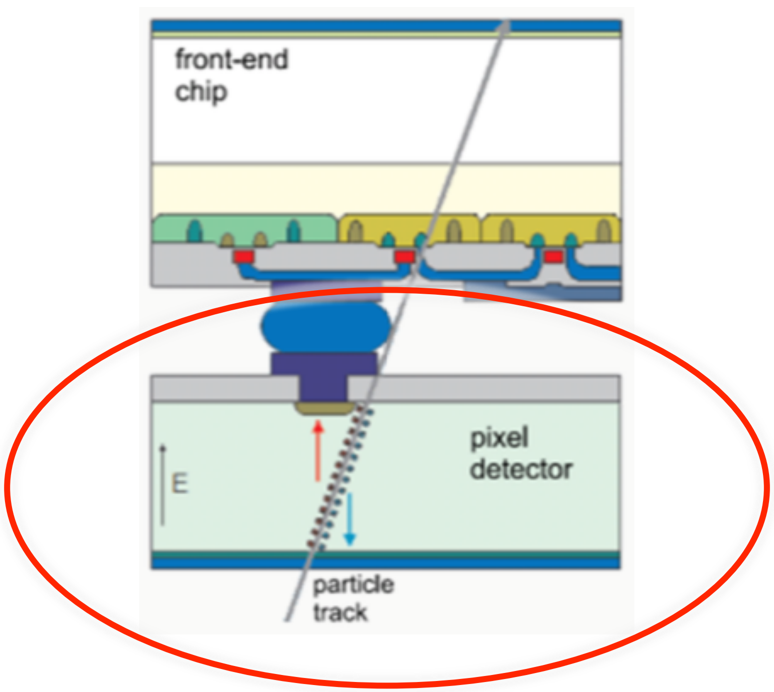
ATLAS and CMS Tracker upgrades

- Why has CMS 6 and ATLAS *only* 4 outer strip layers?
  - You need to count “**OFFLINE**” and “**L1-trigger**” layers separately!
  - With a fine granular pixel, only ***few*** outer layers are needed to measure p_T
    - ***Few*** = enough + redundancy -- 4 seems a perfect number even for an inner 4-layer pixel detector
- Why ATLAS has 5 pixel layers and CMS *only* 4?
  - CMS has in fact 7 ”pixel” layers, counting the 3 PS-layer with 1.5mm macro-pixels





Hybrid pixel sensors



Special sensor for e.g. extreme radiation hardness, timing

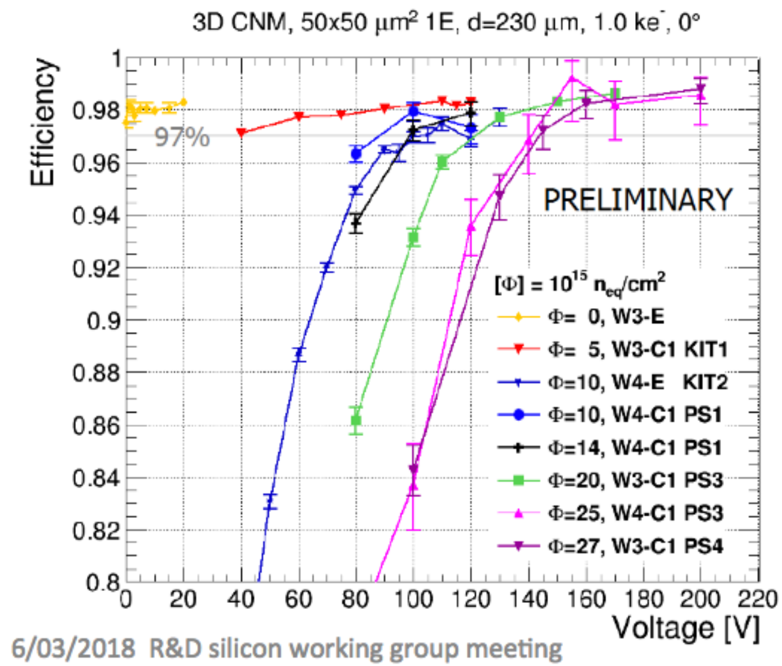
Dedicated FE-chip eg. for very high hit rates, digital functionality (memory, TDC,…)

- Front-end chip
  - Depending on application we need specialized FE-ASIC
  - Complexity of designs are driven by experimental needs
  - Increasing functionality on chip drives the development towards 65nm and smaller node size CMOS processes
- Sensor developments
  - For very high radiation and track density (e.g. 3D sensors, active edge planar)
  - Sensors for 4D tracking, i.e. spatial and time information (e.g. pixel sensors with trench electrodes)

Sensors for hybrid detectors

- 3D and Planar sensors developed to radiation hardness of >10^{16} n_{eq}/cm^2 for HL-LHC on 4” 6” wafer
  - Further development focuses on
  - Better lithography for smaller pixels on 3D
  - Optimizing active edge on planar
  - Move to 8” wafers
- Maybe in the future: special sensor for timing application in pixel sensors?

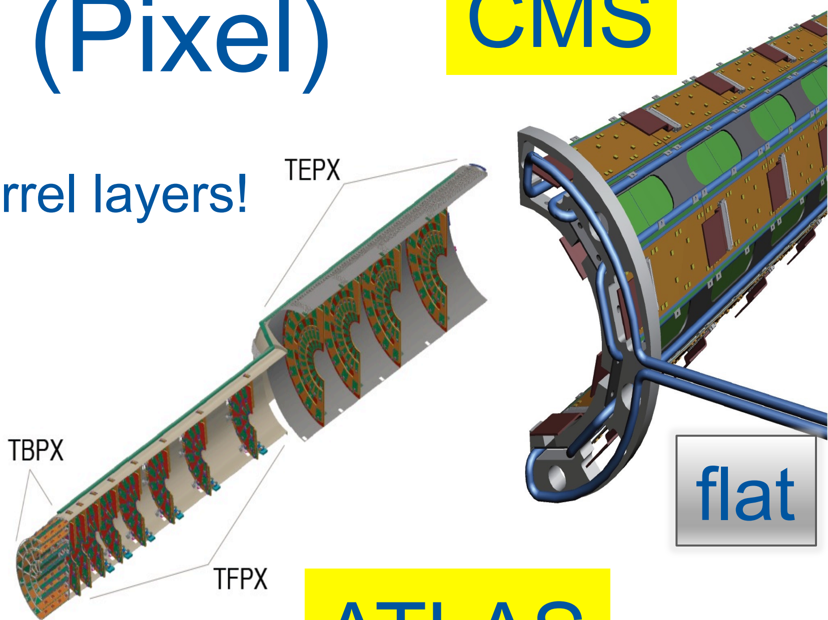
ATLAS Itk 3D



Next to the beam pipe (Pixel)

CMS

4 barrel layers!

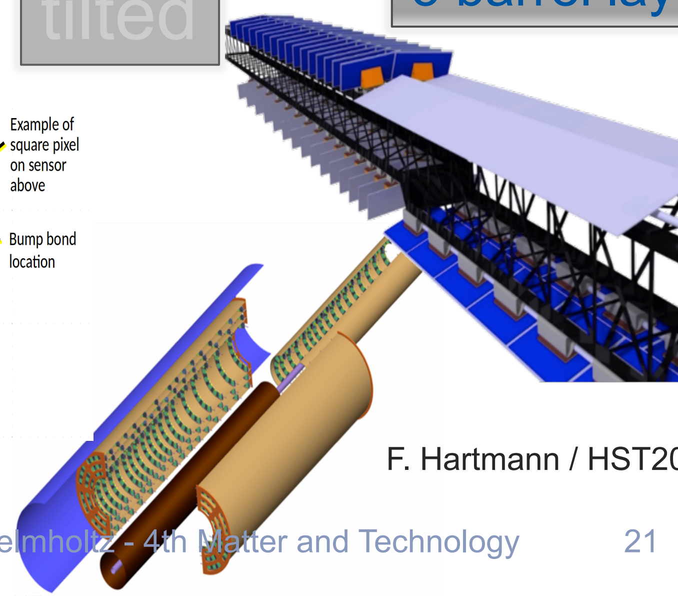


flat

ATLAS

tilted

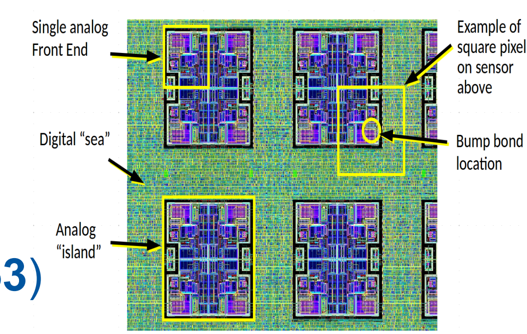
5 barrel layers



Many commonalities:

- "Classical" hybrid pixel detectors with bump-bonding
  - **THIN** Planar n-on-p or 3D detectors (inner layers)
    - Both need coating to prevent sparking
  - Common R&D on chip **RD53**A – 65nm TSMC
  - Modules: Doublets, Quads chip of singlets (ATLAS only)
- Common design of pixel FE-IC implemented with different matrix size
  - Sensor 50 x 50 μm ATLAS
  - Sensor 25x100 μm CMS

RD53

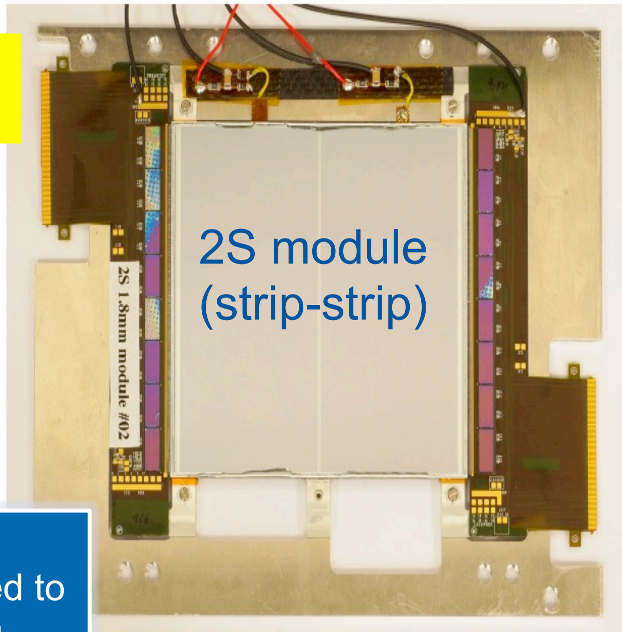


- Serial Powering (part of **RD53**)
- Both detectors up to η=4
- Both easily extractable (half-shells)
- **Surface: 2*CMS < 1*ATLAS**

F. Hartmann / HST2018

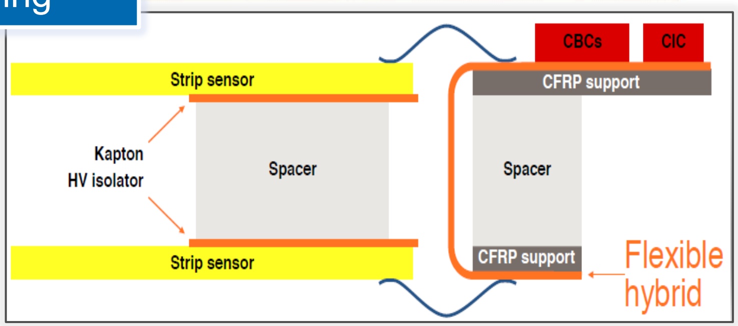
Away from the beam pipe (Strips)

CMS

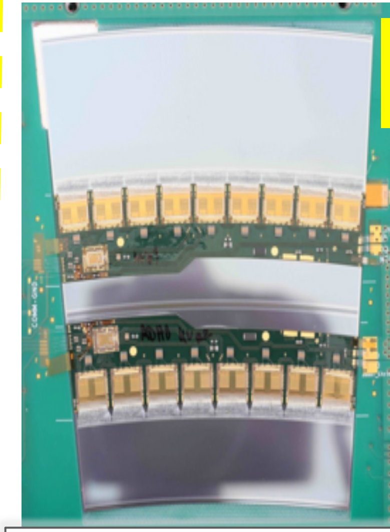


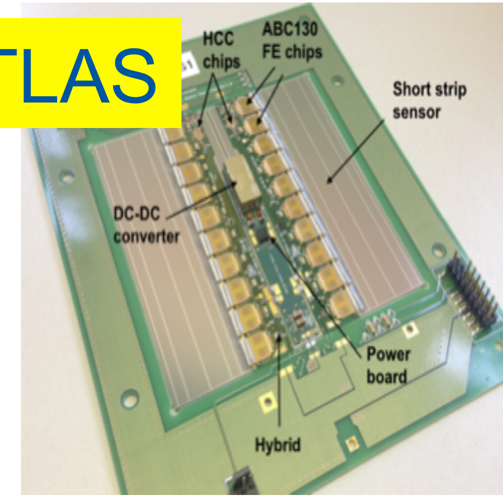
2S module (strip-strip)

Mostly screwed to cooling

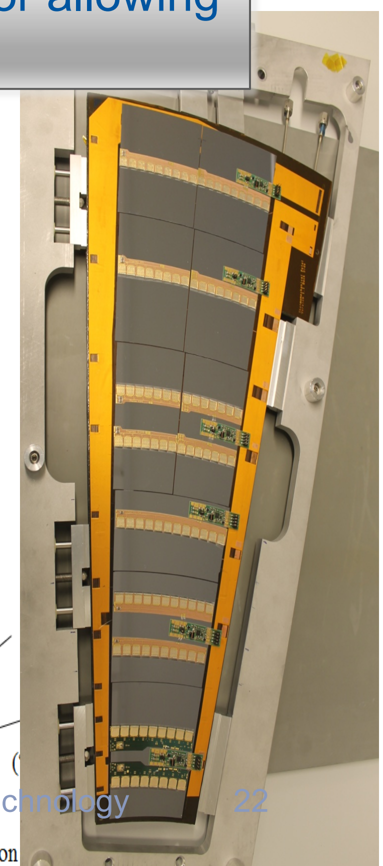


ATLAS

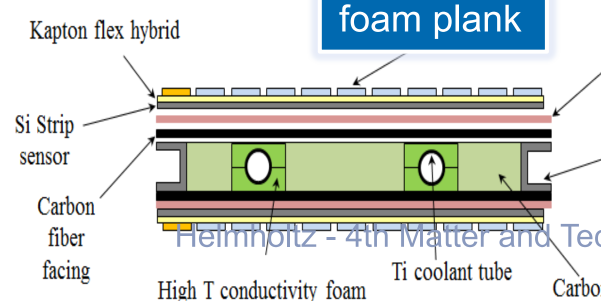




All Stereo – chips **on** sensor allowing different granularity



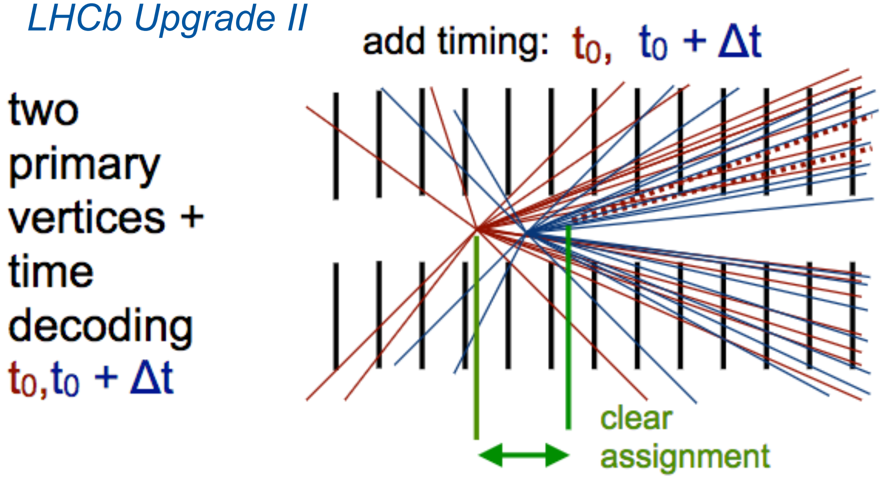
Glued to cooled CF/ foam plank



Functionality and integration

- E.g. combine tracking with timing

LHCb Upgrade II



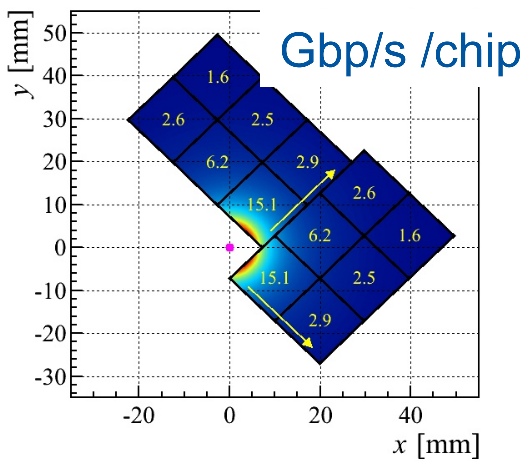
- FE-chip with very high data output (>20Gbps/ASIC) and <1ns time-resolution
- Requires high power and good cooling in a thin hybrid assembly

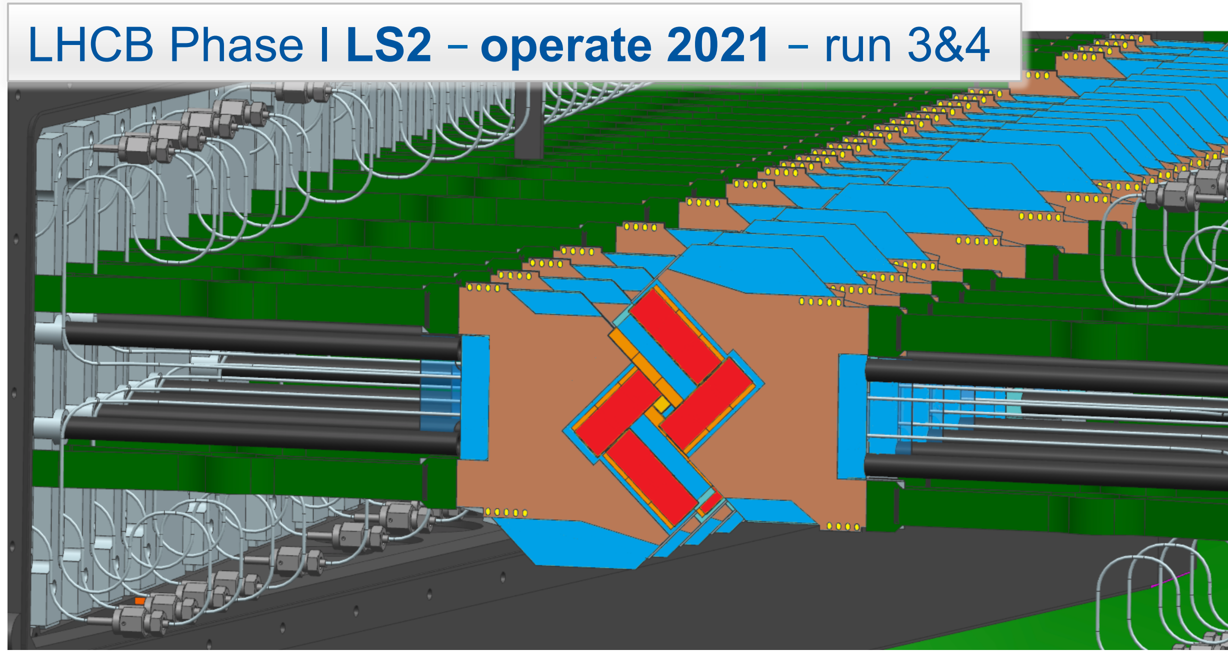
High density interconnection between sensor and dedicated FE-chip:

Essential R&D is also required forfuture integration between ICs

- 3D stacking of dies with different functionality
- Silicon interposer

LHCb VeloPix Upgrade for LS2





Each sensor (43mm x 15mm) bump-bonded to three VELOPIX ASICs

P. Collins / CERN

- All-pixel detector 55x55 μm^2 n-in-p 200 μm thick pixels sensor, readout with VELOPIX
  - Very high (8×10^{15} n_{eq}/cm^2 for 50 fb^{-1} until LS4) & non-uniform irradiation ($\sim r^{-2.1}$)
- Go closer: distance to beam 51 mm instead of 8.2 mm
- Sensors on CO_2 micro-channel cooling
- No hardware trigger
  - **Full 40 MHz readout** – software HLT 1 / 2 → 1-2 MHz / 20-100 kHz
  - 20 Gbit/s for central ASICs

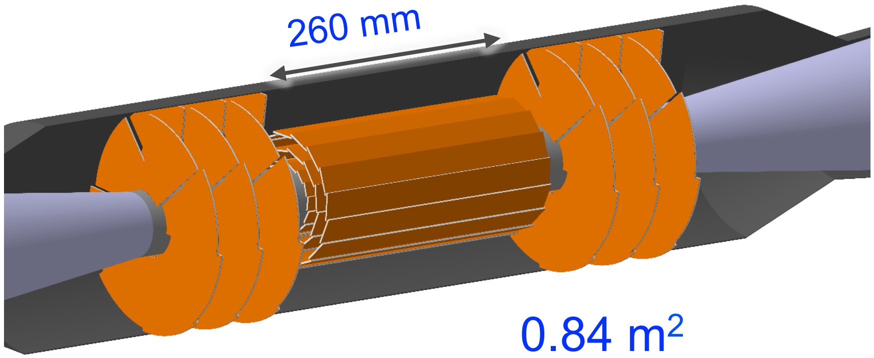
Silicon trackers for ee collisions (e.g. CLIC)

Vertex detector:
- efficient tagging of heavy quarks through precise determination of displaced vertices:
  → **good single point resolution**: σ_{SP}~3 µm
    → small pixels <~25x25 µm^2, analog readout
  → **low material budget**: ≲ 0.2% X_0 / layer
    → low-power ASICs + air cooling (~50 mW/cm^2)

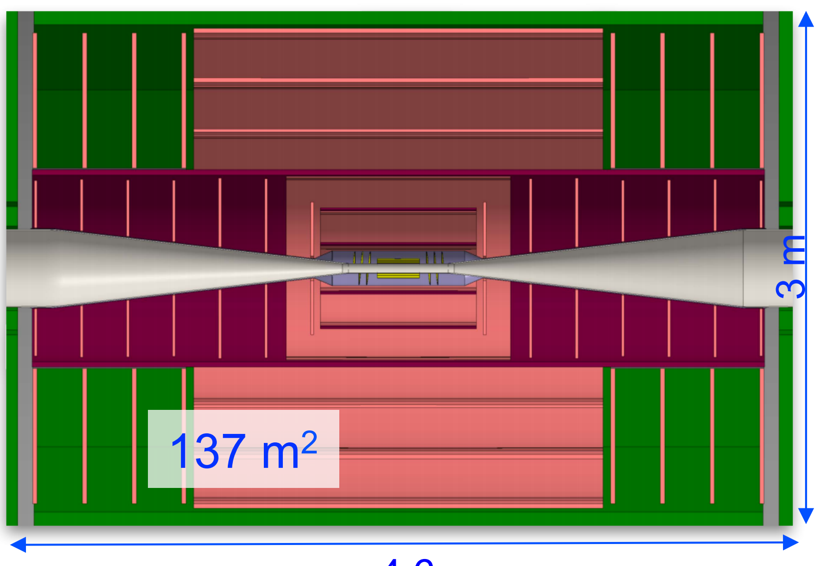
Tracker:
- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  → 7 µm single-point resolution (~30-50 µm pitch in Rφ)
  → **many layers, large outer radius (~140 m² surface)**
  → ~1-2% X0 per layer
    → low-mass supports + services

Both:
- 20 ms gaps between bunch trains
  → trigger-less readout, pulsed powering
- few % maximum occupancy from beam backgrounds
  → sets inner radius and limits cell sizes
  → **time stamping with ~5 ns accuracy**
    → **depleted sensors (high resistivity / high voltage)**
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm^2/y
  - TID: < 1 kGy / year

Vertex-detector simulation geometry



Tracker simulation geometry

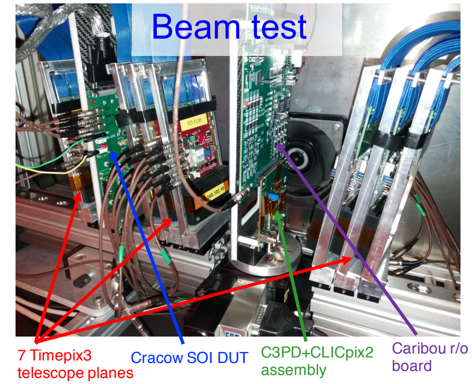


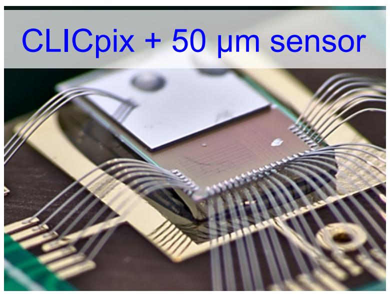
D. Dannheim / CERN

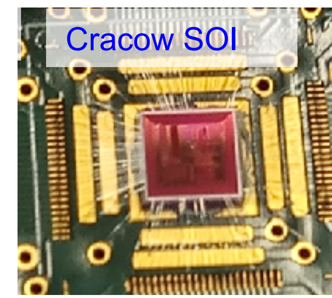
CLIC pixel-detector technology R&D

Sensor + readout technologies

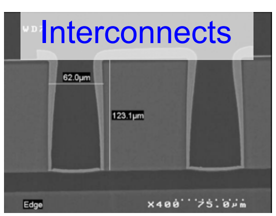
Sensor + readout technology	Currently considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker

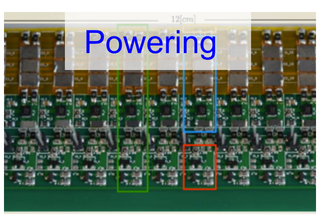


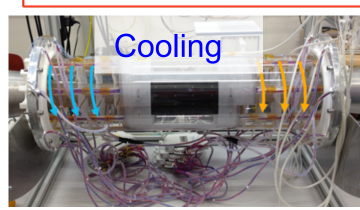


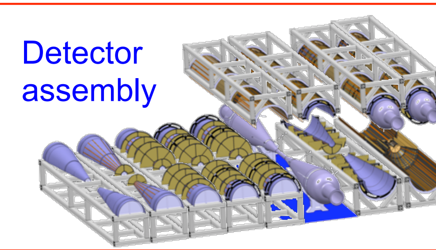


Detector integration studies









- Challenging requirements lead to extensive detector R&D program
- ~10 institutes active in vertex/tracker R&D
- Collaboration with ATLAS, ALICE, LHCb, RD53, AIDA-2020

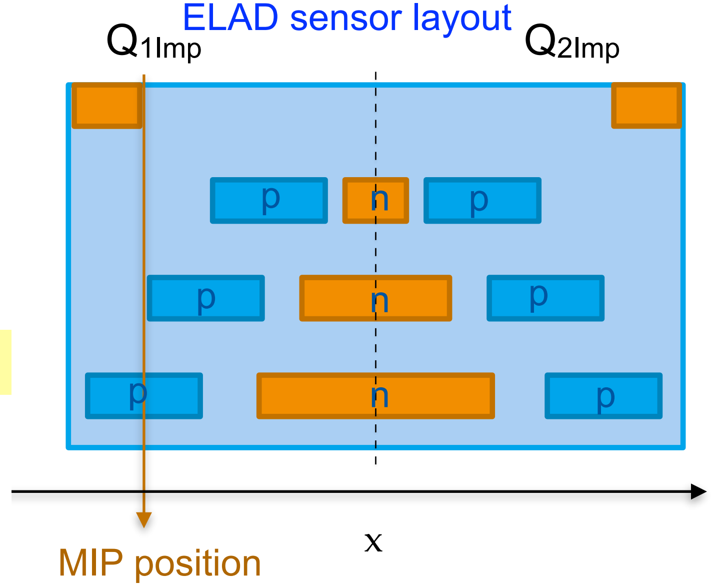
D. Dannheim / CERN

ELAD sensors

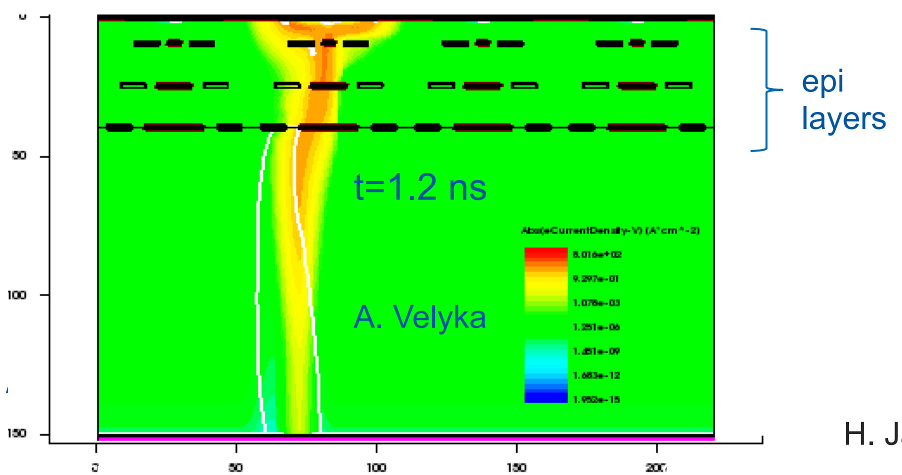
- Position resolution in very thin sensors so far limited to ~pixel pitch / √12 (almost no charge sharing)
- New sensor concept for enhanced charge sharing **E**nhanced **LA**teral **D**rift sensors (ELAD), H. Jansen (DESY/PIER)
- Development supported by Helmholtz
- Deep implantations to alter the electric field
  → lateral spread of charges during drift, cluster size ~2
  → improved resolution for same pitch
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- Ongoing TCAD simulations:
  - Implantation process
  - Sensor performance for MIPs
- First production in 2018: generic test structures, strips and test sensors with Timepix footprint (55 µm pitch)

Patent DE102015116270A1

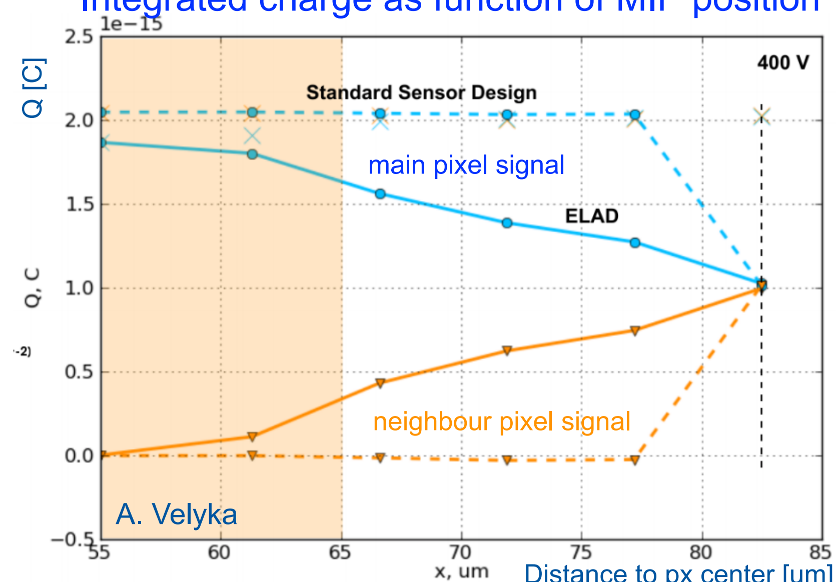
ELAD sensor layout



TCAD simulation of current from MIP



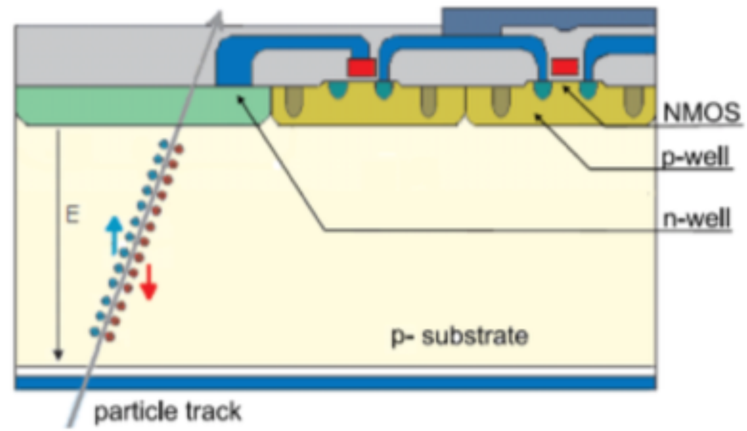
Integrated charge as function of MIP position



H. Jansen / DESY

Monolithic Silicon Pixel Detectors

Depleted Monolithic Active Pixel Sensors

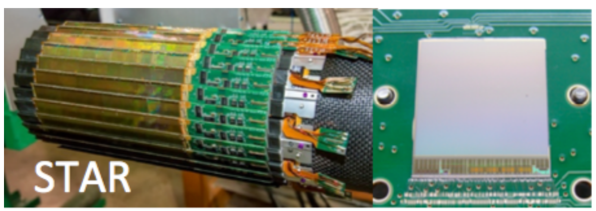


- Depletion is key for fast signal response and radiation hardness
- Thin detector with high granularity

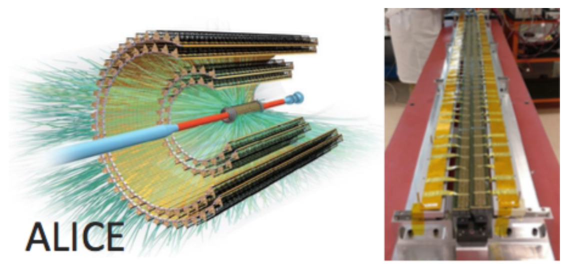
- FE electronics is integrated in sensor and produced on commercial CMOS processes
- Allows very thin sensors to achieve ultimate low mass trackers (0.3% X/X_0)
- High volume and large wafers (200mm) reduces detector costs and allows large area pixel detectors
- Saves costs of bump-bonding (cost driver for hybrid silicon detector systems

DMAPS/CMOS for Future Trackers

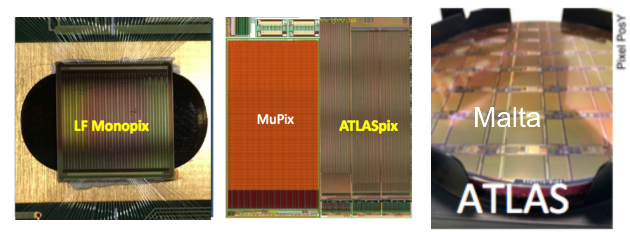
	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm^2]	0.4	10	<0.3	100-200	2000	200-20000



Ultimate Sensor



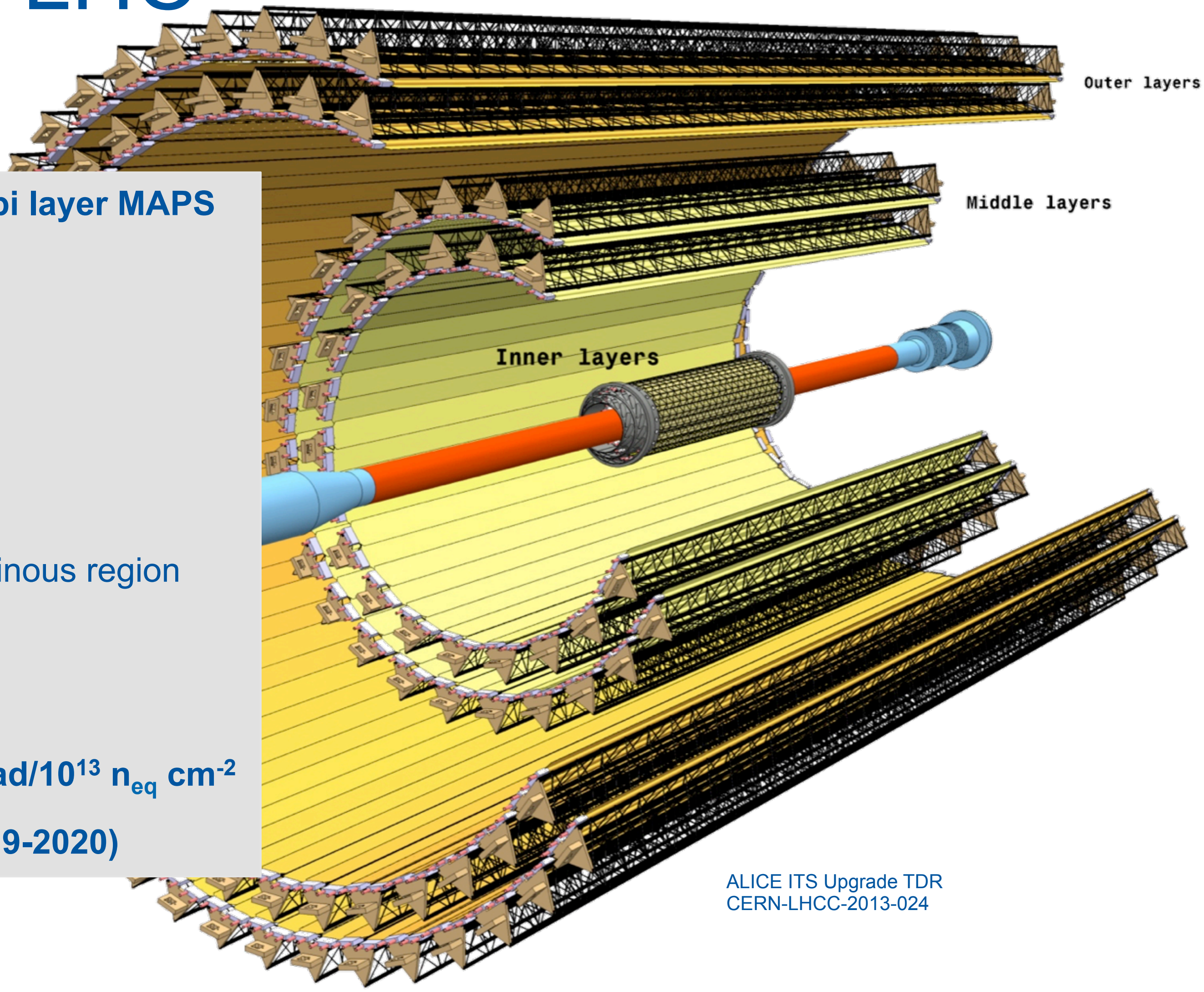
Alpide Sensor



Monopix & AtlasPix & Malta Sensor

- Advances in commercial CMOS technologies combined with dedicated designs allowed significant progress from STAR to ALICE to ATLAS in areas like radiation hardness, response time, hit rates
- **Strong interest for R&D to fully exploit potential of MAPS in future Trackers**
  - **High granularity, Low material budget and power, Large area at reduced cost (cf hybrid)**
  - **CMOS foundries offer substantial processing power to enable significant performance gains**

ALICE Inner Tracking System Upgrade at LHC



Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

~ 10 m^2

|η|<1.22 over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Installation during LS2 (2019-2020)

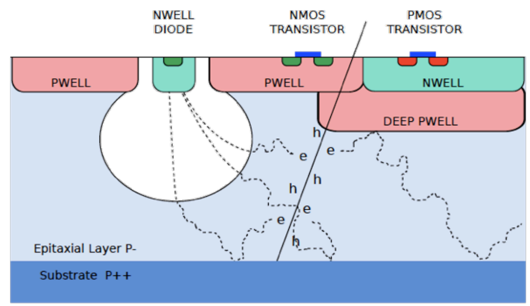
ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

ALICE ITS Upgrade: High resistivity epi layer MAPS

N-well collection electrode in high resistivity epitaxial layer (>1kohmcm)

TowerJazz 0.18 um CMOS Imaging Process

- Special deep p-well for full CMOS within matrix (based on experience of RAL)
- 6 metal layers -> suited for high density, low power circuitry
- Small n-well diode (2-3 μm diameter), ~ 100 times smaller than pixel → low capacitance
- 3 nm gate oxide -> TID tolerant
- Epi thicknesses 20-40 μm tested → higher cluster signal



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

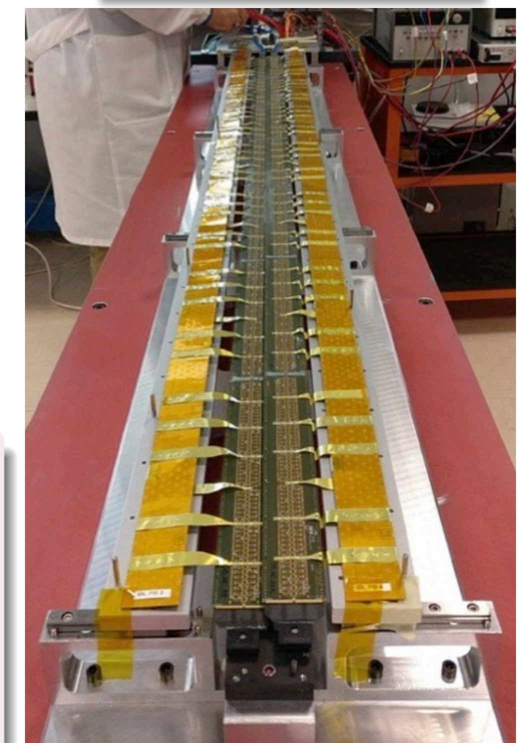
NWELL diode output signal:

$$V \sim Q/C$$

- Increase charge collected by the central pixel
- Minimize capacitance:
  - diode surface
  - depletion volume

→ (reverse substrate) bias

In production

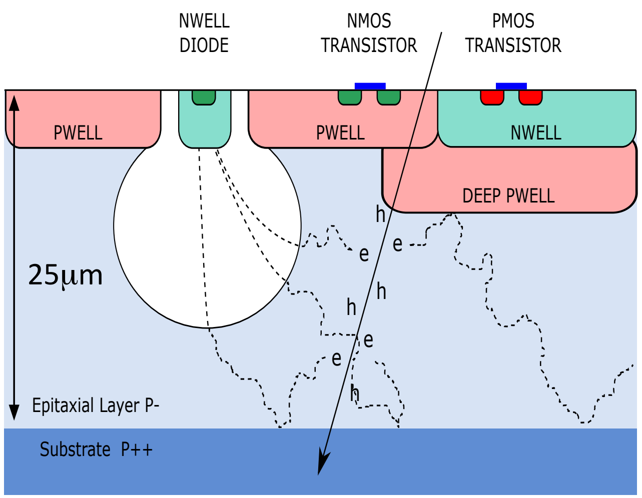


L. Musa, P. Riedler / CERN

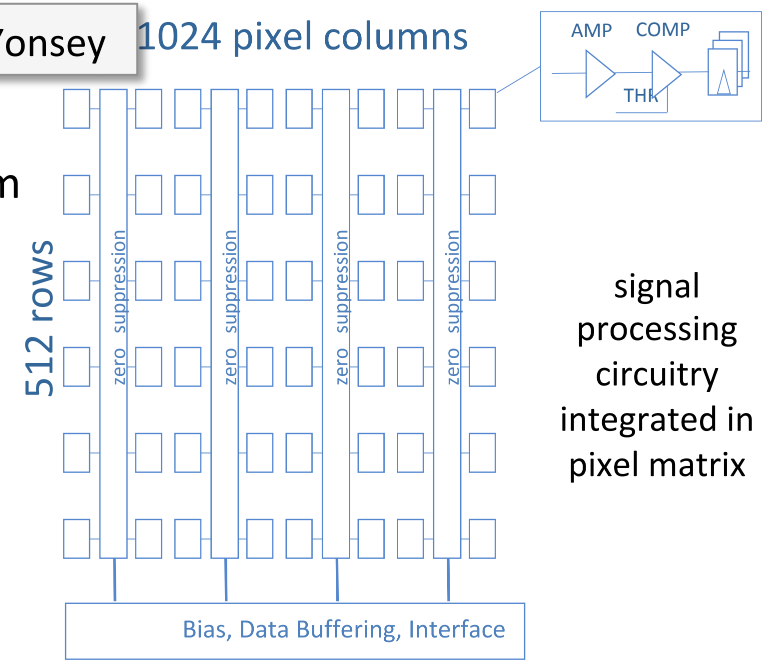
ALICE ITS TDR

ALPIDE – A novel CMOS Pixel Sensors for the ALICE Upgrade

R&D: CERN, CCNU, IPHC, INFN, IRFU, NIKHEF, RAL, Yonsey

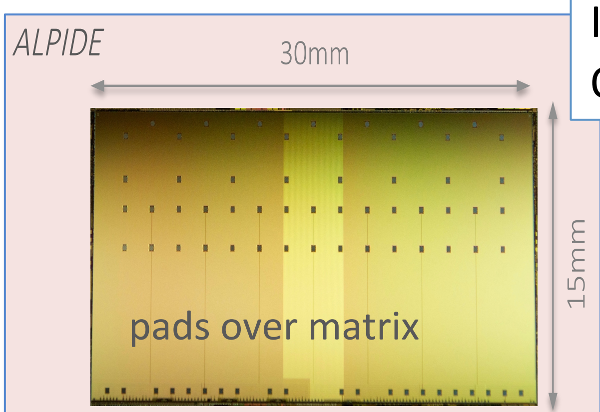


CMOS 180nm



signal processing circuitry integrated in pixel matrix

pixel capacitance 2.5 fF (@ V_{bb} = -3 V) ➪ MIP signal ~ 50mV



IB: 50μm thick
OB: 100μm thick

130,000 pixels / cm^2 27x29x25 μm^3

Charge collection time <30ns (V_{bb} = -3V)

spatial resolution ~ 5 μm

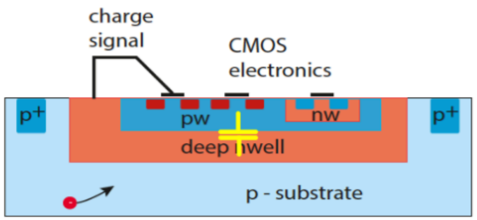
max particle rate ~ 100 MHz / cm^2

fake-hit rate: < 10^{-9} pixel / event

Different CMOS sensor designs

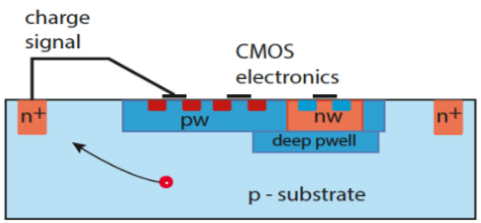
- Purse different design approaches for optimal performance

- Large electrodes



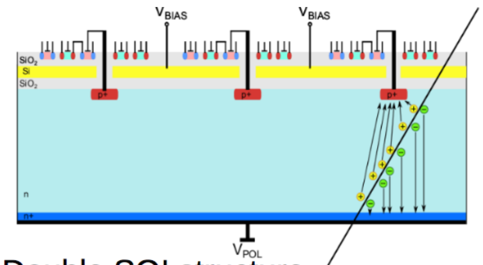
- Electronics in collection well
- No or little low field regions
- Short drift path for high radiation hardness
- Large(r) sensor capacitance (dpw/dnw) ->higher noise and slower @ given pwr
- Potential cross talk between digital and analog section

- Small electrodes



- Electronics outside collection well
- Small capacitance for high SNR and fast signals
- Separate analog and digital electronics
- Large drift path -> need process modification to usual CMOS processes for radiation hardness

- "Burried" electrodes (SOI)



- Electronics and sensor in separate layer
- Can use thick or thin high resistivity material and HV (>200V)
- Special design/ processing to overcome radiation induced charge up of oxides

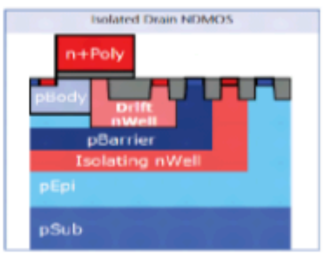
Radiation hard CMOS sensor

$$d \sim \sqrt{\rho \cdot V}$$

I. Peric, NIM A582 (2007) 876-885

1 "High" Voltage add-ons to apply 50 – 200 V bias

2 "High" Resistivity Substrate Wafers (100 Ωcm – kΩ cm)

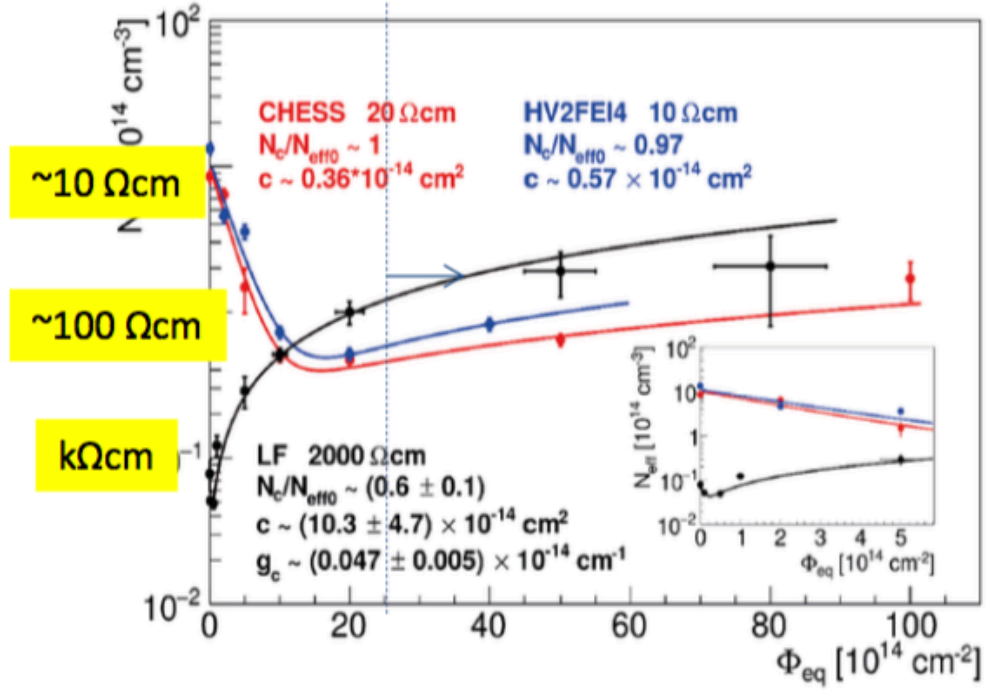


from: www.xfab.com

3 Multiple (3-4) nested wells (for shielding and full CMOS)

4 Backside Processing (for thinning and back bias contact)

Effective resistivity after HL-LHC irradiation ~ O(100Ωcm)



I. Mandic et al., JINST 12 (2017) no.02, P02021

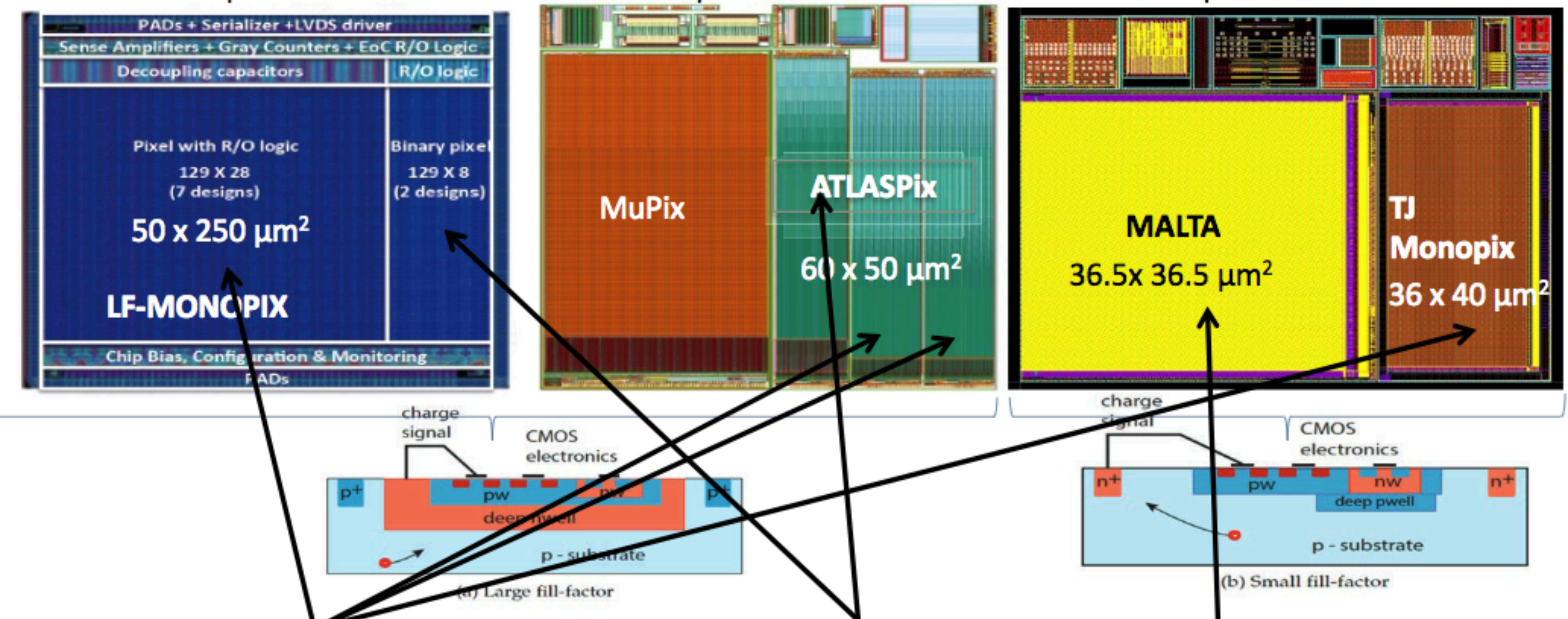
CMOS sensor developments for ATLAS

- Collaboration of 25 institutes
- Targeted towards outermost ITK pixel layer

LFoundry 150 nm
substrate ρ > 2 kΩcm

ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

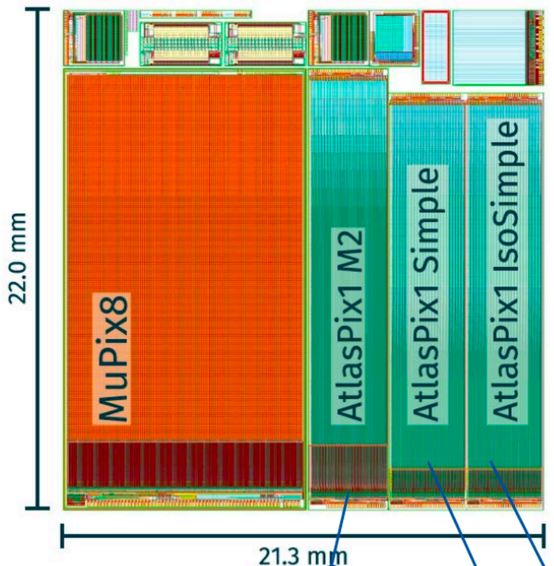
TowerJazz 180 nm epitaxial (25 μm)
substrate ρ > kΩ cm

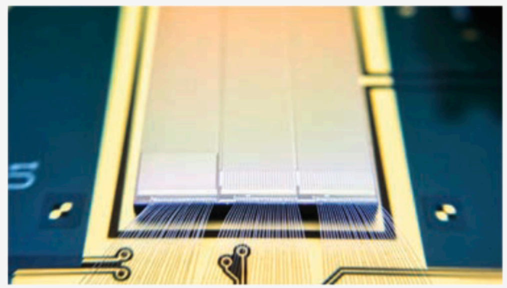


column drain (conservative) - parallel pixel to buffer - asynchronous

HVCMOS sensors (AMS 180nm)

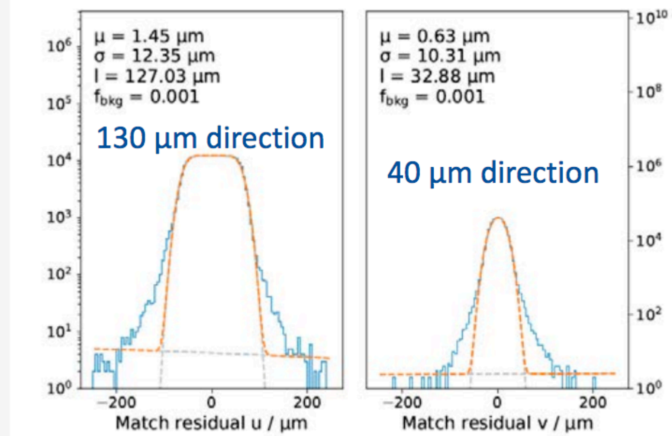
Developments in context of ATLAS and μ3e experiment





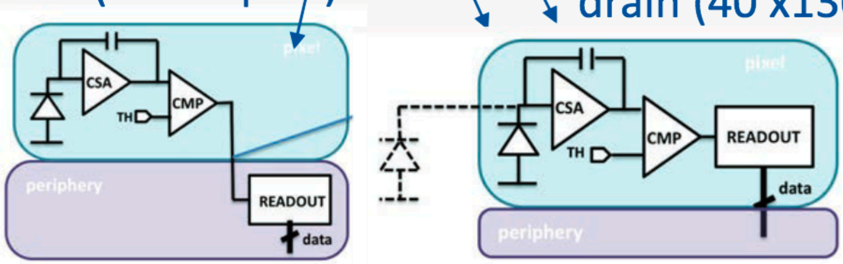
unirradiated

Resistivity 80 Ωcm & 200 Ωcm



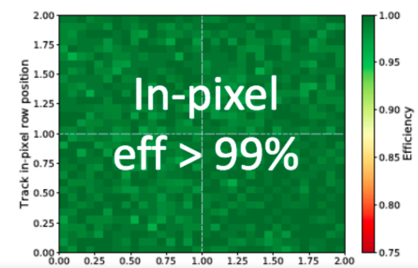
PPtB (60x50 μm^2)

Column drain (40 x130 μm^2)



M. Kiehn
ATLAS UW 4/18

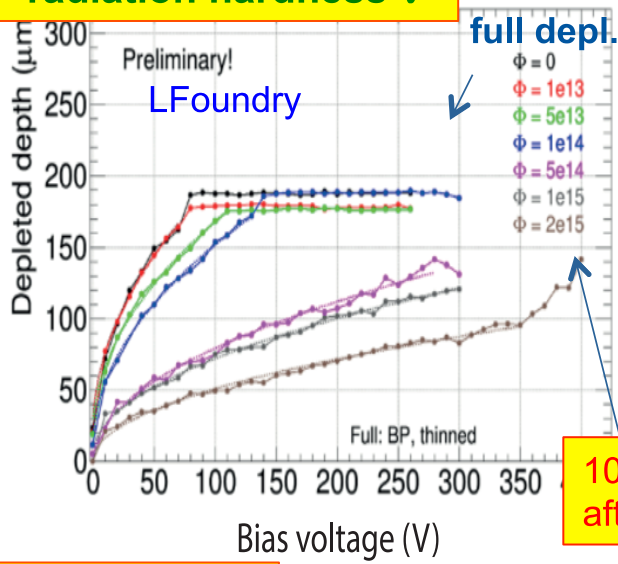
65V HV bias
Threshold 840 mV



See I. Peric's talk Wednesday "Integrated sensors in particle physics"

Preliminary results with large electrodes

- **radiation hardness ✓**

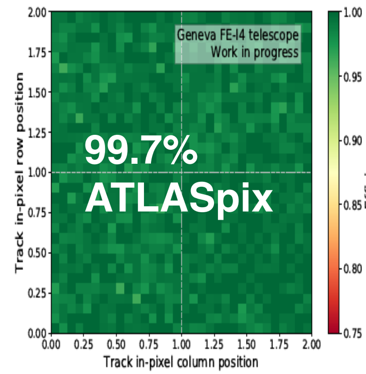


full depl.

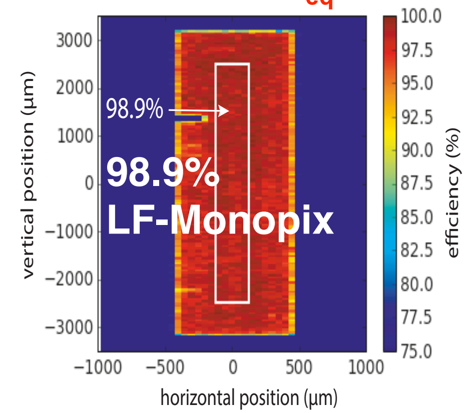
100 µm after $2x10^{15}$

- **efficiency ✓**

before irrad



after 10^{15} n_{eq} cm^{-2}

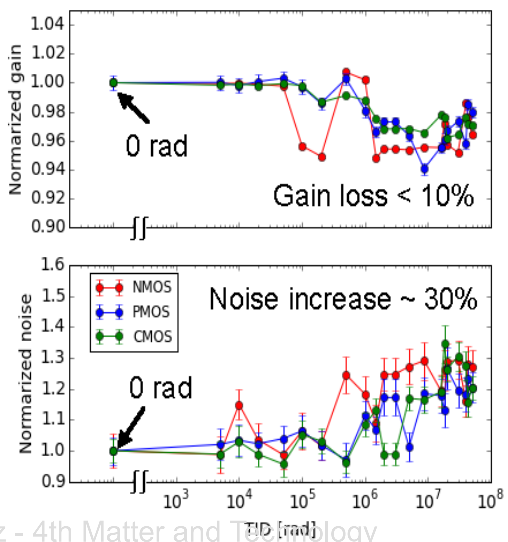


- **TID 1 MGy ✓**

LFoundry

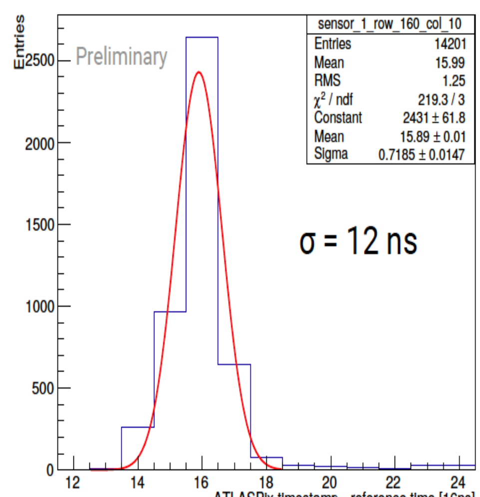
gain

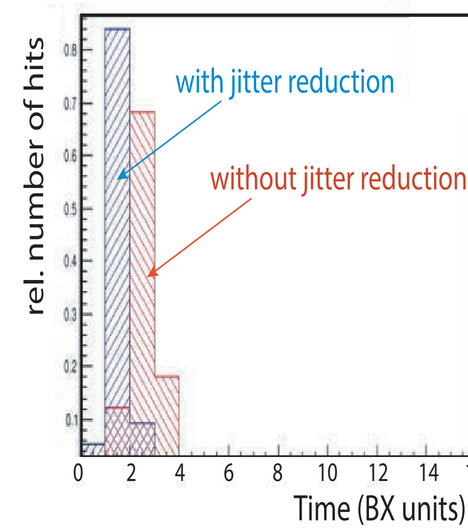
noise



- **timing …**

AMS

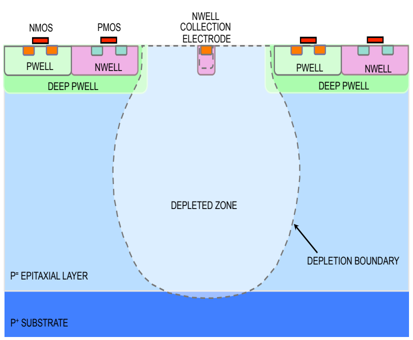




Novel CMOS Pixel Sensors with small electrodes

As R&D for the ALICE upgrade, CERN has developed in collaboration with Tower Semiconductor a process modification that allows full depletion of the high resistivity silicon layer

The process modification requires a single additional process mask with no changes on the sensor and circuit layout



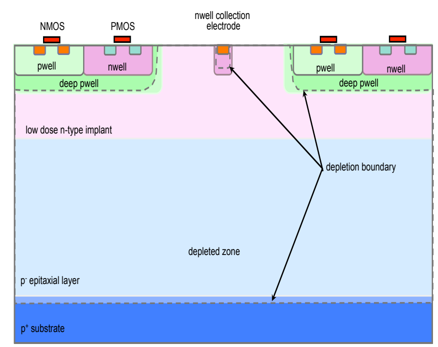
Vertical full depletion

Lateral partial depletion

Collection time < 30ns (V_{bb}=-3V)

Suitable for up to 10^{14} n/cm^2

Foundry Standard Process



Epi-layer fully depleted

Operational at 10^{15} n/cm^2

Modified process CERN/Tower

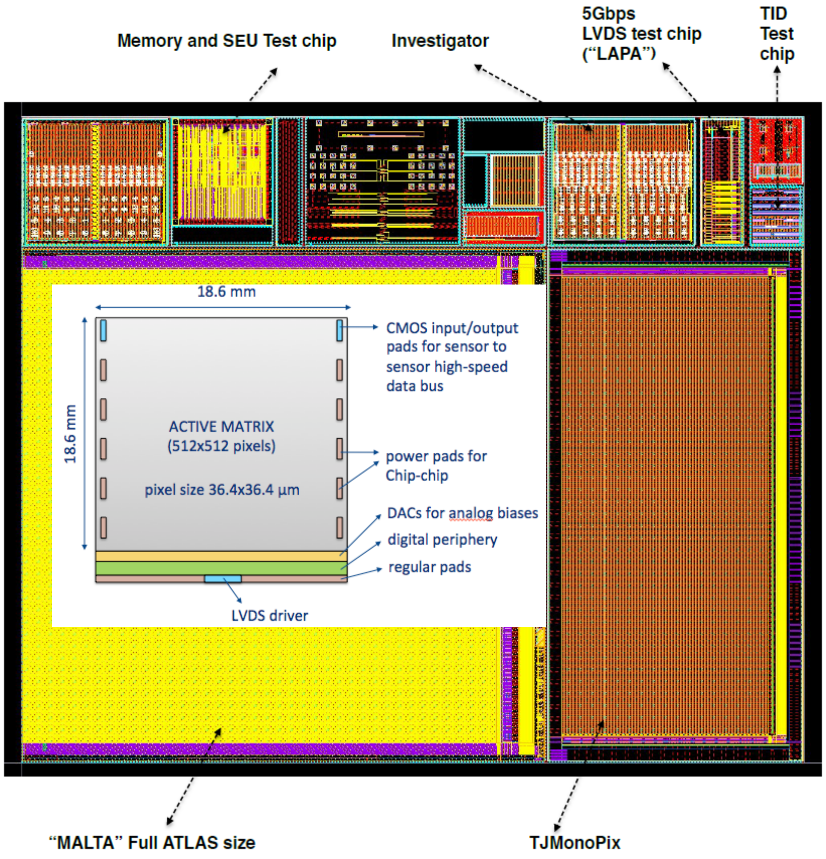
W. Snoeys / CERN

- Explore sensor designs with small electrode to minimize pixel capacitance
- Small capacitance best for low noise & low power operation
- Radiation hardness requirements for HL-LHC requires dedicated optimization of implants under deep p-well for full depletion and to minimize charge loss after irradation -> ongoing RD in ATLAS

MALTA & MonoPix – Novel depleted CMOS sensors with small electrodes

R&D: CERN, Uni. Bonn,

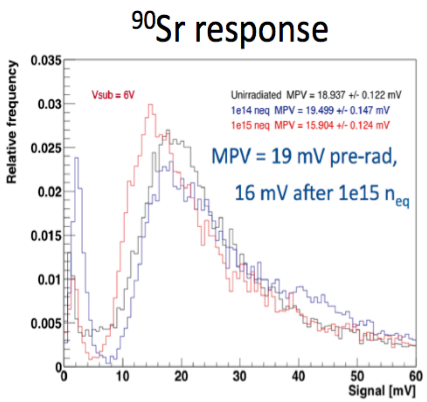
- **Monolithic pixel prototype sensor for the outer layers of the ATLAS Itk Pixel outer layer**
- **Full-scale demonstrators** with different readout architectures and optimized analog performance
  - MALTA: 20x22 mm (full size)
  - MonoPix : 20x10 mm (half size)
- **The ATLAS "MALTA" and "MonoPix" chip** for **high hit rate suitable for HL-LHC pp-collisions**
  - **Radiation hard to >10^{15} n/cm^2**
  - **Shaping time 25ns** (BC = 25ns)
  - **MALTA: Novel asynchronous readout** architecture for high hit rates and fast signal response
  - **MonoPix: Synchronous Column drain** readout architecture

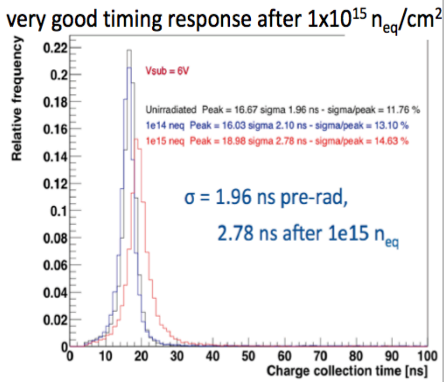


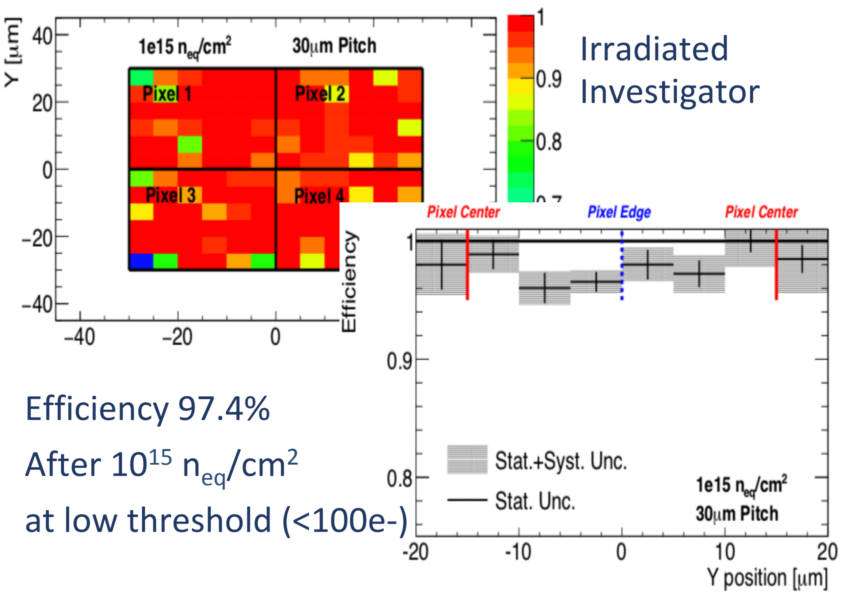
Sensors received back in Jan / both sensors functional and currently under test

Preliminary results with small electrodes

2017 Investigator measurements







Irradiated Investigator

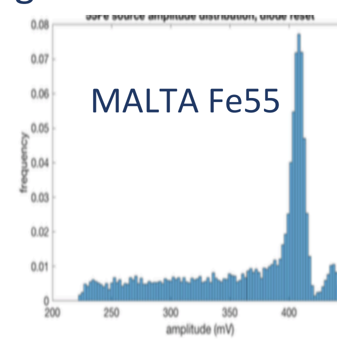
Efficiency 97.4%

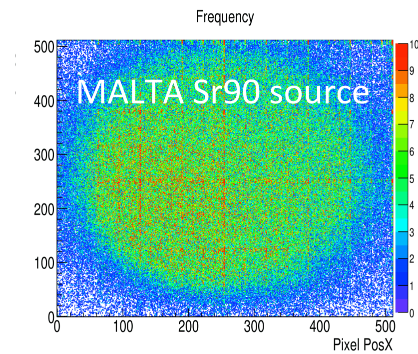
After 10^{15} n_{eq}/cm^2

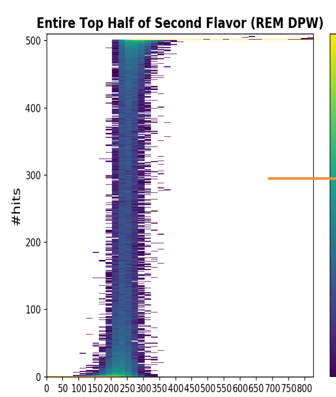
at low threshold (<100e-)

2018 MALTA & TJMonoPix measurements

- Both chips work – same FE design, different readout architecture
- Tests ongoing (lab, beam tests, irradiations) show excellent ENC ~ 8e- and threshold dispersion ~ 15 e-
- Irradiation tests ongoing



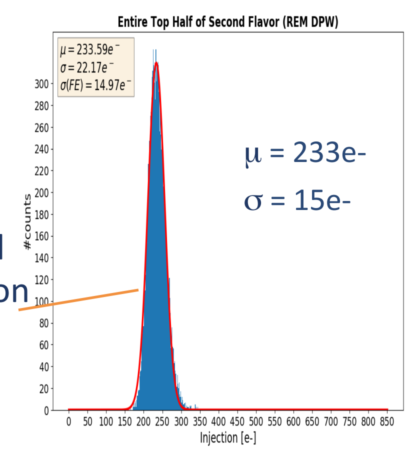




MonoPix:

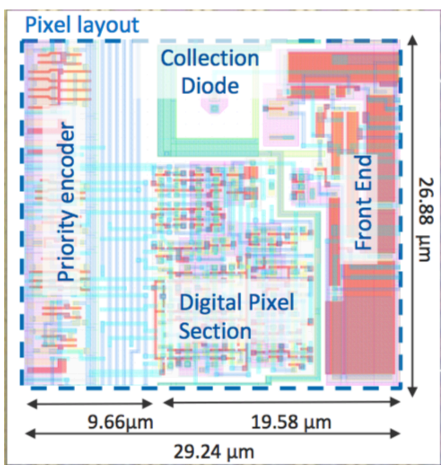
S-curves

Threshold distribution

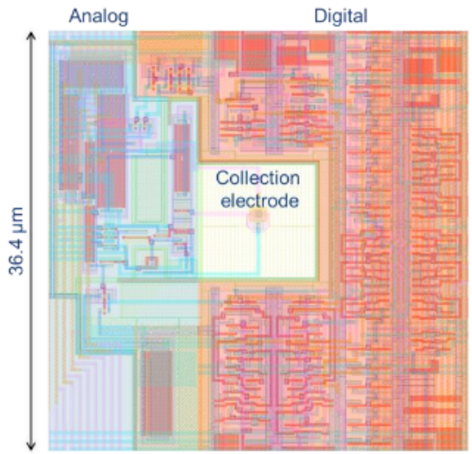


Enhanced Performance

- Achieve better spatial resolution, fast timing and high rate capability through higher integration density for future trackers



Alpide pixel



MALTA pixel

Now in 0.18 µm

Q/C > ~ 0.25 fC / 5 fF = 50 mV

- ALPIDE: 40 nW/pixel (analog)
- MALTA/Monopix: 1 µW /pixel (25ns)
- Analog power in matrix dominant

Pixel pitch ≈ sensitive layer thickness ≈ 30 µm

- Position resolution ~ 5 µm

Matrix hit rate capability:

- MALTA matrix > 100 Mhit/mm^2/s (but cannot cope at periphery)

Deeper submicron

Q/C >>

- Analog power will go close to zero

Pixel pitch ≈ sensitive layer thickness ≈ 5-10 µm

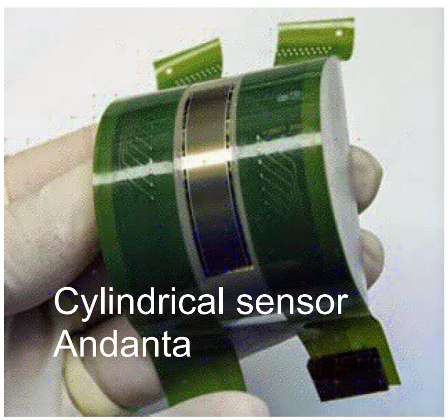
- Position resolution ~ 1-2 µm

Matrix hit rate capability:

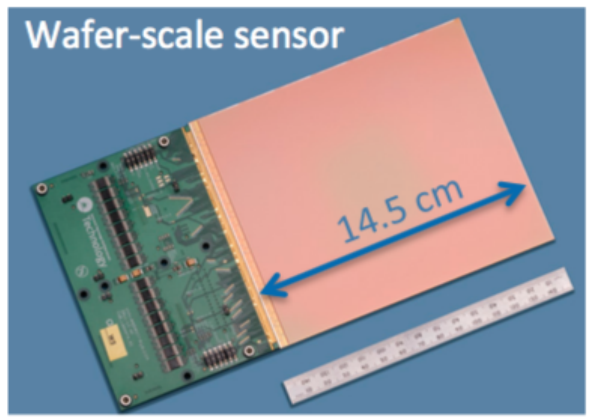
- 10's of GHz/mm^2 (but need to cope at periphery)

Large sensors & systems

- Developed **"stitched" designs for large sensors and special geometries**
  - Chain sensors for large area trackers and large acceptance
  - Exploit mechanical flexibility of thin sensors in cylindrical or spherical geometry



Cylindrically Curved CCD (Convex)



- CMOS sensor key advantage is large volume production on 200/300mm wafers
- Improve ratio between chip and total detector area through stitching

Explore new solutions for data aggregation and transmission for high data rates

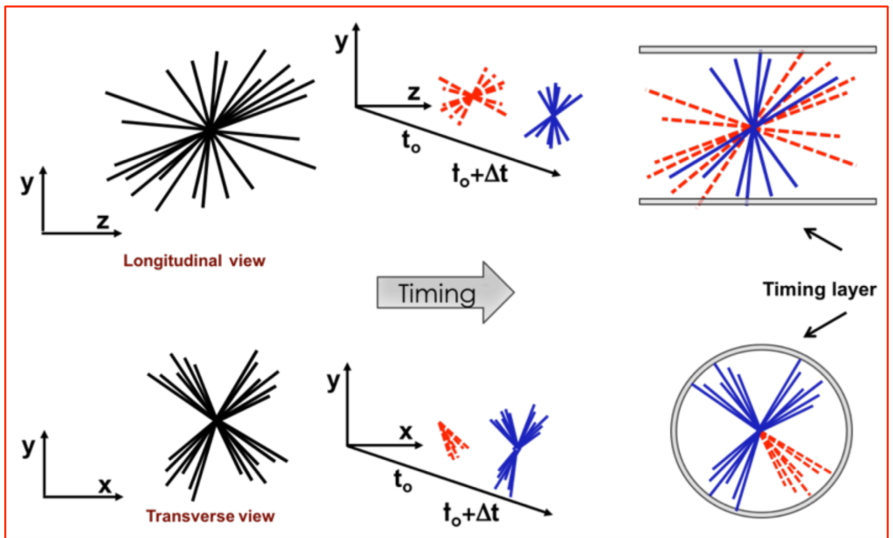
E.g. demonstrator module with sensor to sensor interconnection and high-speed data readout via photonics chip (WP on data transmission)

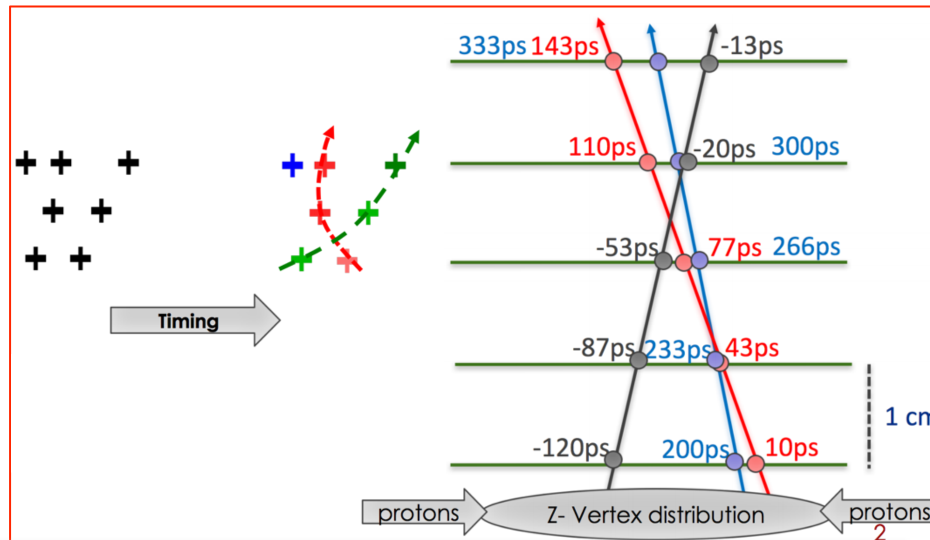
Timing for tracking

Need sub-nanosecond track time to suppress background in environments with large pile-up (HL-LHC, FCC) → **4D tracking**

Separate timing layers with coarser granularity
→ timing for reconstructed tracks
(e.g. HL-LHC upgrades **~30 ps**)

Timing within pixel layers
→ time info for pat rec
(e.g. LHCb Upgrade II **20-200 ps,** depending on pixel size, radiation)

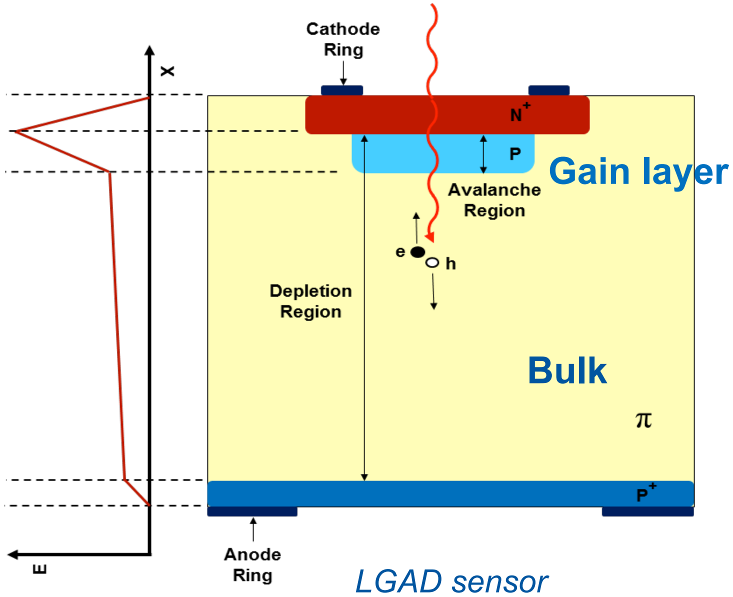




See N. Cartiglia's talk Tuesday "Ultrafast timing detectors in particle physics"

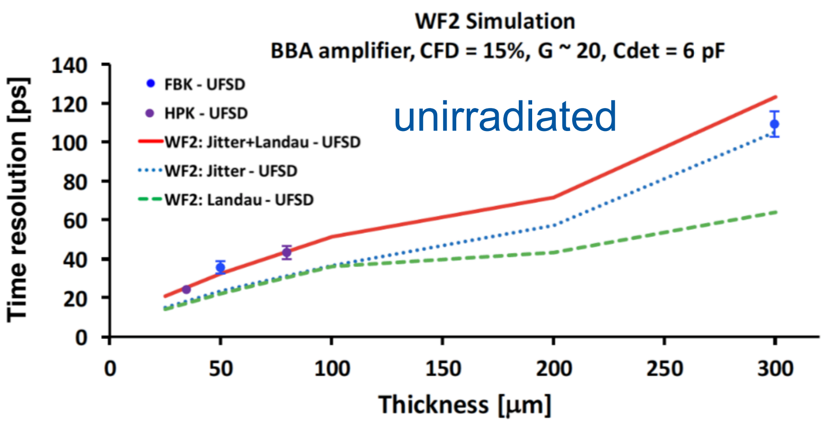
→ Trade-off between time resolution and pixel size / layer thickness
→ FCChh needs track timing at **5 ps** up to **6×10^{17} n_{eq}/cm^2** fluences

LGAD timing sensors



LGAD sensor

N. Cartiglia, H. Sadrozinski



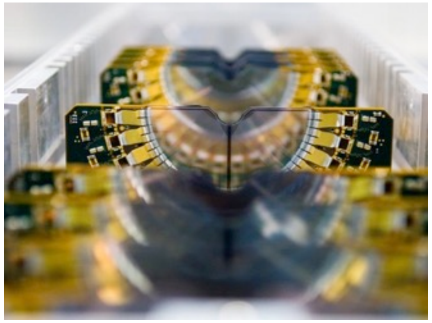
Low Gain Avalanche Detectors (LGAD):
Multiplication of charges (~10-100x) in thin gain layer → fast rise time, increased S/N

- Several vendors: CNM, FBK, HPK
- Reached **~30 ps** for few mm^2 size sensors → considered for HL-ATLAS/CMS/LHCb **timing layers**
- Limiting factors for time resolution:
  - Weighting **field uniformity** → favors larger pixels
  - **Radiation effects** → ok up to ~10^{15}, mitigation measures under study for higher fluences
  - **r/o electronics + clock distribution** → IC work package
- R&D to achieve radiation hardness
  - Variation in doping to limit gain loss after irradiation
- RD for **larger fill factors** (currently ~70-00 μm inactive region between pixels):

F. Carnesecchi / Frontier Detectors – Elba 2018

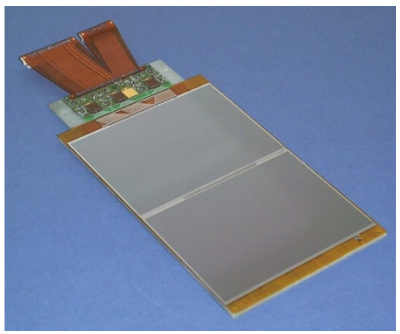
From sensors to modules to silicon detector systems

Module Construction & Interconnect

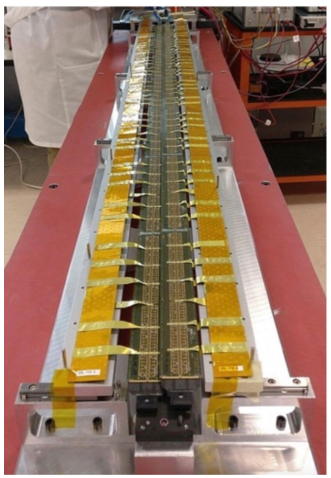


LHCb VELO

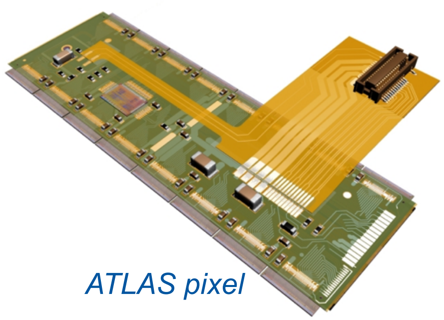
- Silicon modules are complex structures composed of many components and usually are installed in areas with limited access → **new module designs**
- Optimising each component, and validating module concepts is key to a successful operation → **reliability**



CMS Tracker



ALICE ITS stave



ATLAS pixel

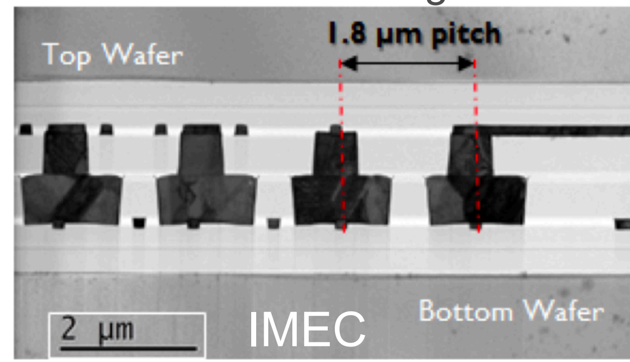
- **Module building and interconnection** is used in all projects on various scales: numbers, complexity, environment,…
- **Many different components** involved in this step (sensors, interconnects, ASICS, PCB, support, etc.)
- **Mostly done "in house" but upcoming projects are also investigating outsourcing** to industry

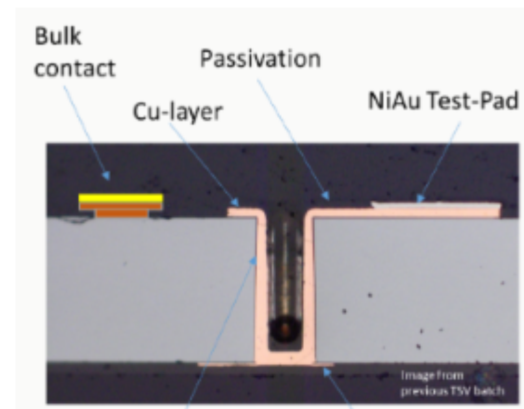
Hybrid - Interconnection

- Hybrid pixel detectors are costly because of cost of die-die interconnection
- New interconnection technologies use wafer-wafer or wafer-die
- Examples copper-copper direct bonding (e.g. IMEC, LETI) or hybrid direct bonding (Ziptronic DBI)

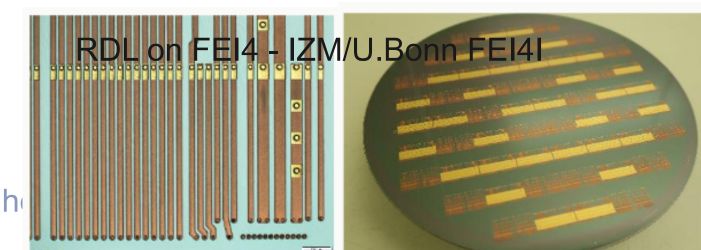
- Wafer level assembly requires through silicon vias (TSV) to bring electrical connections
  - Via-last examples and Cu redistribution layer on wafer back-side by e.g. Fraunhofer IZM for ATLAS FEI4
- All these technologies are industry-driven and we are technology users
- Very good relation to dedicated industry in longer-lasting projects are essential to gain satisfactory results for HEP

IMEC direct bonding





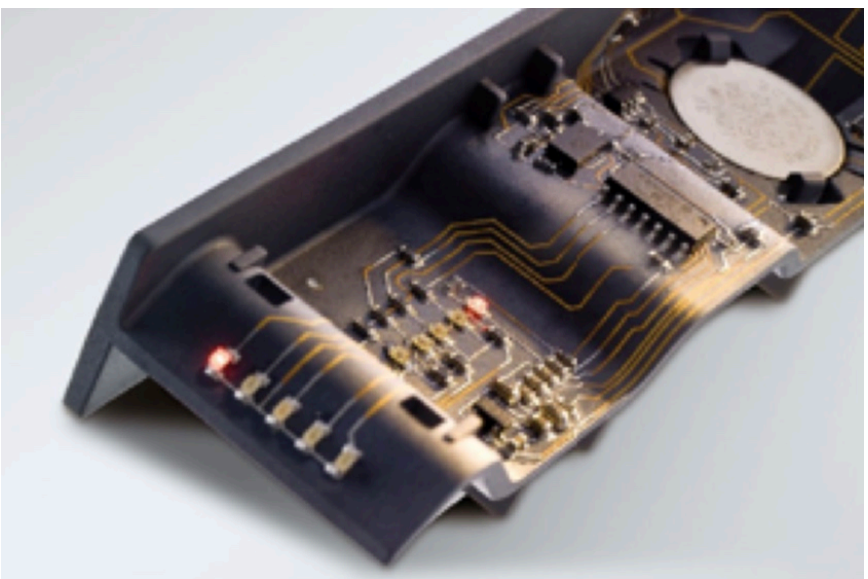
TSV - IZM/U.Bonn FEI4I



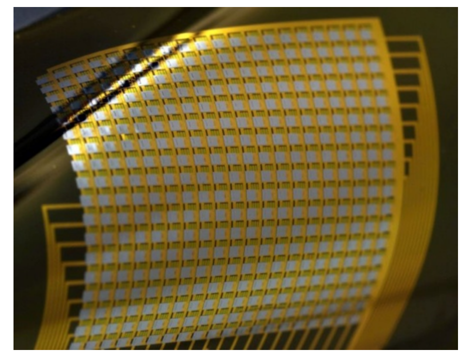
RDL on FEI4 - IZM/U.Bonn FEI4I

Module Construction & Interconnect

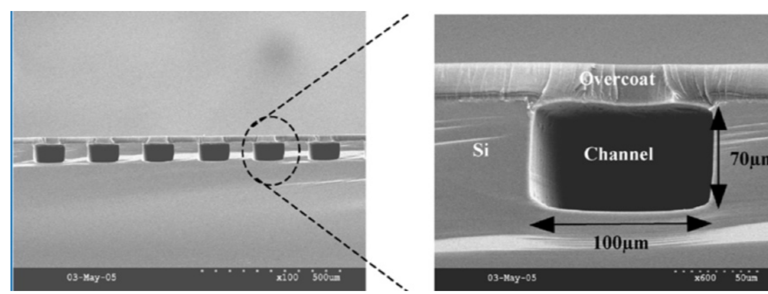
- Investigation of **new materials** (graphene,…) and **thermal management concepts** to work out new and reliable module concepts
- Reduce CTE miss-match, material and **simplify assembly process** by exploring new techniques (additive manufacturing, printing,…)



LED Professional, 13 Sep 2011. https://goo.gl/aVkLzo



http://engineering.nyu.edu/press-release/2011/11/14/

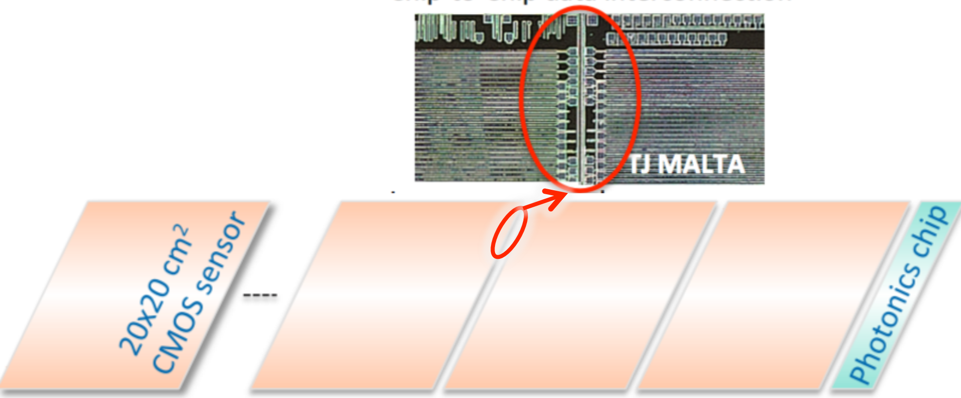


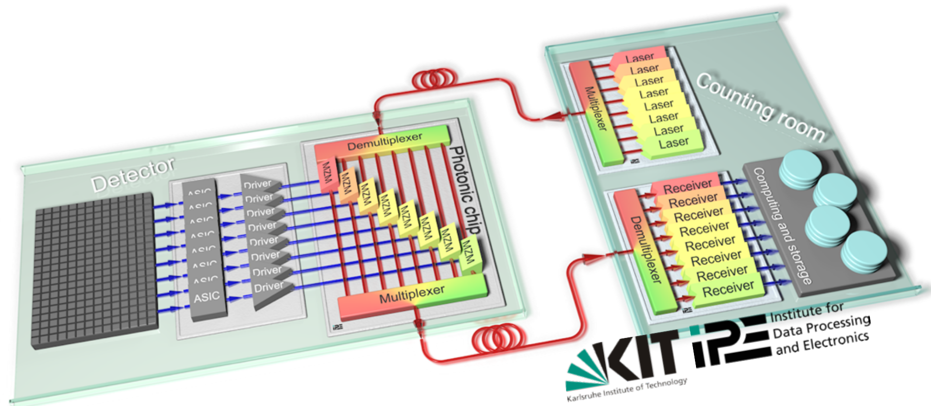
http://ieeexplore.ieee.org/document/1580600/

System design for future trackers

- Future silicon tracker modules will need tight integration with data transmission and powering systems
  - efficient assembly and packaging technique
  - Serial powering to reduce cables
  - High hit rates and/or trigger-less readout results in very high data rates:
- Explore new solutions for data aggregation and transmission from sensor to stave end
  - E.g. demonstrator module with sensor to sensor interconnection and high-speed data readout via photonics chip

Chip-to-Chip data interconnection



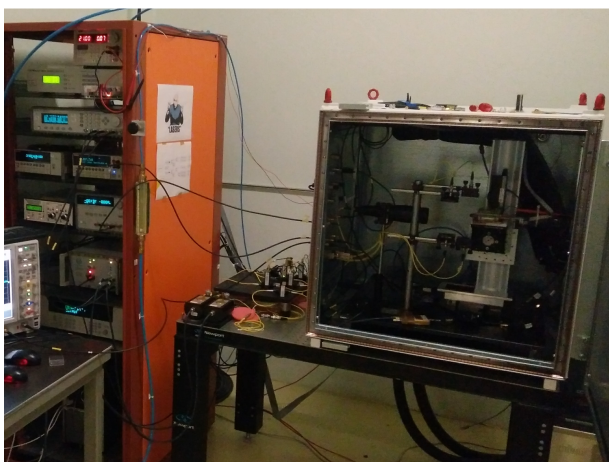


Characterization Techniques for silicon

- New challenges for sensor characterization:
  - Sensors getting smaller and more integrated + have new functionalities (e.g. gain)
  - Harder to access processing properties (e.g. CMOS)
  - Environment gets harsher (higher fluences)

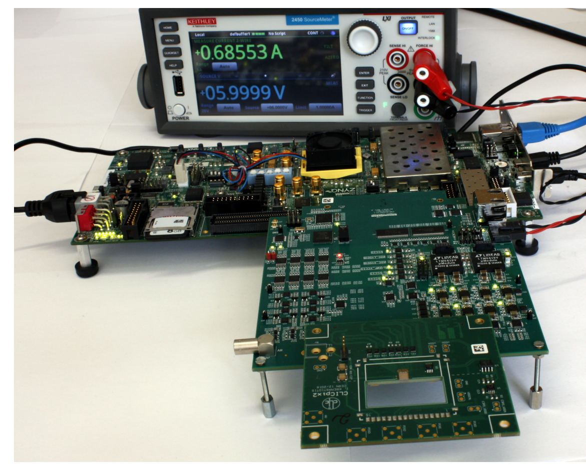
- Characterization tools have to follow
  - **advanced TCT**, **beam telescopes**, **flexible r/o systems**, …

TCT – Transient Current Technique



High-rate beam telescope

CaRIBOU universal r/o system



Summary

- The required functionality from silicon tracking detectors leads to more and more complex detector systems to cope with accelerator's present and future performance
- The need for these new complex systems has triggered a **large RD effort in the area of sensors, electronics and detector integration**
- **Hybrid pixel dete**ctor detector for HL-LHC cope with **enormous radiation level and hit rates** together with sophisticated on-chip data handling
- **Monolithic CMOS sensors** are being developed for **high-radiation environments with complex readout architectures** for future large pixel systems
- The **combination of timing and tracking** leads to the development of new sensors for new level of performance in future silicon system
- Developing and **integrating these sensors to modules** and systems leads to many new RD collaborations with semiconductor industry for manufacturing and post-processing

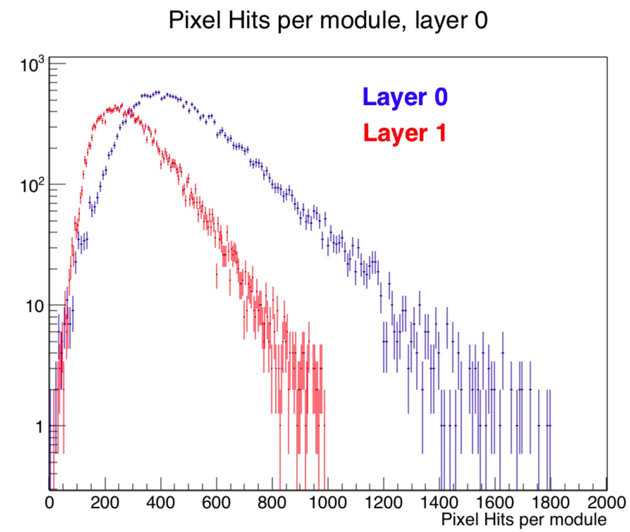
Backup slides

ATLAS CMOS Pixel Collaboration

- Collaboration of ~25 ATLAS ITK institutions

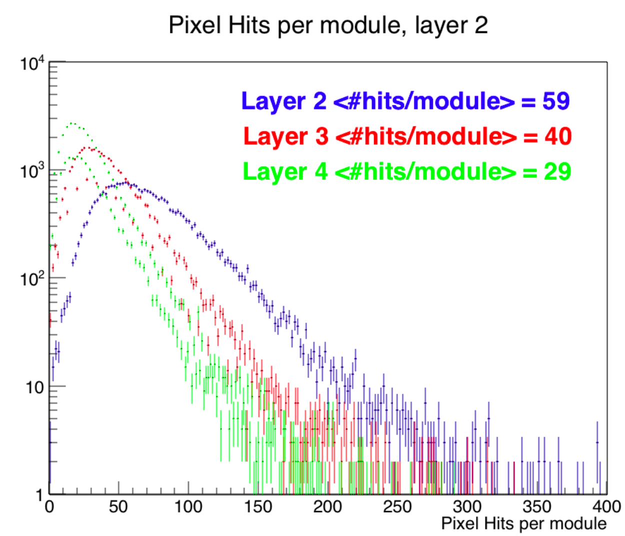
Hitrates per module in different (pixel) layers

- Example Atlas ITK pixel simulation of pixel 50x50x (150μm depletion)
- Collisions per bunch crossing μ=200
- Module size 33.8mm (phi) x 40.3mm (z) (or 16.9x40.3 for L0)
- Look at average number of hits per module or per column per BC



- <hits/mod> Layer 0 = 464 and Layer 1 = 289
- <hits/mod> Layer 2 = 59, Layer 3=40 and Layer 4 = 29
- Tails up to 4x average

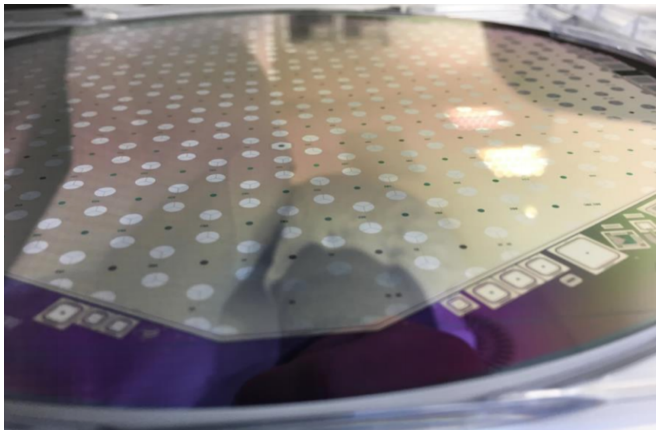
- The high hitrate dominates the complexity of design in Front-end IC as well as data transmission off the detector
  - E.g. large memory on FE chip and number of data link from modules to readout system



k)

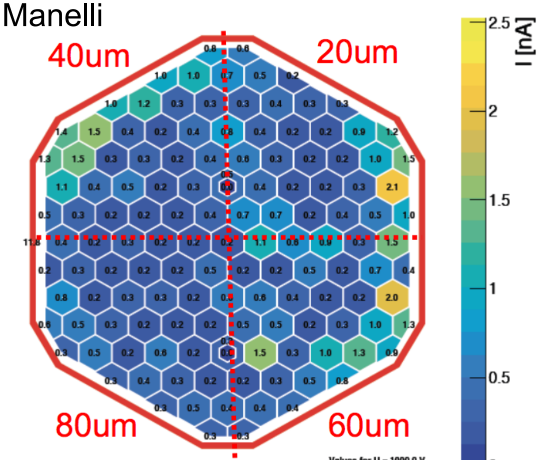
Silicon pad detectors

Si pad detectors with ~0.5-1 cm^2 area for active layers of fine-grained sampling calorimeters



CMS-HGCAL sensor wafer

M. Manelli



CMS-HGCAL sensor leakage currents

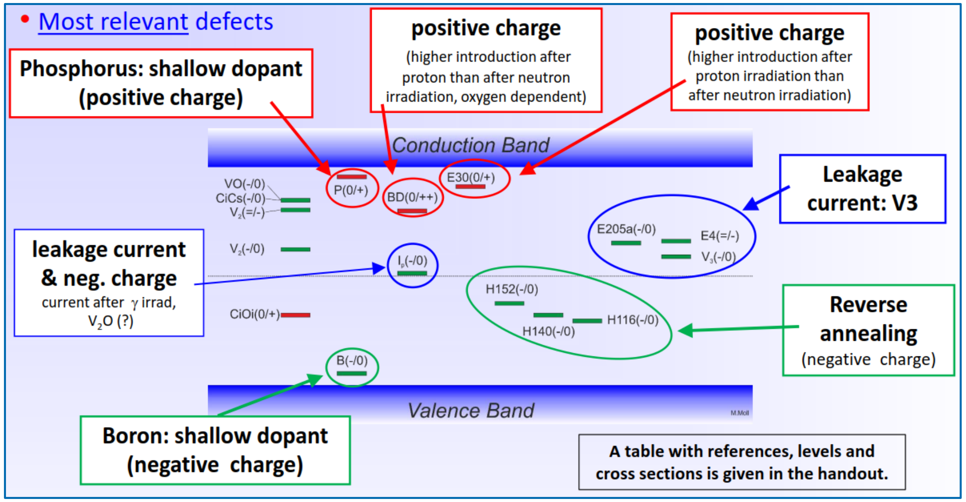
- State of the art: **CMS-HGCAL**
  - 600 m^2 of silicon pads, fluence up to 10^{16} n_{eq}/cm^2,
  - <100 ps timing per cell at 3.5 MIPs and S/N~40
- Si pad detectors under consideration for EM and forward calorimeters at future facilities (LHCb Upgrade II, ILC, CLIC, FCC)

- Many challenges at **system level**:
  readout ASICs, clock distribution,
  module design, interconnects, cooling, automated production
  → Mainly addressed in **Calorimeter** and **IC** WGs

- Silicon-specific R&D needs (WG 1):
  - **Sensor technology**: planar, passive CMOS, LGAD
  - Sensor **characterization** and **simulation**
  - Understanding/mitigation of **radiation effects**

Device Simulation and Modelling

- Microscopic simulations for in-depth understanding of charge collection and radiation effects in silicon increasingly important:
  very high doses/fluences at HL-LHC, FCC; complex sensors (e.g. CMOS, LGAD)



M. Moll

- Significant progress on **defect characterization** over last decade
- **knowledge** about defects is <u>essential</u> to understand the physics of radiation damage and to perform device simulations and **defect engineering**

- **Future R&D in a large collaboration (RD50) to improve understanding:**
  - **Full identification of the structure of the defects**
  - **Predictive Modelling, improved TCAD simulations**
  - **Defect generation and modelling at very high fluences**
    - Note: Many characterization tools don't work properly for extreme fluences
  - **Better radiation background simulation → reduction of safety factors**