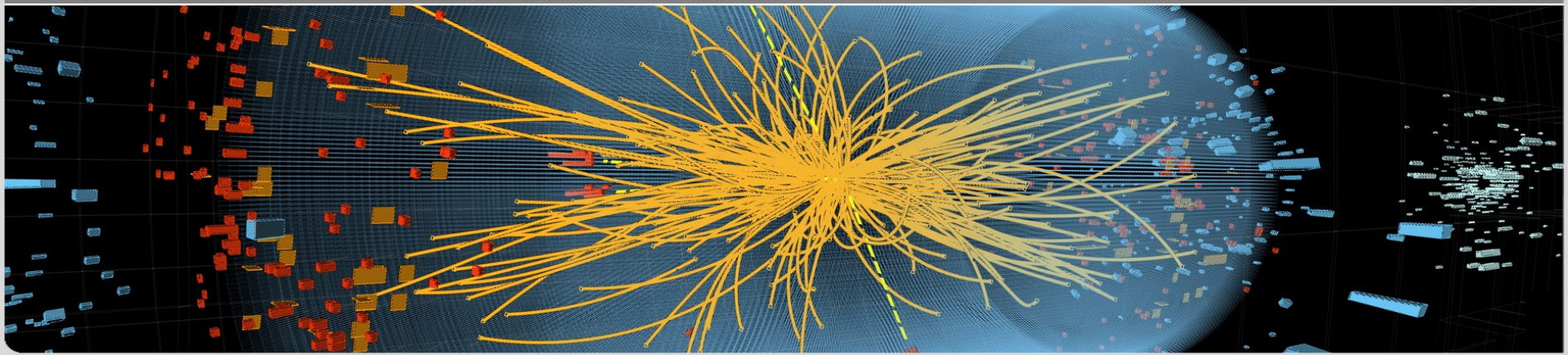
Karlsruher Institut für Technologie

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

The HL-LHC CMS Level-1 Track Trigger

Luis Ardila

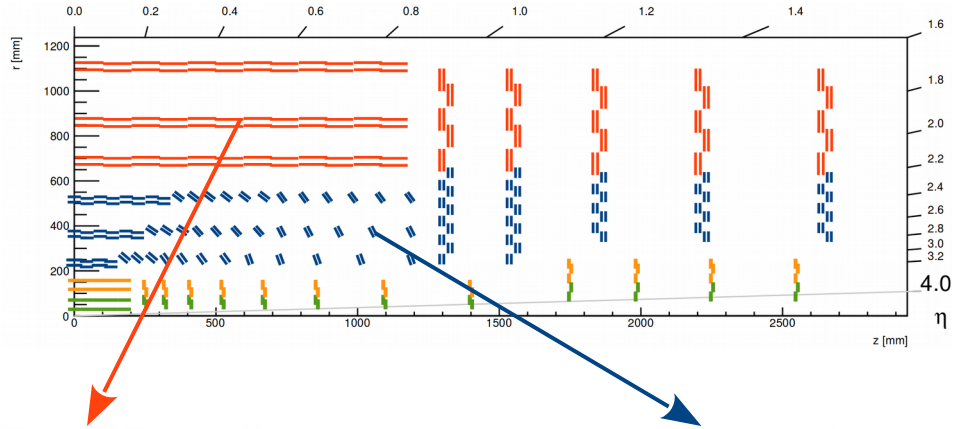
INSTITUTE FOR DATA PROCESSING AND ELECTRONICS (IPE)

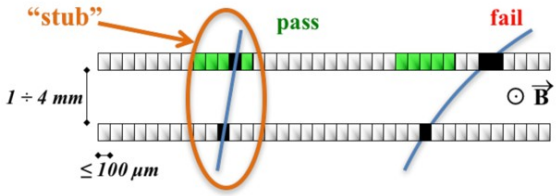


A TRACKER BUILD FOR TRACKING

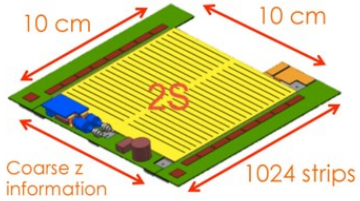
p_T discrimination provided by use of special modules

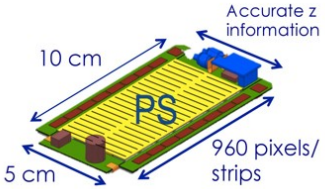
- Pairs of closely spaced silicon sensors, separated 1-4 mm
- Signals from each sensor are correlated
- Only hit pairs compatible with **p_T > ~2GeV/c ("Stubs") are forwarded off-detector**
- Factor ~10 data reduction





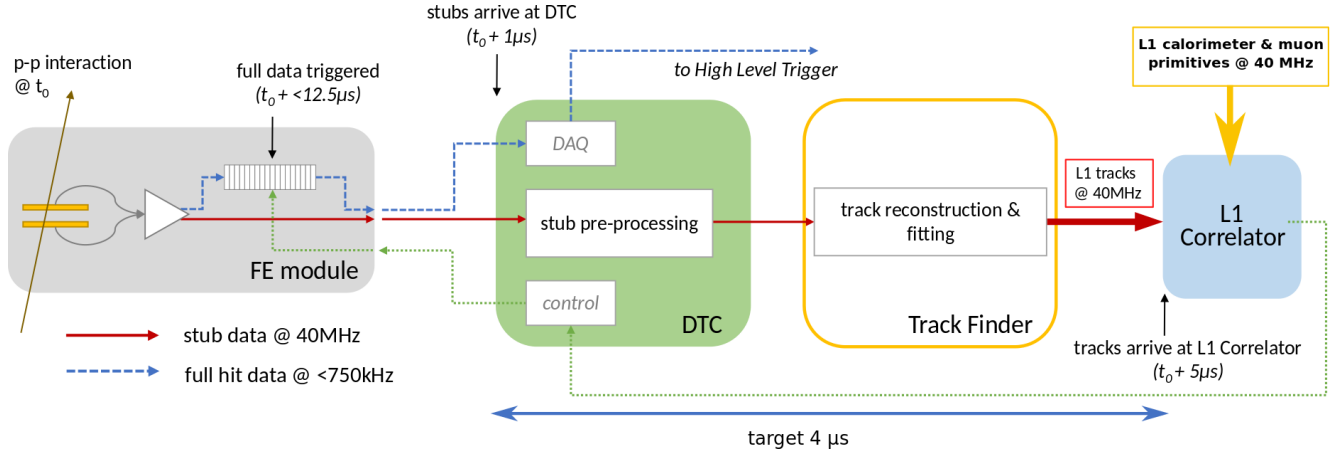
Strip Sensor × 2:
5 cm × 90 μm
+
Strip Sensor × 2:
5 cm × 90 μm





Strip Sensor × 2:
2. 5 cm × 100 μm
+
Pixel Sensor × 32:
1.5 mm × 100 μm

TRACKER → TRIGGER DATA FLOW



L1 hardware trigger reduces event rate from **40 MHz to <750 kHz** using calorimeter, muon and tracker primitives

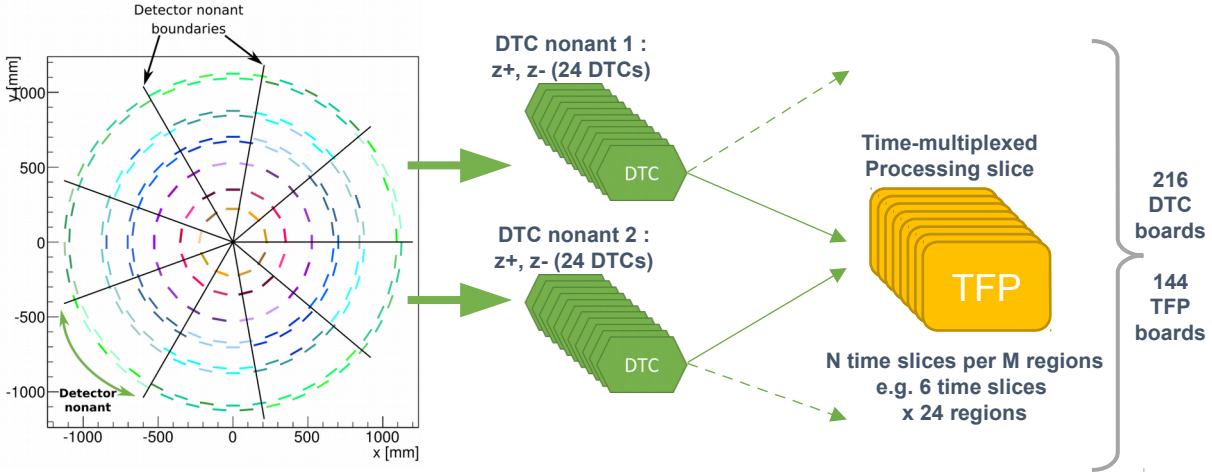
- **TK primitives are all tracks (pT > 2-3 GeV/c) from Outer Tracker**
- L1-Accept triggers all front-end buffers to read out to DAQ → HLT farm

FE L1 latency buffers limited to 12.5 μs

Transmission of stubs to BE electronics	1 μs
Correlation of trigger primitives (inc. tracks)	3.5 μs
Broadcast of L1-Accept to FE buffers	1 μs
Safety Margin	3 μs

→ Track finding from stubs must be performed in 4 μs

TRACK FINDER ARCHITECTURE



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane

Outer Tracker cabled into **nonants**

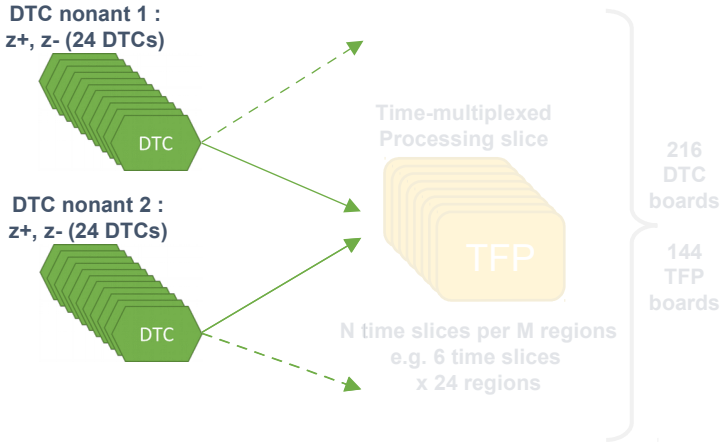
Use of time-multiplexing to increase parallelization

- Time-multiplexing directs data from multiple sources to a single processing node
- **1 event per processing node**

Processors are independent entities → simplifies commissioning and operation

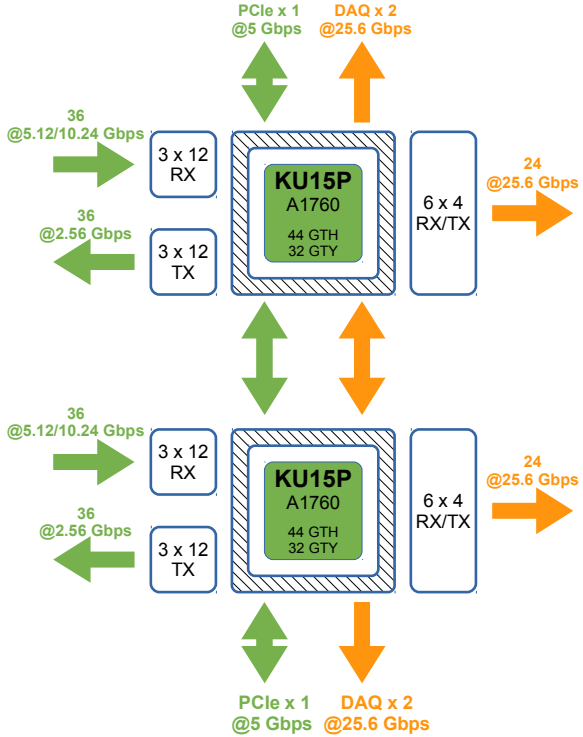
Spare nodes available for redundancy

TRACK FINDER ARCHITECTURE – DTC



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane



DTC card must handle

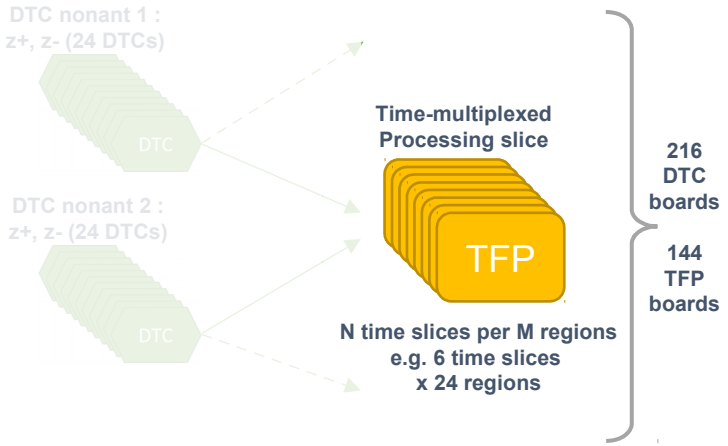
- **<=72 modules (5G/10G lpGBT opto-links)**
- Control/Readout for each module
- Direct L1 stream to central DAQ (16G/25G)
- Direct stub stream to TFPs (16G/25G)

Stub pre-processing includes:

- **Local→ Global** look up, position calibration
- Sort and pre-duplication
- Time-multiplexing

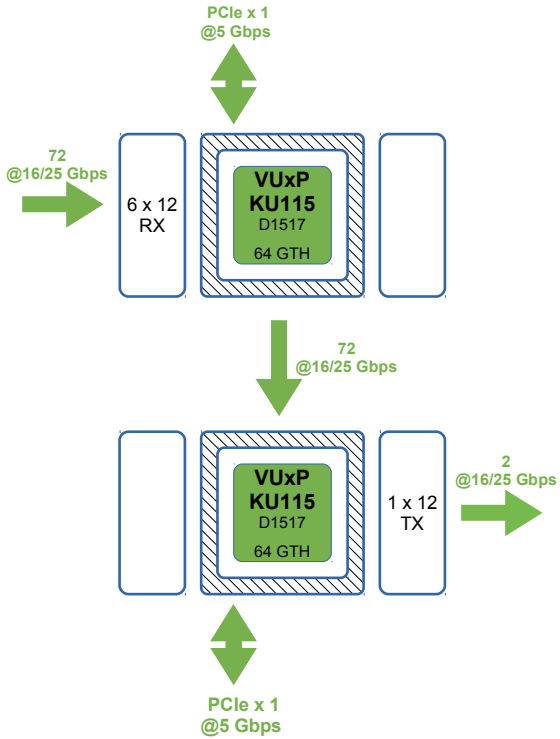
→ **216 DTC boards, 18 shelves, 1 rack/nonant**

TRACK FINDER ARCHITECTURE – TFP



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane



→ **144 TF boards, 12-18 shelves**

TFP card must handle

- **Up to 72 DTCs (16G/25G optical links)**
- Track Finding from stubs
- Track Fitting
- Transmission to L1 Correlator Trigger

High bandwidth processing card

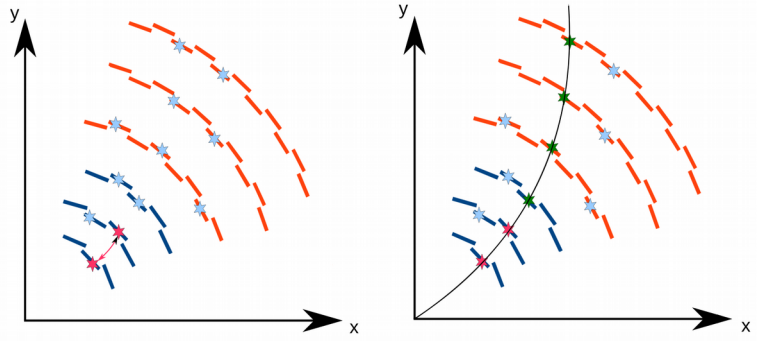
- **~1 Tb/s** processing bandwidth
- Rate to L1 Correlator much lower < 30 Gb/s

TRACK FINDING ALGORITHMS

Check Poster on Tuesday

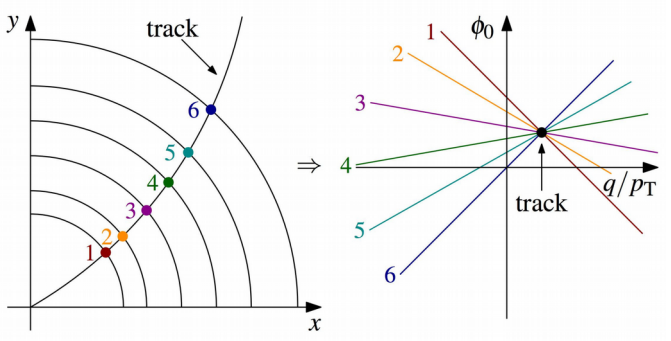
Karlsruher Institut für Technologie

Two main algorithms for reconstructing tracks, plus a number of hybrids, variation and options



TRACKLET APPROACH

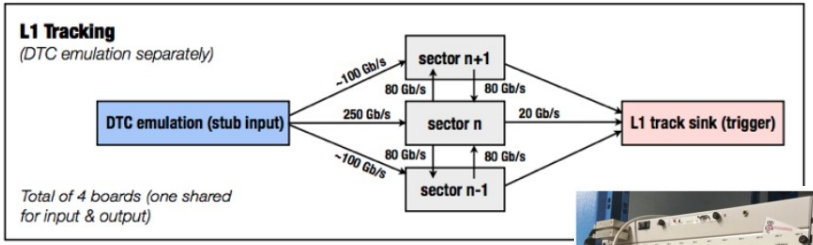
- Combinatorial approach using **pairs of stubs as seeds**
- **Extrapolation** to other layers → hit matching
- **Linearized χ2** fit on candidates
- Uses **full resolution stubs** at earliest stage of processing
- N time-slices x M regions → 6 x 24, 9 x 18

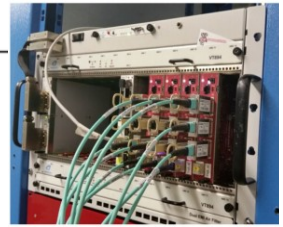


HOUGH TRANSFORM + KALMAN FILTER APPROACH

- Uses a **Hough Transform** to detect coarse candidates
- Candidates are filtered and fitted in a single subsequent step using a **Kalman Filter**
- Combinatorial problem pushed to latter stages of processing
- N time-slices x M regions → 18 x 9

HARDWARE DEMONSTRATORS

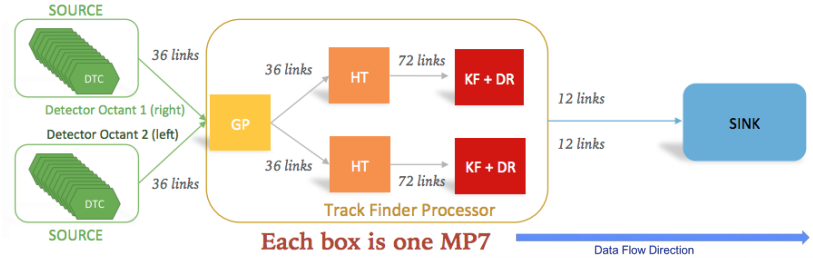


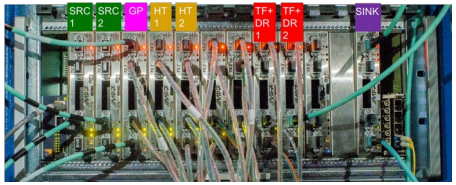


Demonstrator in hardware, verified using emulation software

Hardware demonstrator has been built to validate the algorithm and measure latency

- 4 CTP7 boards with Virtex-7 FPGA – 3 CTP7 cover 3 Φ sectors – 1 CTP7 emulate DTC
- 1 AMC13 card for clock and synchronization
- 240 MHz internal fabric speed
- Measured latency of **3.33 µs** in agreement with latency model



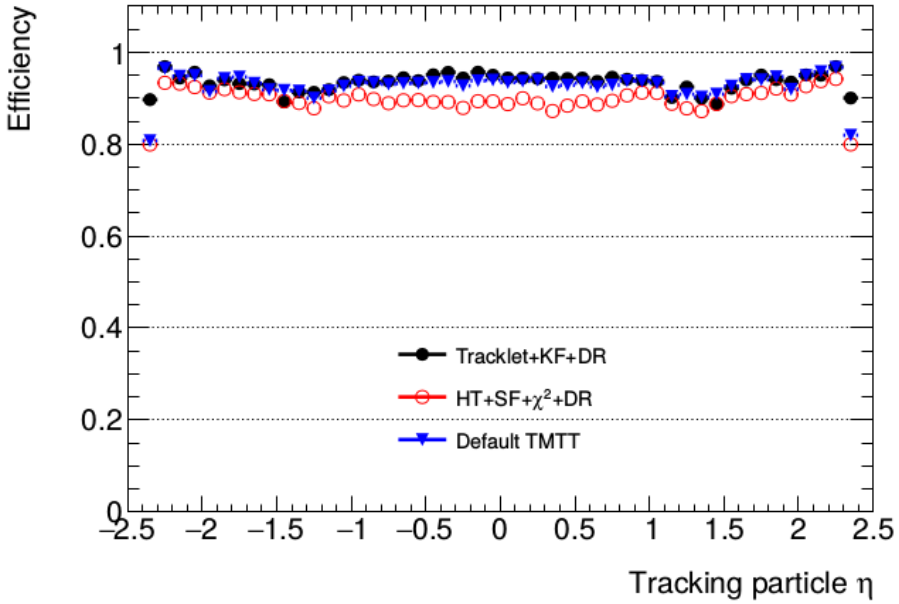


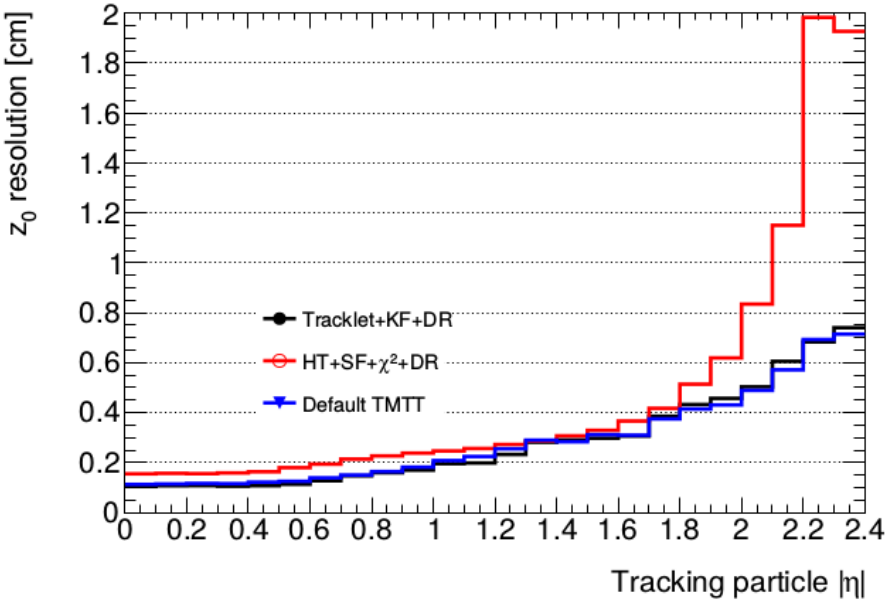
Both Demonstrators were tested with samples from PU 0→ 200

Demonstrator in hardware and emulation

- One per time multiplexing and detector nonant
- Each box is one MP7 board with Virtex-7 FPGA
- Can compare hardware output directly with software
- 240 MHz internal fabric speed
- Latency verified to be **3.5 µs**

HYBRID ALGORITHMS



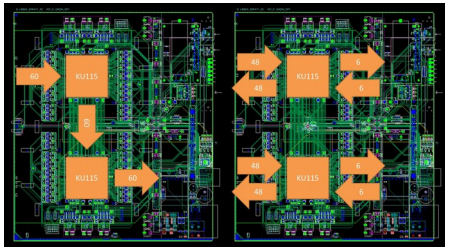


Efforts have started to **merge** the two approaches

- Working on defining a **reference algorithm**

R&D

Bristol University, Imperial College, Ioannina, INFN, KIT, RAL, SACLAY, TIFR



Karlsruher Institut für Technologie

ATCA infrastructure

- Systematic **thermal studies** about air x-section and impact on opto-lifetime
- Backplane signal integrity → important for DAQ/timing

Use of **interposer technology**

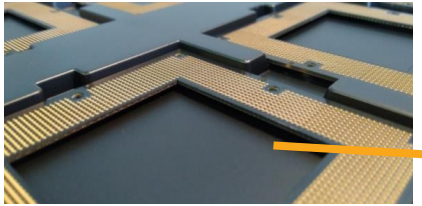
- Flexibility (e.g. FPGA)
- Mitigate losses/costs due to yield issues
- Modularity; separate complex and simpler part of the board design

On-board computing and control variety

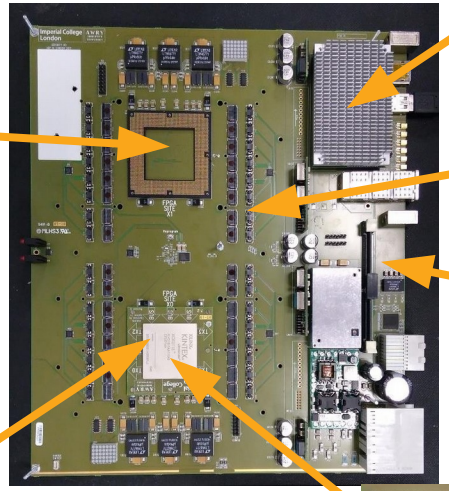
- Standard on-board PC (COM Express mini)
- Zynq Soc
- IPMC only

PCB design practices, stackup and material

- Build up relationship with manufacturers

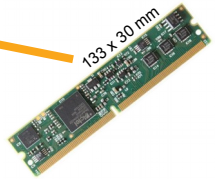


Samtec Z-RAY interposer



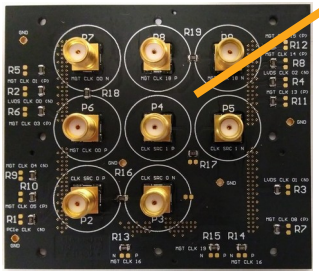
COM Express

Samtec Firefly x12 RX/TX pairs

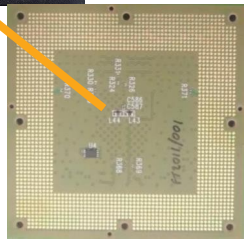


CERN-IPMC

Clock test daughtercard



FPGAs
KU115
KU15P
VU9P
daughtercards



THERMAL SIMULATION AND TESTS

Simulation setup

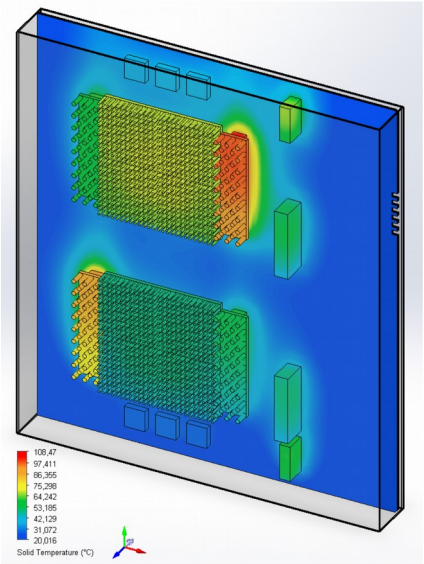
- PCB imported from PADS
- Placed in a 33 mm deep tunnel
- 4 m/s airflow from bottom (20 °C) to top

Placed components

- KU15P (50 W) doubled θ_{JB} to take interposer into account
- Firefly banks 25 G (30W) and 16 G (12 W)
- **Total power 205.4 W**

Test setup

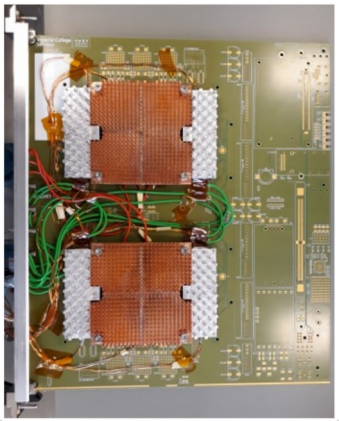
- Two heat-pads **45 mm x 45 mm** and **12 mm x 70 mm**
- Just one mockup board is present, it will be put in between two additional soon
- **~11 W for 6x block** of 16 Gbps optics
- **~10 W for 6x block** of 25 Gbps optics

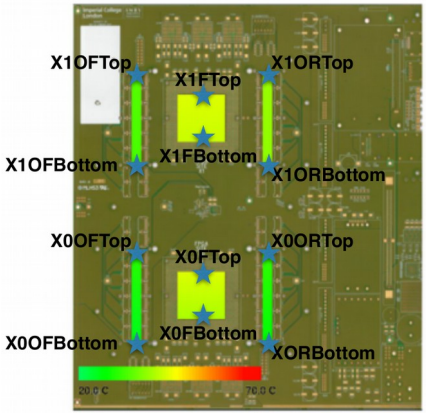


Test1 (°C)
4xFan-block speed=50%
Exhaust temp ~17°C (~amb)
Power on FPGA heaters = 86 W
Power on Optics heaters = 41 W

X1FTop = 60.7
X1FBottom = 59.1
X1ORTop = **50.8**
X1ORBottom = **49.7**
X1OFTop = 43.1
X1OFBottom = 41.7

X0FTop = 53.7
X0FBottom = 50.1
X0OFTop = 35.8
X0OFBottom = 28.2
X0ORTop = 37.2
X0ORBottom = 31.1





SUMMARY

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

KIT
Karlsruher Institut für Technologie

L1 track trigger at HL-LHC necessary but also challenging

- p_T modules provide first layer of efficient data reduction

Two all-FPGA approaches: **Tracklet** and **TMTT**

- Use high-performance FPGAs
- Highly parallelized tracking algorithms
- Data organization → pattern recognition → track fitting → duplicate removal
- **Both have demonstrated feasibility and good performance**

Efforts have started to merge the two approaches

- Working on defining a **reference algorithm**
- **Common infrastructure R&D**
  - ATCA thermal simulations and tests
  - Slow-control and shelf manager concept
  - High-speed optical link test