The progress in LumiCal readout electronics

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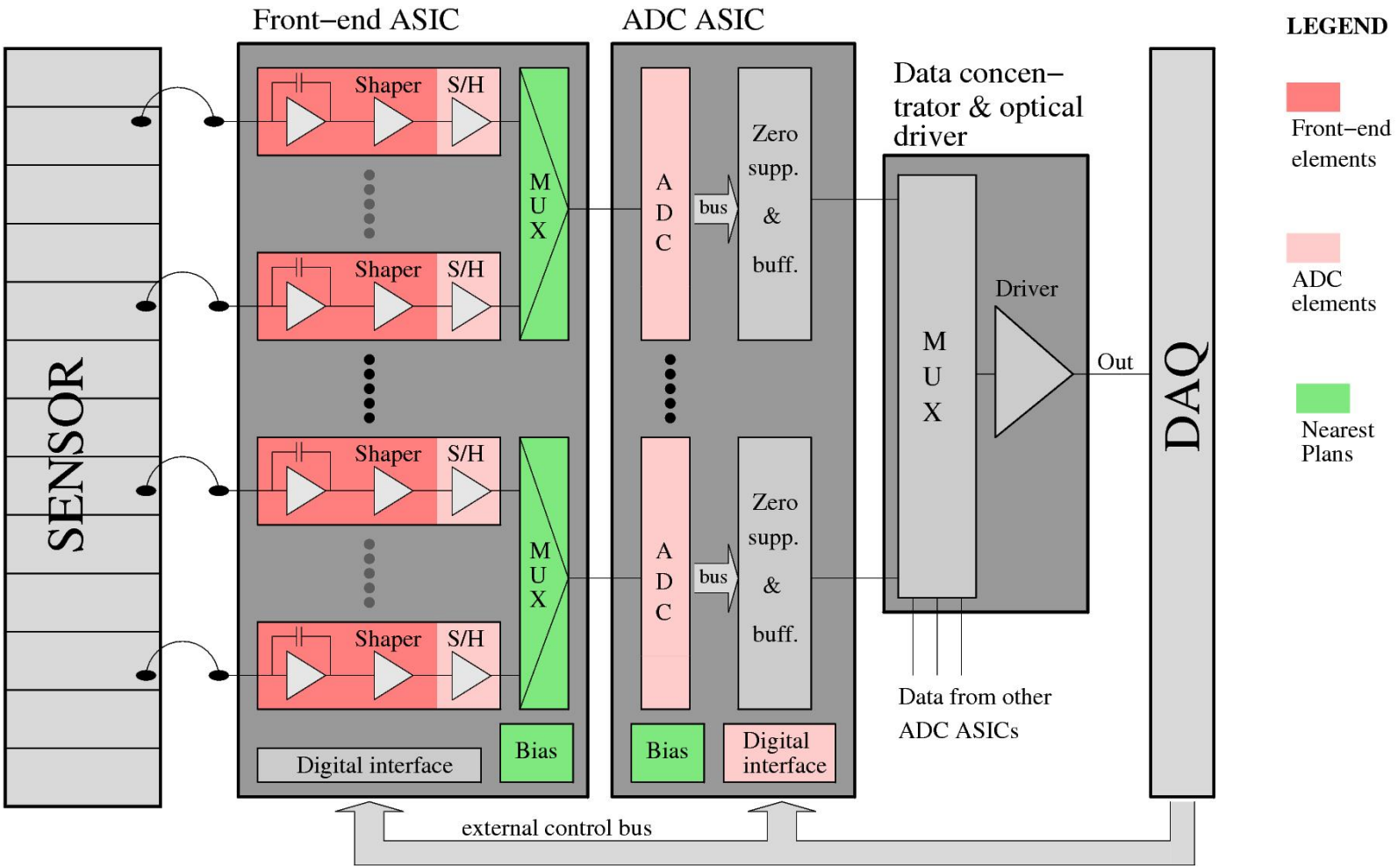
Outline

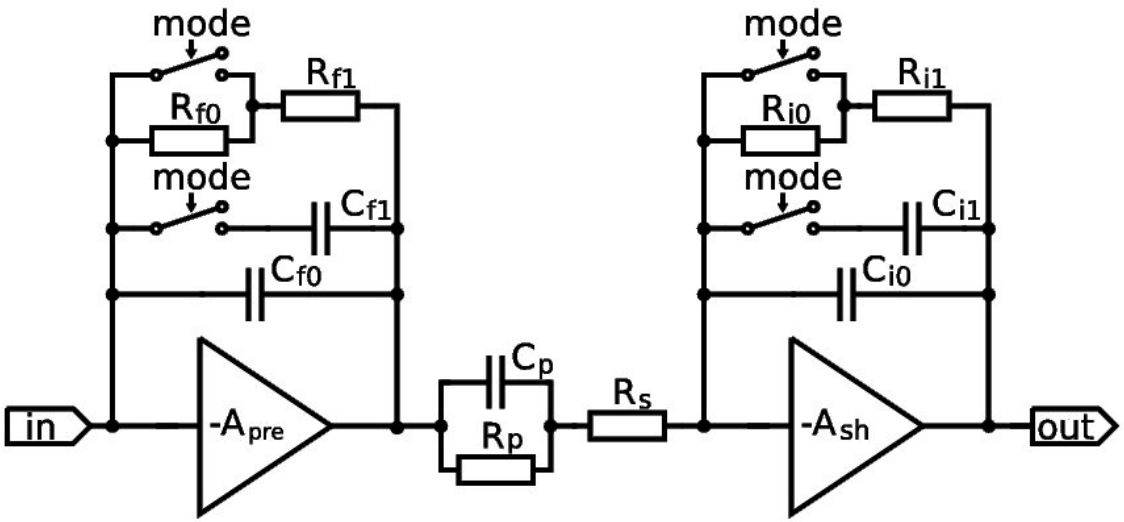
Our work

- Front-end chip one submission 4 (Rf) + 4 (MOS) channels — May 2007
  - tested and fully operational
  - agreement with simulations
- ADC core (8 pipeline stages) — May 2007
  - tested and operational
  - some nonlinearity problems (DNL higher than expected)
- 10 bit ADC (almost complete) with and without S/H — September 2008
  - under test

LumiCal Readout System



Front-end requirements (old)



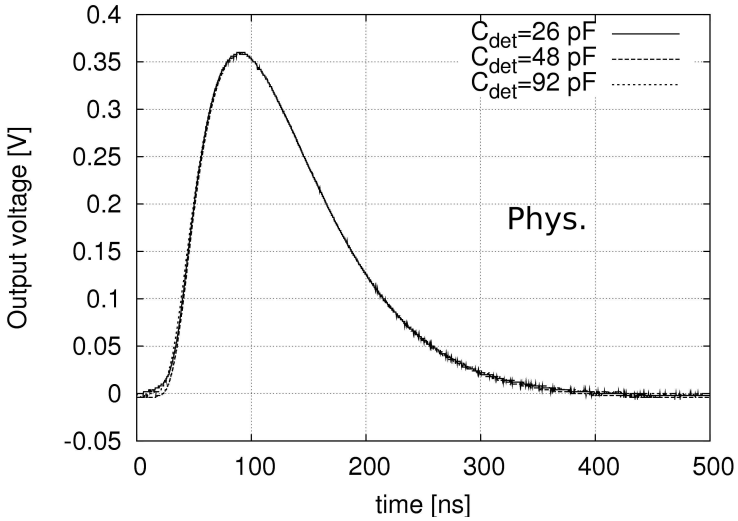
Components

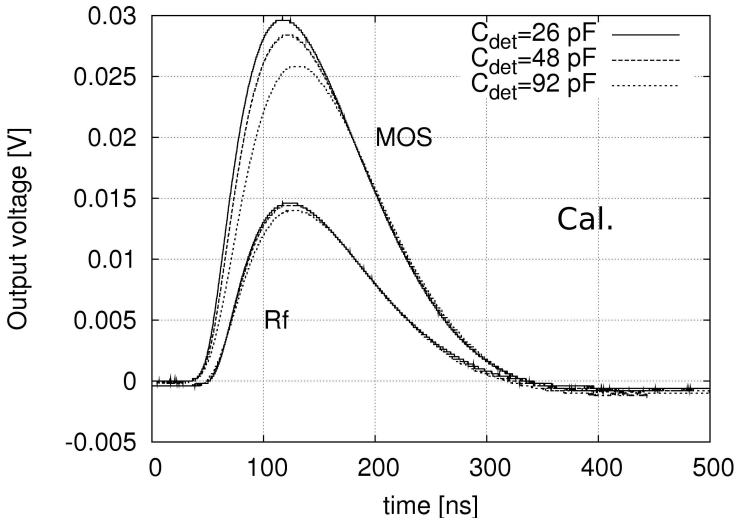
- Charge amplifier
- Pole zero cancellation
- 1st order shaper

- $C_{det} = 10 \div 100$ pF $\rightarrow$ charge sensitive amplifier
- $\Delta t \simeq 300$ ns $\rightarrow$ $T_{peak} \simeq 60$ ns
- Two independent modes: physics and calibration (MIP) $\rightarrow$ gain switched as a configuration option
- Physics mode: $Q_{max} \approx 10$ pC $\rightarrow$ $C_f \approx 10$ pF
- Calibration mode: $S/N > 10$ for MIP

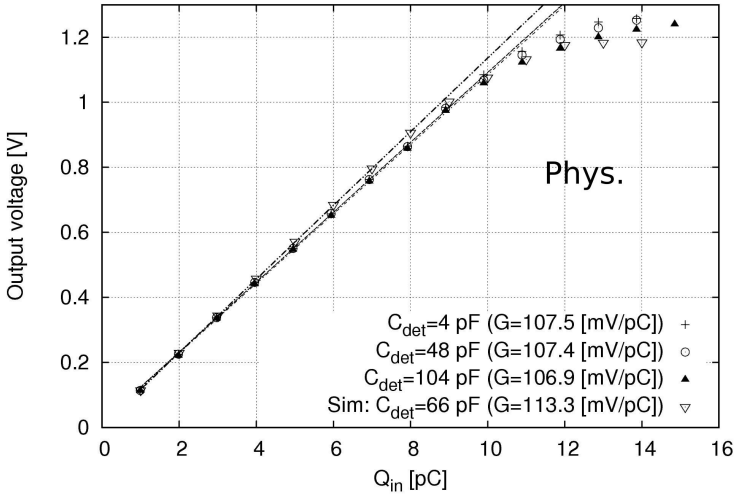
Example pulse shape and linearity

Pulse shape





Gain



- For physics mode $Q_{in} = 3.3$ pC (upper left)
- In calibration $Q_{in} = \approx 10$ fC (left)
- Linear up to 10 pC

Front-end parameters summary

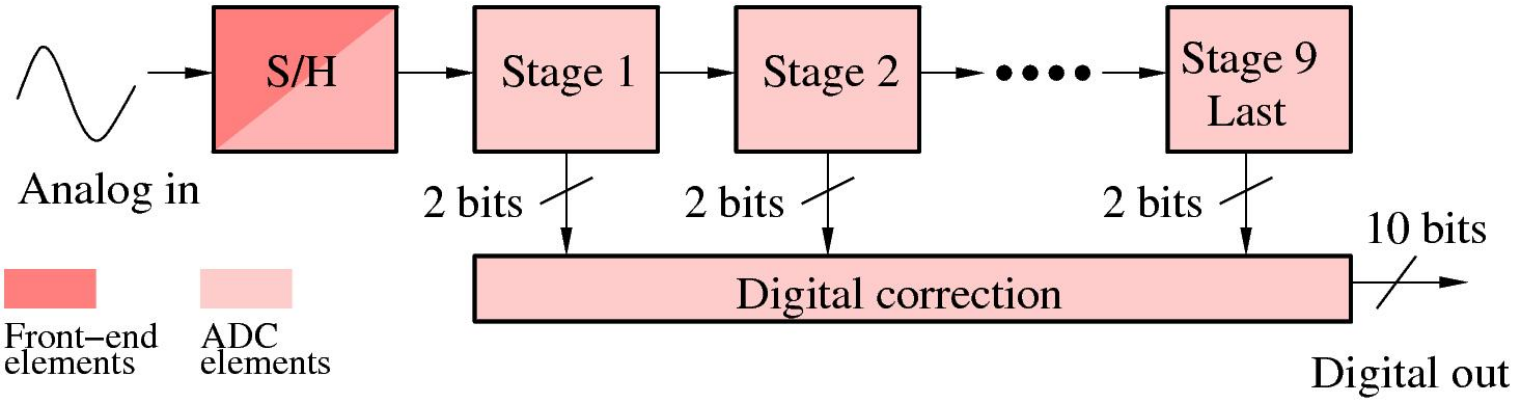
Mode	Gain [mV/fC]	Noise@50pF [fC]	Linearity [pC]	Rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	≈1
Calibration	≈20	0.28	0.035	2.5	≈0.1

- Similar results for both R_F and *MOS* configurations (MOS slightly better)
- Crosstalk needs to be measured with sensor fanout
- Power consumption per channel is 8.9 mW
- Noise in details:
  - $\mathrm{Noise}_{\mathrm{phys}}[\mathrm{aC}] = 522 + 2.08 \cdot C_{in}[\mathrm{pF}]$
  - $\mathrm{Noise}_{\mathrm{cal}}[\mathrm{aC}] = 48 + 4.65 \cdot C_{in}[\mathrm{pF}]$

Front-end status and future plans

- Status
  - First prototype tested and ready for tests with sensor
  - Single prototype chip consist of 8 channels
  - All parameters meet old specification
- Future plans
  - Tests with sensor and fanout
  - Measurements on test beam
  - New prototype will be designed *after* tests with detector and fanout — are there still some parameters to be fixed?

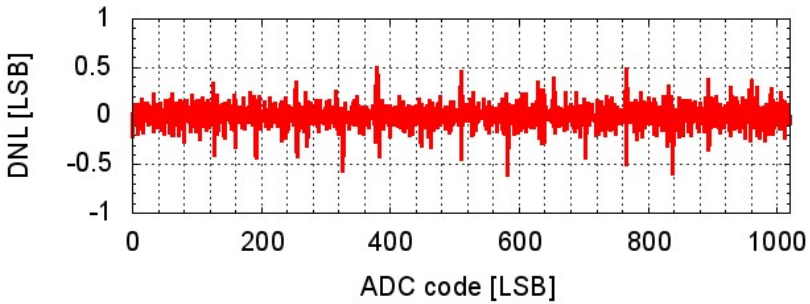
ADC Requirements

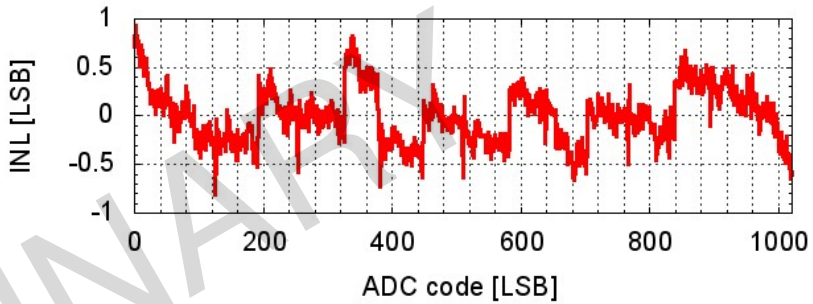


- Speed or clock frequency
  - 3MHz when one ADC per channel ← *most probable conf.*
  - 30MHz when one ADC per ∼8 channels
- 10 bits at the moment
- Power efficient & small area
- Fully differential pipeline architecture
- S/H can be a part of ADC or front-end channel → two prototypes with and without S/H designed

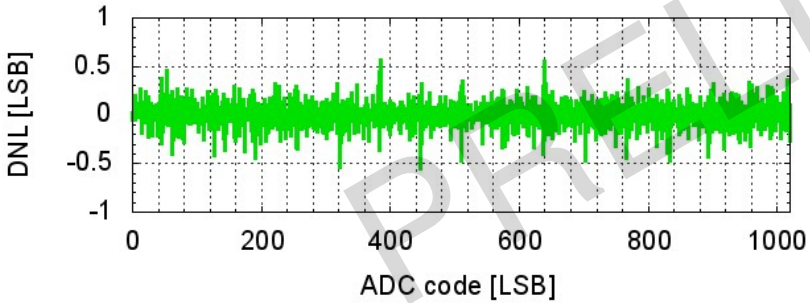
Static Nonlinearities (DNL & INL) at 30 MHz

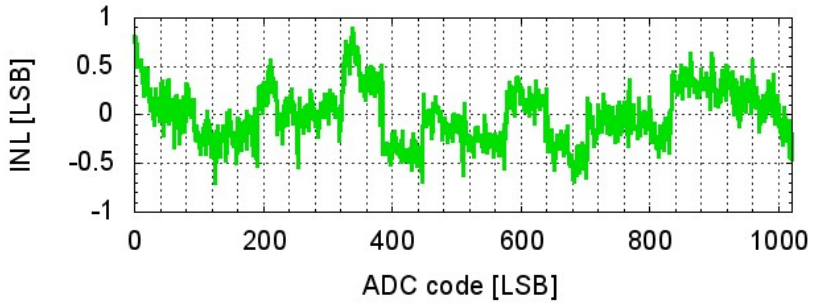
- with Sample&Hold





- no Sample&Hold

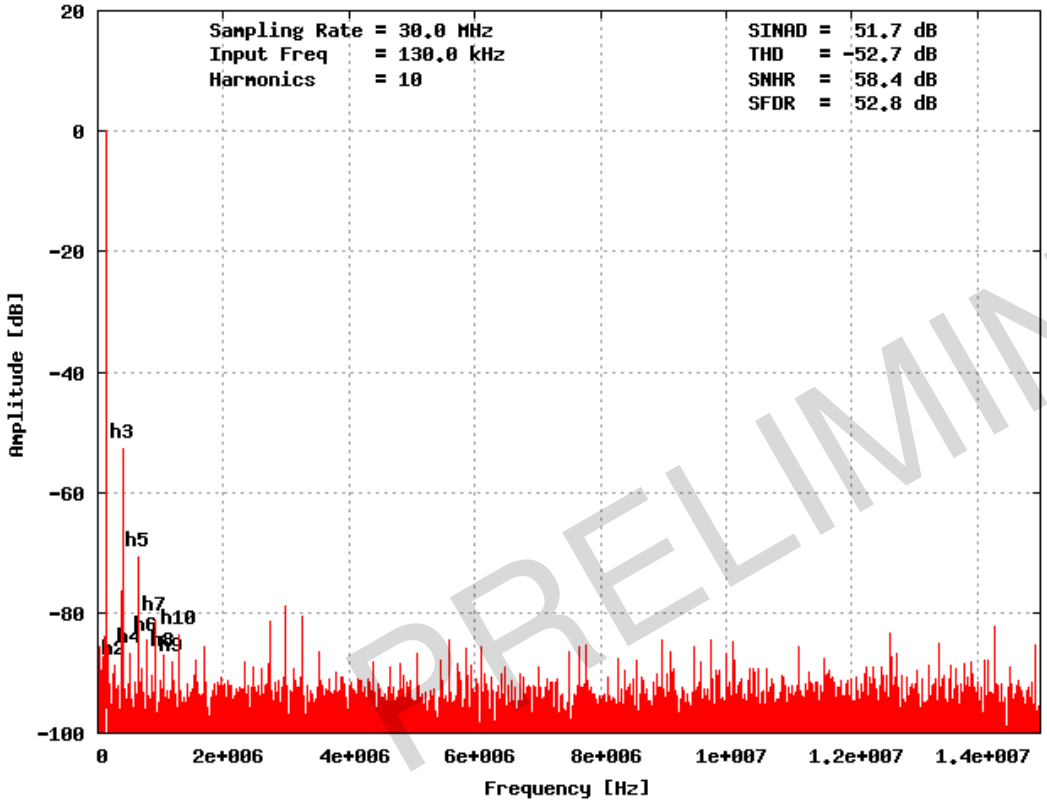




- DNL – difference between ideal and measured ADC step
- INL – the global difference from ideal value
- ENOB is 9.50 for S/H and 9.51 without S/H
- Three different configuration; tests in progress

Dynamic measurements 30 MHz

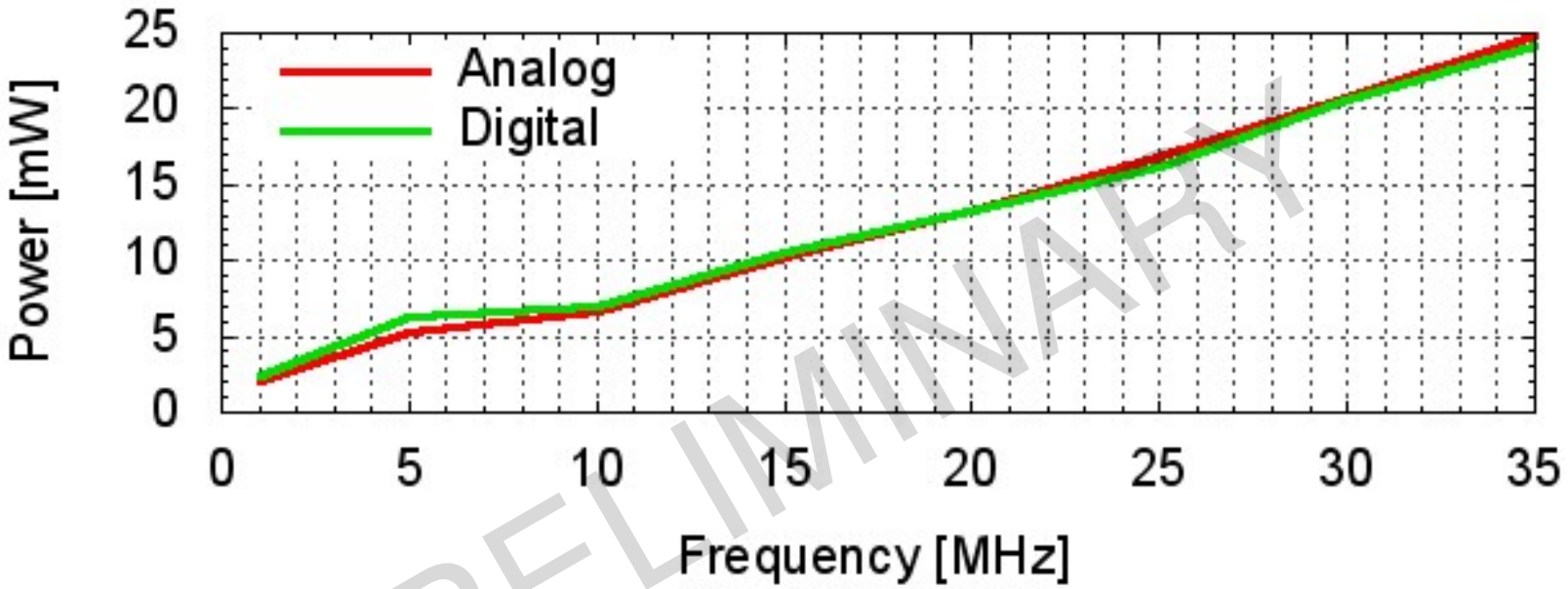
FFT spectre



- SINAD = 51.7 dB (8.2 bits)
- THD = -52.7 dB (8.5 bits)
- SNHR = 58.4 dB (9.4 bits)
- SFDR = 52.8 dB (8.5 bits)

- Very preliminary. In fact first tries
- SNHR (noise) is good
- SINAD low because of harmonic distortions which may come from setup; needs further studies

Power scaling (S/H)

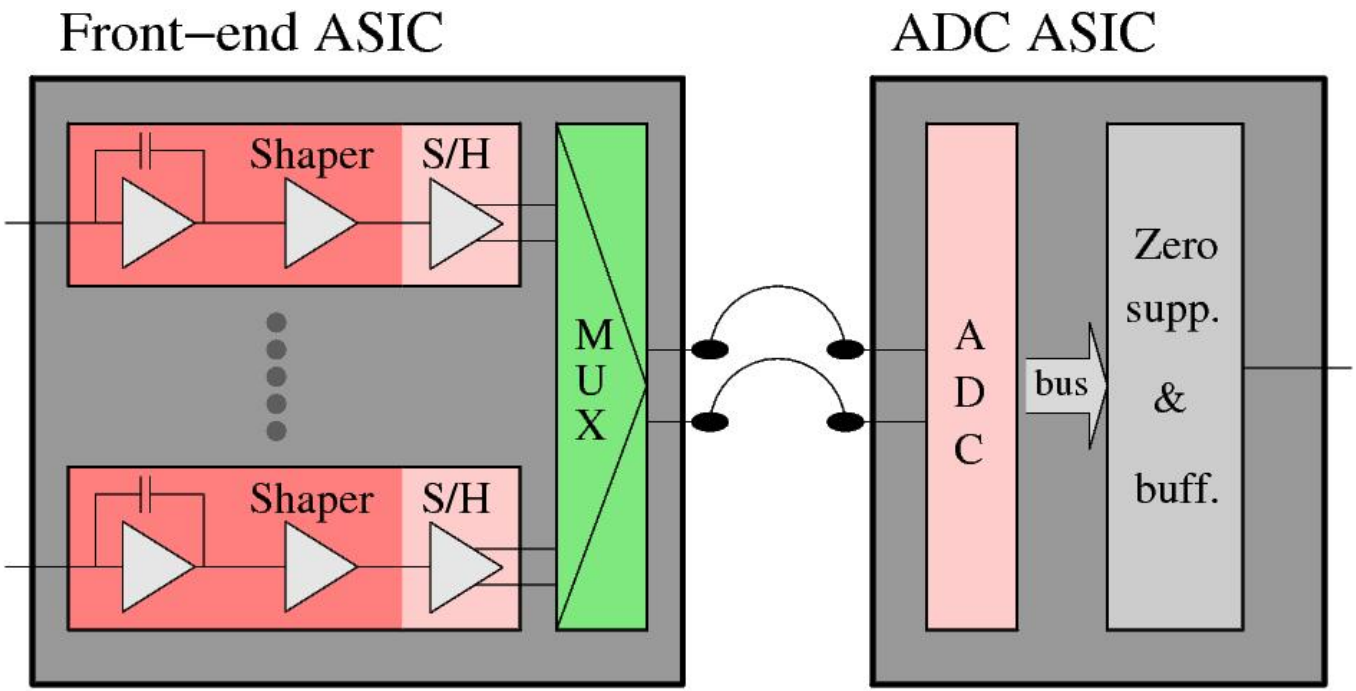


- Analog power measurement procedure:
  - frequency is set
  - biasing are lowered
  - ENOB must be keep high enough

ADC summary and future plans

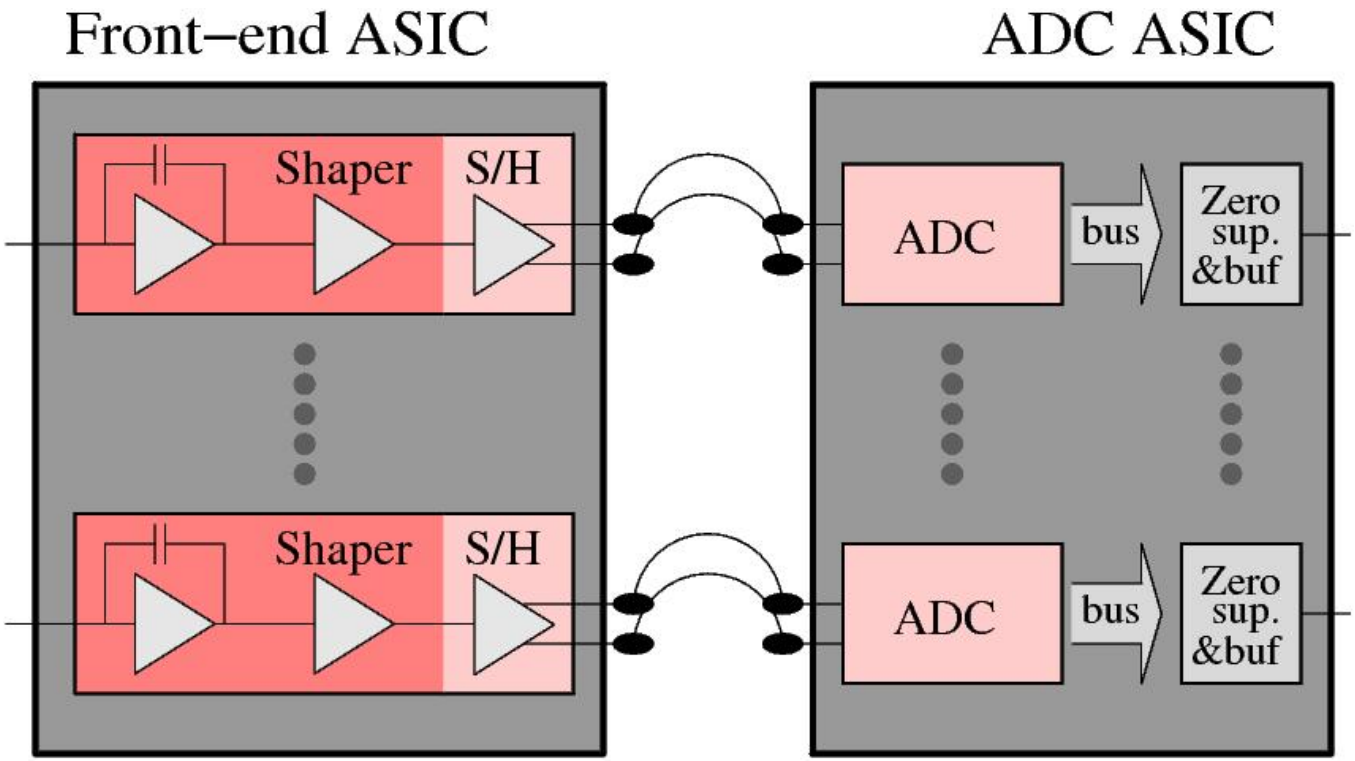
- Summary
  - New 10-bit prototypes of ADC with and without S/H are fully functional
  - They work stable up to about 35 MHz as expected
  - Static measurements show good DNL, INL & ENOB
  - Dynamic measurements — first tries
  - Power consumption can be scaled with frequency
- Future plans
  - Measurements
    - Continue power scaling measurements
    - Preform dynamic measurements
    - Prerform clock and power switching tests
  - Preapare multichannel version

One ADC per 8 channels



- ADC is differential so S/H needs to convert single-ended signal to differential
- Differential multiplexer must be in the analog chip
- S/H + single–diff converter should be in front-end channel

One ADC per single channels



- No multiplexer so design is simpler (but more bonds)
- ADC should be slower but we can scale the power in the current prototype!
- The S/H can be moved to ADC chip → complete removal of clock from front-end chip

Digital processing & data concentrator

- Waiting for detector specification to be established more or less $\rightarrow$ data flux
- Pure digital design so can be done fast in comparison to front-end and ADC
- Will first be designed and tested with FPGA
- FPGA design is enough even for advanced tests (eg. beam tests)
- In most cases no needs of ASIC prototyping
- If design is tested the ASIC implementation in fast (mounth or two)

Summary

- Front-end prototype is finished tested and waits for test beam
- ADC new almost complete prototype is being tested; preliminary results looks promising
- ADC multichannel version is planned
- Digital procesing and data concentrator will be first implemented as an FPGA circuit, so no need of ASIC prototyping