AGH University of Science and Technology

Preparation of Testbeam Equipment (in Krakow)

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Agenda

- Some initial questions
- Sensor and fanout configuration
- Readout chain
- Open issues
- Summary

Is it worth at the present development stage to prepare the "whole" readout chain or even testbeam setup?

- **cons**
  - Only 8 channel analog front-end chip exist (4+4)
  - The specifications for the front-end has changed
    → new slightly different prototype is needed
  - No multichannel ADC exists → external ADC is needed, so no “whole” readout possible...

- **pros**
  - The chain sensor+fanout+front-end has never been tried tougher.
    → **We need to see how it behaves all together**.

- **conclusion: To check the whole chain we need to build such small system, but ...**

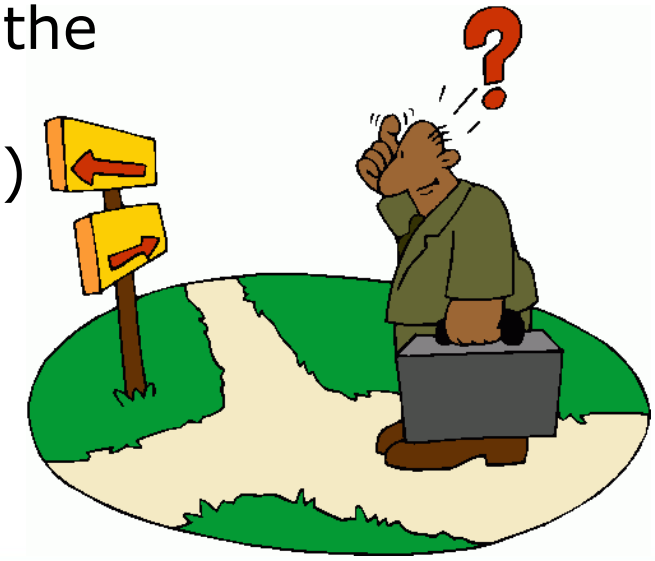
It really worth to prepare the testbeam setup with the existing ASICs ??

(assuming the readout chain works)

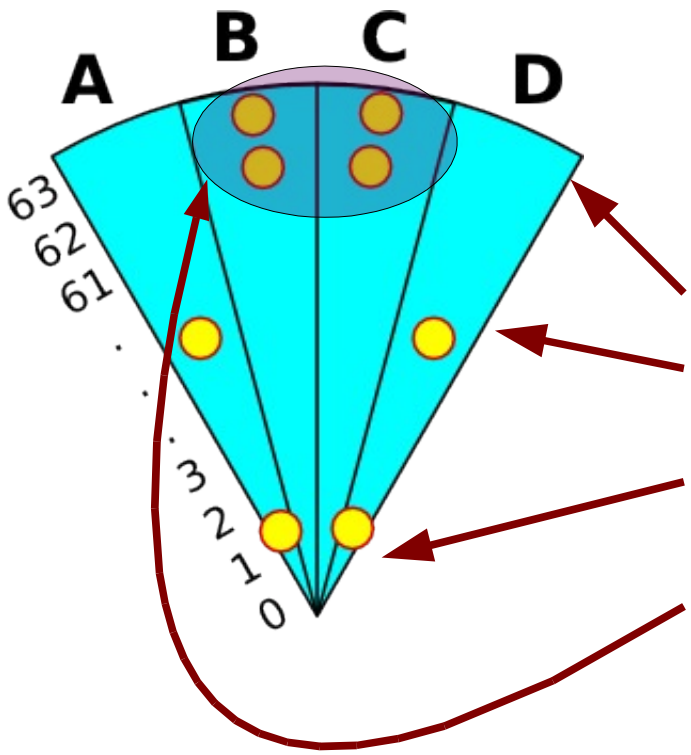
- Can we organize a few tens of channels in a way to do some useful **checks of detector performance** ?
- Can we **read all** those **channels** simultaneously without having multichannel ADC ?

- Is it worth to spend time and resources for such try ?
- Should not we rather try to complete the design and submit the front-end and multichannel ADC (e.g. 16 channels ?)
- How much time would it take ? (9/12/15 months ?)

- **how should we go ???**



Sensor and fanout test configurations

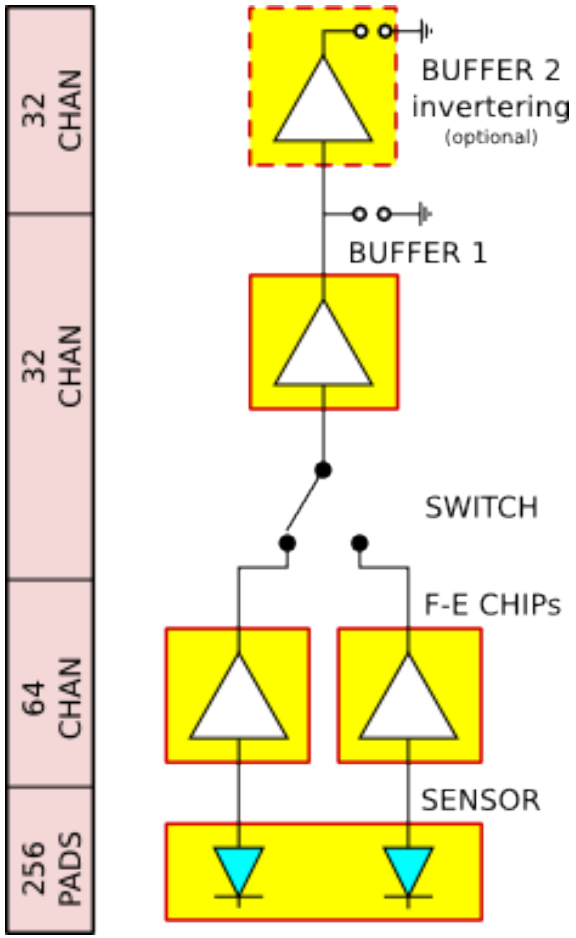


- 2 fanout types:
  - normal (A&B)
  - interlaced (C&D)
- Chosen channels (64 in total):
  - Large Cap (short fanout) (2x16)
  - Medium Cap (medium fanout) (2x8)
  - Small Cap (long fanout) (2x8)
- 32 channels close to each another can be readout simulateously

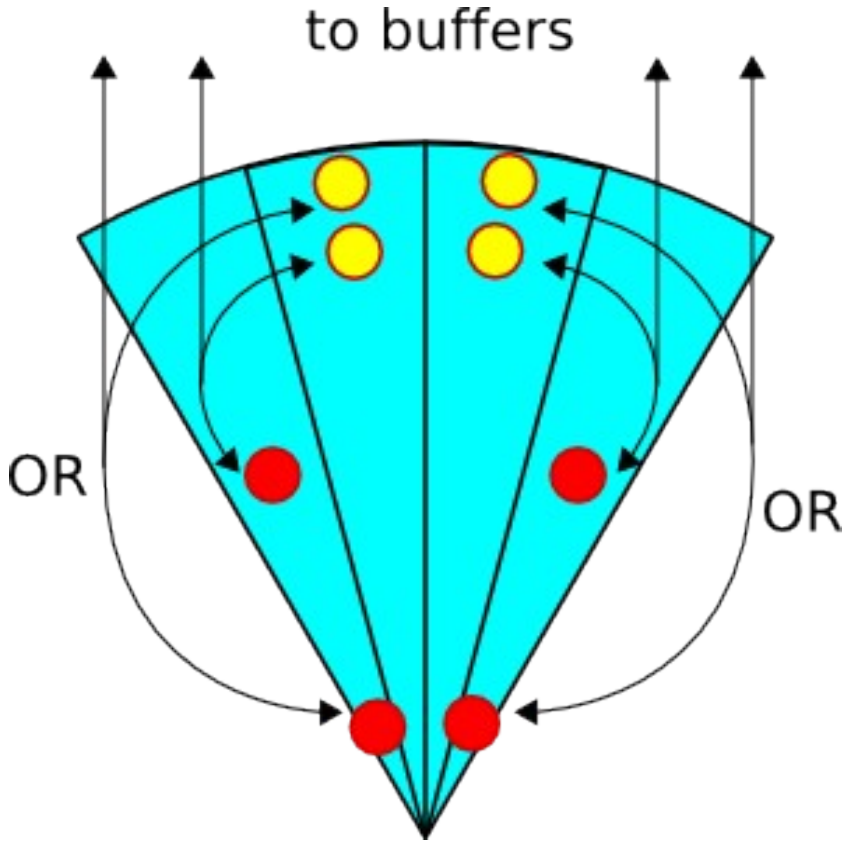
→ test beam area ?

Each yellow dot means :
1 ASIC CHIP (8 channels)

Read out chain

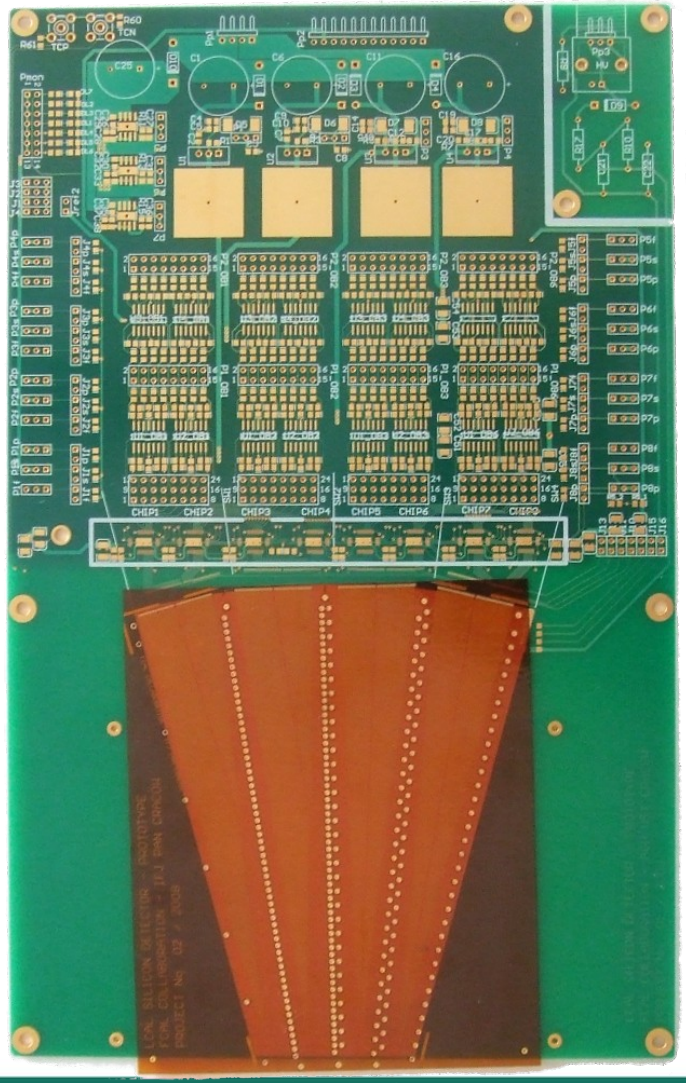


Read out chain



Switches configurations

PCB board ready



- 4 board just arrived (not mounted jet)
- kapton fanouts available (provided by IFJ KRAKOW)
- 28 front-end ASICs left

Technical informations

- There is power supply and distribution block on board (only 2 voltages are needed + one HV for sensors)
- Each chip has its own independent biasing circuit
- Front-end gains are switchable (both preamplifier and shaper)
- Overall gain can be changed via output buffers gain
- There are 2 test pulses inputs (even/odd)

Open issues (test setup)

- What DAQ will follow the PCB board (analog output)?
  - Multichannel integrating ADC (DESY one)
    - We have one(two ?) in hand
    - There is software which can be a starting point ..
    - additional ADC integration reduces noise level
    - delay lines have to be used? (for timing issues)
  - Multichannel ADC (e.g. VME - V1740)
    - Similar to final design
    - We don't have one (cost ?)
  - Wait for multichannel ADC ASIC ?
    - Time needed
- What will triger the DAQ ?

Open issues (physics)

- What do want to test/measure during test beam ?
  - Position resolution ?
  - Alignment ?
  - High performance rate ?
  - Molier radius
  - ???
- How do we want to do ?
  - Geometry /mechanical design ?
  - Absorber ?
  - Number of layers ? (various ?)
- What kind of beam do we need ?
  (DESY / CERN / Darmstadt)
- No ideas / conclusion on this topic ...

Summary

- Board was prepared to understand if front-end chips are able to manage sensors
- 4 boards available, 28 front end ASICs left
- Open issue is if board can be used for detector study (during test beam)
- DAQ following the board is needed