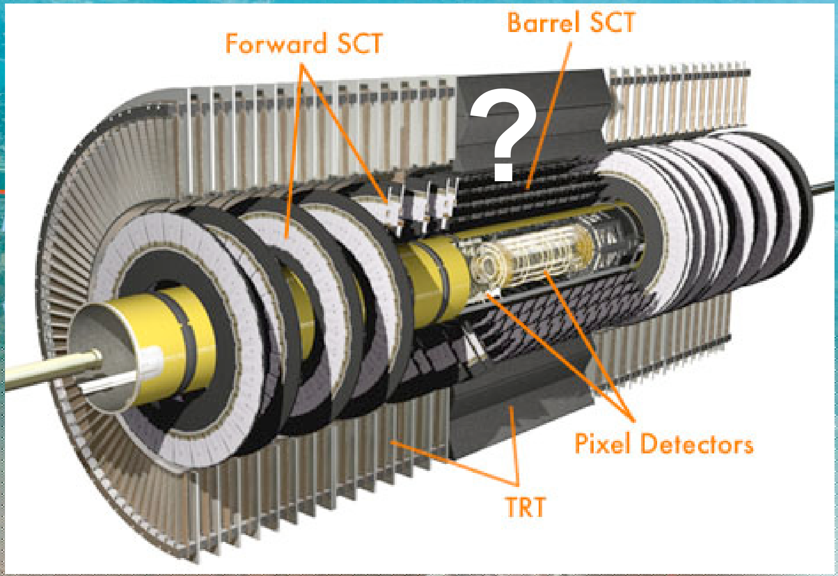
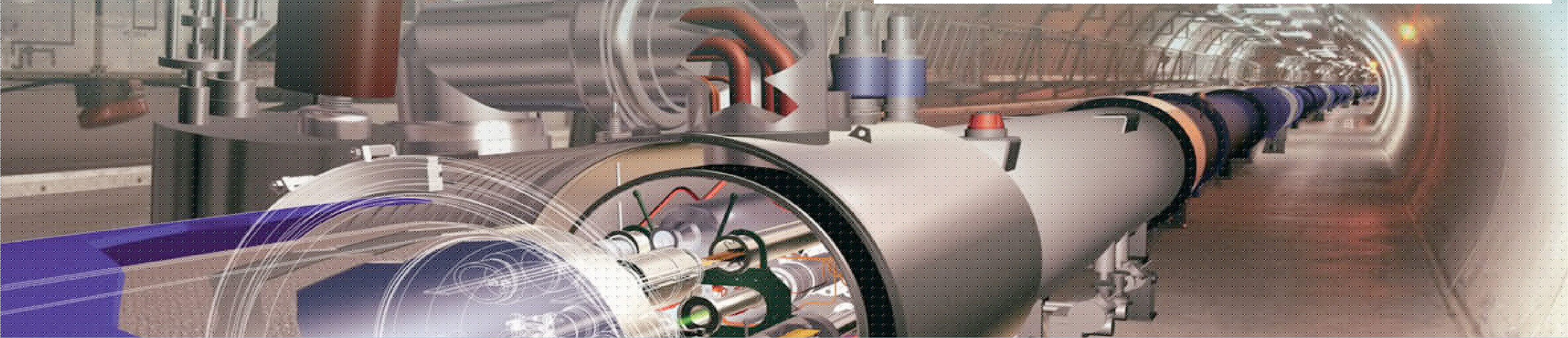
Summary of

ATLAS TRACKER UPGRADE WORKSHOP

Liverpool, December 06-08, 2006

Peter Kostka





The European strategy for particle physics

http://council-strategygroup.web.cern.ch/council-strategygroup/

"The LHC will be the energy frontier machine for the foreseeable future, maintaining European leadership in the field; *the highest priority is to fully exploit the physics potential of the LHC, resources for completion of the initial programme have to be secured such that machine and experiments can operate optimally at their design performance.* A subsequent major luminosity upgrade (SLHC), motivated by physics results and operation experience, will be enabled by focussed R&D; *to this end, R&D for machine and detectors has to be vigorously pursued now and centrally organized towards a luminosity upgrade by around 2015.*"

ATLAS High Luminosity Upgrade Tracker Workshop

Liverpool

6th – 8th December 2006

Web page: http://www.liv.ac.uk/physics/AHLUTW

Chairperson: Phil Allport

Conference Coordinator

Mrs Jackie Sharp

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High Energy Physics Group

Department of Physics

University of Liverpool

Liverpool L69 7ZE UK

Introduction

ATLAS Tracker Upgrade Workshop

Date/Time: from Wednesday 06 December 2006 (09:00) to Friday 08 December 2006 (16:00)
Location: Liverpool University Foresight Centre
Chairperson: Phil Allport (U. of Liverpool) Secretary Coordinator
Contact: j.sharp@liv.ac.uk
Description:
Following the success of the Genova ATLAS Tracker Upgrade Workshop in July 2005 a further workshop is being held.
This will run from 6th to 8th December 2006, hosted at the University of Liverpool's Foresight Centre.
A number of working groups have also requested rooms in the Physics Department for pre-meetings on the morning of 6th December.
The Workshop itself starts on Wednesday 6th December at 13:00 with lunch provided.

Material: Conference Venue; Workshop Home Page - http://indico.cern.ch/conferenceDisplay.py?confId=a063014

Wednesday 06 December 2006 09:00->12:50	ATLAS 3D Sensor R&D Meeting
Wednesday 06 December 2006 09:00->12:45	Electronics Meeting
Wednesday 06 December 2006 09:30->11:50	Thermal Management Working Group Meeting

Wednesday 06 December 2006 14:00->15:30	Organisation ()
Wednesday 06 December 2006 16:00->17:45	Layout and Simulation ()
Thursday 07 December 2006 08:30->13:00	Module Integration Session ()
Thursday 07 December 2006 14:00->17:40	Engineering ()
Friday 08 December 2006 08:30->13:00	Sensors and Electronics ()
Friday 08 December 2006 14:00->16:00	Services, Irradiation and Wrap Up ()

Disclaimer

- *I tried to extract some of main information's which might be of common interest - discussion about DESY participation in R&D project for the ATLAS upgrade.*
- *Steiner Stapnes has given a summary already at the end of the workshop - had to extent & shortened*
- *It was my first ATLAS meeting -*
  - *I might have misunderstood some of the facts presented*
  - *I do not even try to cover all topics discussed there*

Outline (1)

- ***Organisation***
  - ***News from the machine (bunch spacing, low β - hardware ...)***
  - ***LAr forward region - impact of high luminosity; modifications/upgrade - necessary/possible (?)***
  - ***Steering group - Status of R&D, timetable 2007***
- ***Layout & Simulation***
  - ***Layout versions ⇔ material, services (not compromising functionality)***

    - innovations unavoidable
  - ***Simulation (material, performance ...) - some progress, FATRAS (MPI); Full simulation and reconstruction needed;***
    ⇒ pixel layout provides improvements, thin Si sensors!

    ⇒ new support structures
- ***Module Integration - Inner Layers (Pixel)***
  - ***Elimination of inefficiencies - active edge silicon detectors (thinner)***
  - ***Development: thinner, new interconnection of FE-electronics - sensors; trend 3D structures: less material, less power consumption, faster R/O;***
    - following the progress of chip makers, using new technologies
  - ***GOSSIP: a new and potentially better vertex detector for ATLAS***

Outline (2)

- ***Module Integration - Inner Layers (Strips)***
  - ***New concepts of sensor integration, self-supporting stave structures***
  - ***Power supply: DC-DC near the sensors - new industrial developments; serial powering of staves***

- ***Engineering***
  - ***Radius of beam pipe probably unchanged - innermost pixel layer***
  - ***UHM fibre/foam support structure; outstanding property - cooling***
  - ***Cooling - hot issue***

- ***Sensors and Electronics***
  - ***ASIC's design on new level of standardisation - e.g. tracker & LAr R/O; CMS co-operation (other partners?!);   Very essential: costs!
Man power needed urgently for architecture design, controllers, protocol design***
  - ***3D pixel collaborators - good progress - 6 EOI - new groups joining; radiation hard, fast, highly integrated structures, time-table***
  - ***SSP group with new results***

Introduction

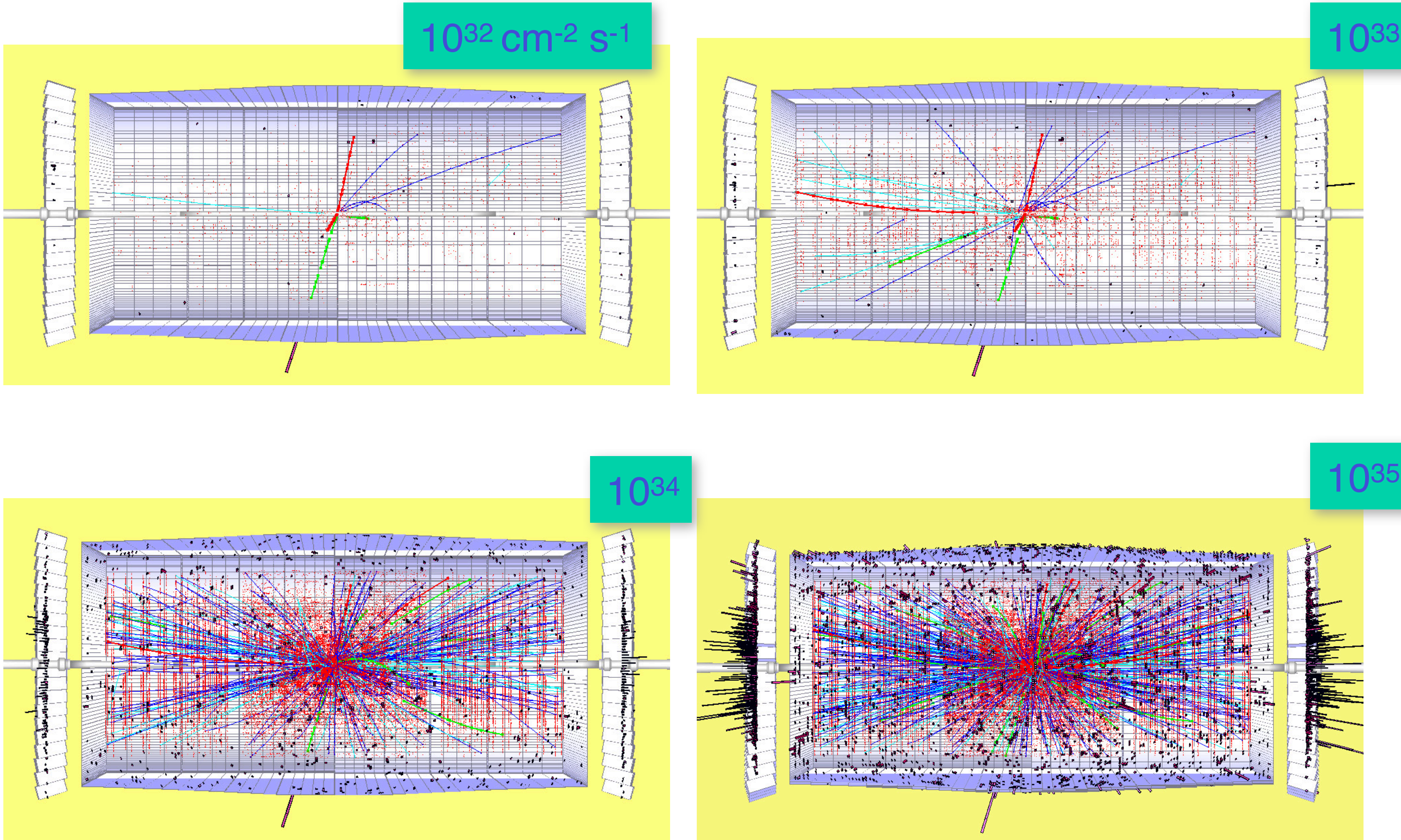
- ***The LHC upgrade to SLHC***
  - ***10^{35} cm^{-2} s^{-1} peak luminosity***
  - ***~1000 fb^{-1}/year***

- ***Long preliminary lead time required for machine and for detector R&D***
  - ***Time scale for upgrade of the LHC is around 2015***
  - ***(Sub-)Detectors and machine elements are reaching their effective lifetimes;***
  - ***Some Sub-Detectors have to be replaced earlier: 2011-2012***
  - ***Time scale for decreasing statistical errors becomes very long***

- ***Basic idea of the machine upgrade***
  - ***Increase the current in the machine***
  - ***Increase the focusing (β^* from 0.5 m to 0.25 m)***
  - ***Change optics to avoid parasitic beam interactions***

- ***Would likely require a long shutdown***
  - ***Time enough for new optics for the IR***
  - ***Also gives time for replacement of tracking detectors and other required upgrades***

CMS from LHC to SLHC



I. Osborne

J. Nash, *CMS SLHC Upgrades, 12 Oct. 2006*

Machine and Organisation

ATLAS Tracker Upgrade Workshop

Wednesday 06 December 2006

Organisation (14:00 ->15:30)

Chairperson: Marzio Nessi (*CERN*)
Location:

14:00	Welcome and Introduction (10') (Slides)	Phil Allport (*U. of Liverpool*)
14:10	Summary of LHC Proposals (20') (Slides)	Per Grafstrom (*CERN*)
14:30	Project Office Report (25') (Slides)	David Lissauer (*Department of Physics*)
14:55	Review Office (15') (Slides)	Mike Tyndel (*Particle Physics*)
15:10	Steering Group Report (20') (Slides ; Slides - original ; Slides - ppt)	Nigel Hessey (*NIKHEF*)

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zoom on heat load

parameter	symbol	nominal	ultimate	12.5 ns	25 ns, smaller β*	50 ns, long
SR heat load 4.6-20 K	P_{SR} [W/m]	0.17	0.25	0.5	0.25	0.36
image current heat	P_{IC} [W/m]	0.15	0.33	1.87	0.33	0.78
total BS heat load w/o e-cloud	P_{SR} + P_{IC} [W/m]	0.32	0.58	2.37	0.58	1.14
local cooling limit*	P_{cool} [W/m]	2.4	2.4	2.4	2.4	2.4
cooling remaining for e-cloud	$P_{cool, rest}$ [W/m]	2.08	1.82	0.03	1.82	1.26
simulated e-c heat for SEY=1.4 (1.3)	P [W/m]	1.07 (0.44)	1.04 (0.6)	13.34 (7.85)	1.04 (0.59)	0.36 (0.1)

* L. Tavian, LUMI'06

Not feasible

OK

The Valencia meeting

My simplified conclusions

- Heat load & cooling capacity
  - rule out some of the scenarios considered earlier
- Our message understood:
  - max integrated luminosity and not max peak luminosity
  - "min" instantaneous Luminosity (pile-up)

⇒ Two new baseline scenarios

- 25 ns small beta (0.08 m)

  keep the current acceptable low by getting most of the luminosity from a very small ß
- 50 ns long bunch (0.25m)

  Keep the current acceptable low by less electron cloud and fewer bunches

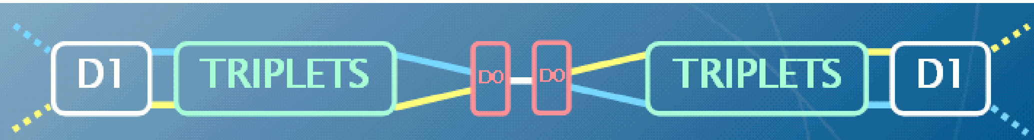
Per Grafstrom, ***Summary of LHC Proposals***

Hardware needed for these two scenarios

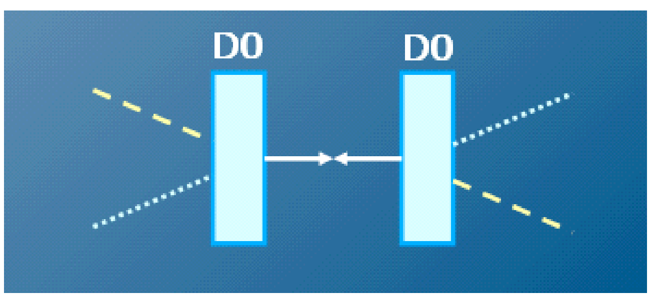
- 25 ns small ß (8 cm)
  - New triplet with bigger aperture (L* =23m)
  - Small angle crab cavity (~100 m from IP)
  - D0 needed
  - If NbTi technology Qo is needed
  - If Nb_3Sn technology no Qo needed
- 50 ns long bunch
  - New triplet with bigger aperture (L*=23 m)
  - No D0 needed
  - Both NbTi and Nb_3Sn possible without need for Qo
  - Wire compensation needed (~100 m from IP)

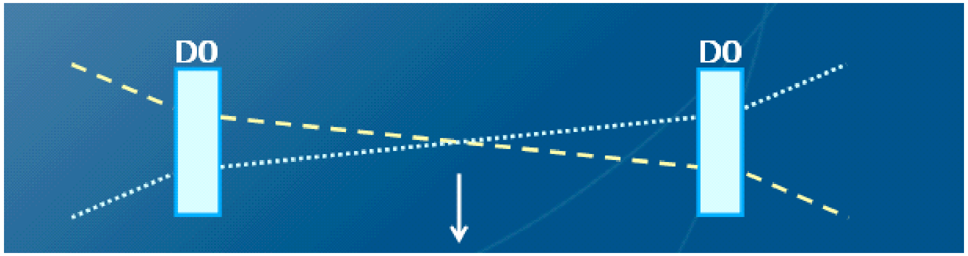
Per Grafstrom, ***Summary of LHC Proposals***

Early separation schemes - D0 inside ATLAS



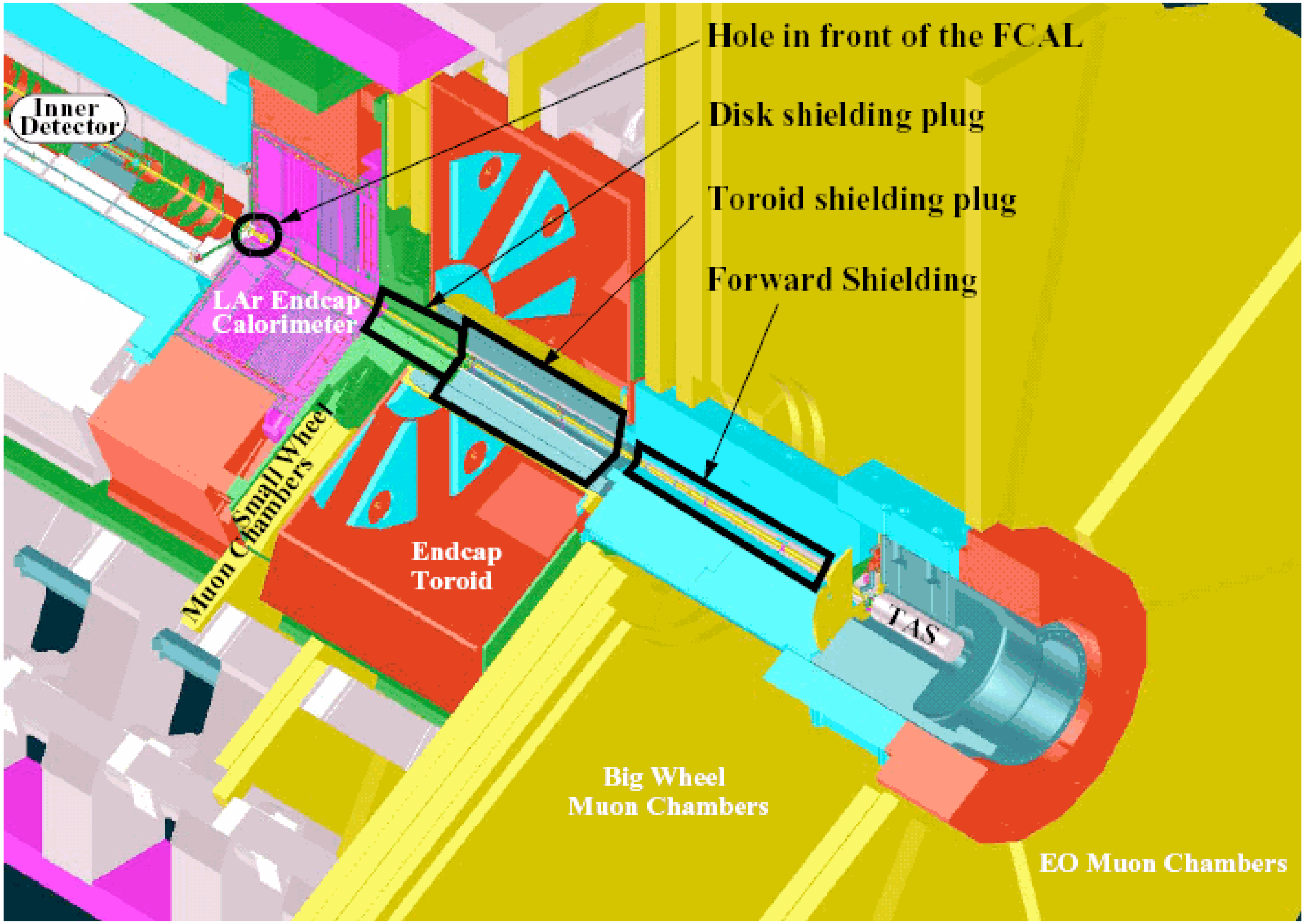
- Allow a vanishing crossing angle at the IP using a dipole on each sides of the IP: the D0
- PROS
  - simple, cheap, local change, transparent to the rest of the machine.
- CONS
  - intrusion of magnetic element in the detectors
- Two possible implementations
  - the Full Early Separation scheme (FES)
  - the Partial Early Separation scheme (PES).





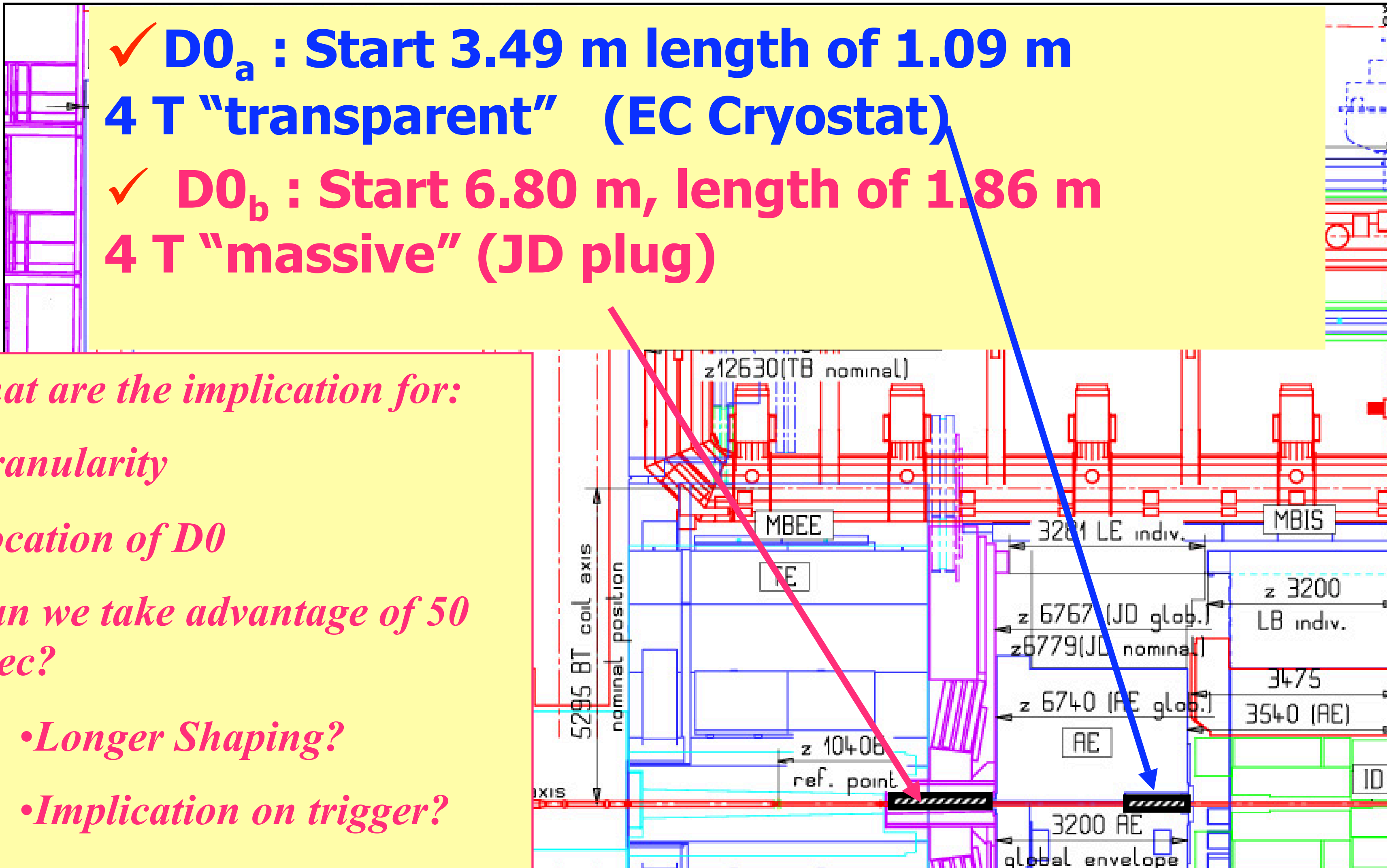
Per Grafstrom, *Summary of LHC Proposals*

Slim magnets inside ATLAS



Per Grafstrom, *Summary of LHC Proposals*

Possible Location of D0 in ATLAS



✓ $D0_a$: Start 3.49 m length of 1.09 m
4 T “transparent” (EC Cryostat)

✓ $D0_b$: Start 6.80 m, length of 1.86 m
4 T “massive” (JD plug)

What are the implication for:

- *Granularity*
- *Location of D0*
- *Can we take advantage of 50 n-sec?*
    - *Longer Shaping?*
    - *Implication on trigger?*
    - *Pipeline length?*

D. Lissauer, ***Project Office Report***

Relevant parameters for us in the two scenarios

	25 ns small	50 ns long
Bunch spacing:	25 ns	50 ns
Rms bunch length:	7.55 cm	14.4 cm
Long. Profile:	Gauss	Flat
Luminous region:	2.5 cm	3.5 cm
Peak lumi:	$15.5\ 10^{34}$	$8.9\ 10^{34}$
Events crossing:	296	340
Lumi. Life time:	2.1 h	5.3 h
Effective lumi : (10 h turn around)	$2.4\ 10^{34}$	$2.3\ 10^{34}$
Effective lumi: (5 h turn around)	$3.6\ 10^{34}$	$3.1\ 10^{34}$

Per Grafstrom, ***Summary of LHC Proposals***

Machine Upgrade News

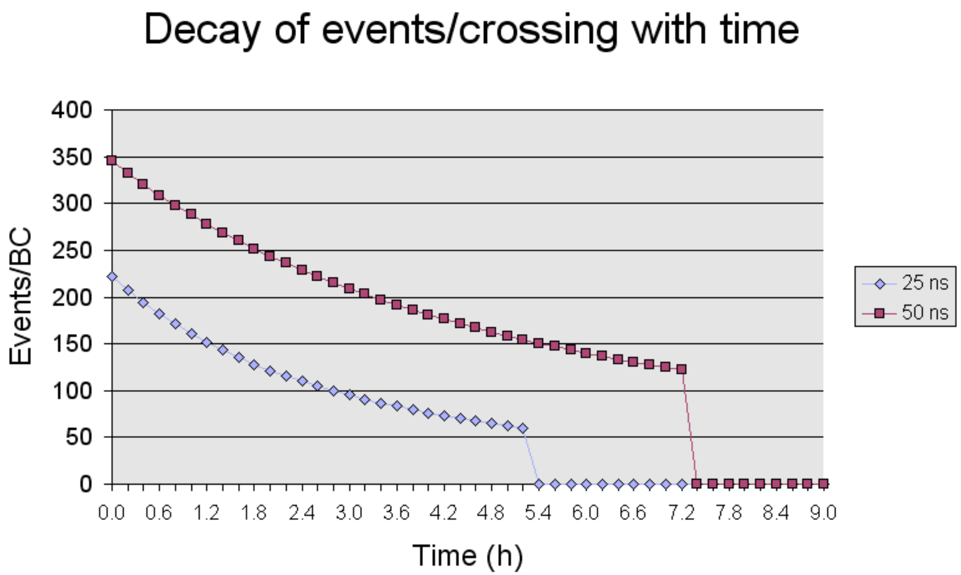
zoom on decay time & integrated luminosity for various options

parameter	symbol	nominal	ultimate	12.5 ns	25 ns, smaller β^*	50 ns, long
max. # events / crossing		19	44	88	296	340
peak luminosity	L [1e34 cm-2s-1]	1	2.3	9.2	14.4	8.9
effective beam decay time	τ_{eff} [h]	45	29	14.4	4.6	10.7
effective luminosity ($T_{turnaround}$=10 h)	L_{eff} [10^{34} $cm^{-2}s^{-1}$]	0.46	0.91	2.7	2.4	2.3
	$T_{run,opt}$ [h]	21.2	17.0	12.0	6.5	10.3
effective luminosity ($T_{turnaround}$=5 h)	L_{eff} [10^{34} $cm^{-2}s^{-1}$]	0.56	1.15	3.6	3.6	3.1
	$T_{run,opt}$ [h]	15.0	12.0	8.5	4.6	7.3
	Average events/bc				150	208

Per Grafstrom, *Summary of LHC Proposals*

Further comparison (Nigel Hessey)

	25 ns small ß	50 ns long bunch	25 ns small ß'
Peak lumi:	15.5 10^{34}	8.9 10^{34}	11.7 10^{34}
Events crossing:	296	340	223
Lumi. Life time:	2.1 h	5.3 h	2.8 h
Effective lumi:	3.6 10^{34}	3.1 10^{34}	3.1 10^{34}



Nigel version for
"honest" comparison
ß from 8 cm to 11 cm
(turnaround 5 h)

Per Grafstrom, *Summary of LHC Proposals*

Conclusions

- The 12.5 ns scenario seems to have left the scene (for how long?)
- The 75 ns scenario pushed backwards
- Two new scenarios appears in the front
  - 50 ns long bunch 340 evt/bc (at start of fill)
  - 25 ns high ß 223-296 evt/bc

Keep doors open and remember that we do not know (yet) σ_{tot} at LHC .

(some theoreticians say anywhere between 100 and 150 mbarn!)

Per Grafstrom, ***Summary of LHC Proposals***

LAr R&D Update

- ✓ One day workshop at CERN to define LAr upgrade- plans held Dec 4th.
- ✓ Emphasis on the R&D Program needed to define the issues and possible solutions for the Forward region.
- ✓ Issues (In the forward region)
  - → Protection resistors (In the cold) might have to be changed.
  - → Space charge effects (Reduce effective HV on the Gap)
  - → Boiling – bubbles → Sparks ⇐ high luminosity impact
- ✓ Radiation Resistance in the forward region:
  - → GaAs HEC Preamplifiers: built-in margin
  - → To be replaced if radiation strongly under-estimated LAr
- ✓ Prepare R&D plans for upgrade of the readout electronics
  - → Expects expression of interest ~ end of the year.

Can we intervene in the EC calorimeter?

What can be done without disturbing the EC

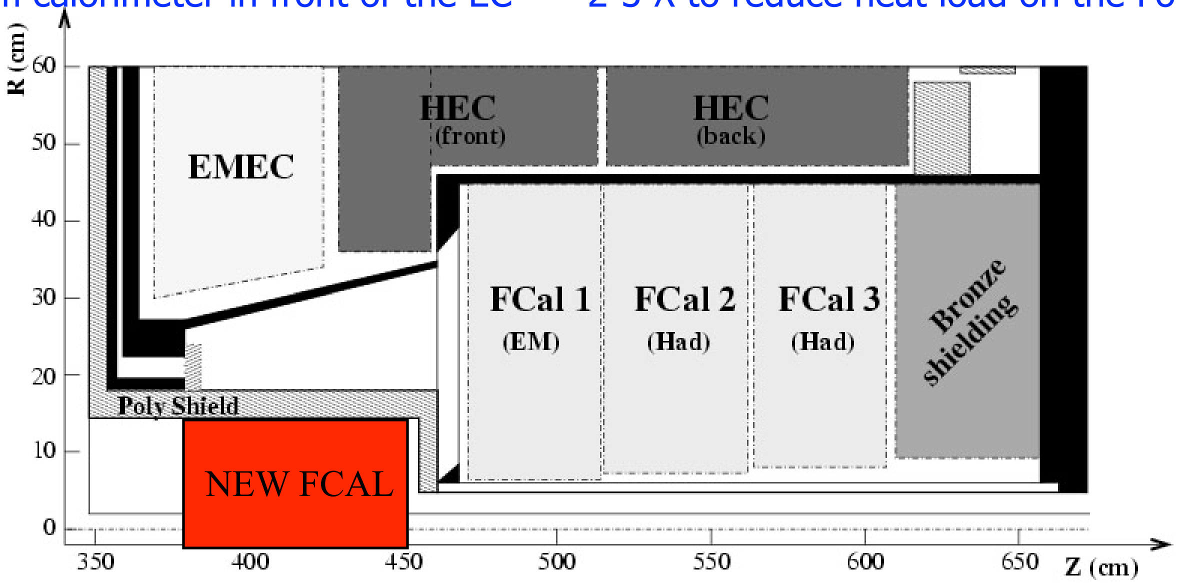
D. Lissauer, ***Project Office Report***

LAr R&D Update

- Intervention in the EC Calorimeter
  - → Is it possible to open EC in the Pit?
  - → Is it possible to open the EC in building 180?
  - → Is it possible to bring the full assembly to the surface?

- Rough time estimate for the above operations is now under study.
  - → Marzio gave a first rough estimate – 2.5-3 years – looks tough!!!

- What if we can not open the EC calorimeter?
  - → Degradation of the EC calorimeter performance – needs simulations
  - → Add a warm calorimeter in front of the EC - ~ 2-3 λ to reduce heat load on the Forward calorimeter.



D. Lissauer, *Project Office Report*

Conclusions

- ATLAS and Technical Coordinator top priority is to complete the present detector
- Upgrade activities have started
- Muon, Tile, Trigger plans still are evolving and we need to understand the implications on the Schedule/cost etc.
- Key people are still missing for many PO/Upgrade activities. Groups/people who are interested willing to participate in upgrade activities should make contact ASP.
- Aim to maximize the overlap between Maintenance and operation activities and the Upgrade!!!

D. Lissauer, *Project Office Report*

Status of R&D Projects

- Approved by EB:
  - Opto-electronics, ABC-Next, Radiation background
- Approved by USG and to be sent to CB:
  - Staves, Strip detectors, SiGe
- Expressions of Intent received:
  - 3D sensors, Modules, Powering, Gossip, High-rate Straw Tracker

Integrated Luminosity Goal

- Although peak luminosity is 10 times nominal, efficiency is lower
  - --> annual integrated L not 10x
      - (10 times LHC ATLAS goal would be 7300 fb-1)
  - Expect about 500 fb-1 per year max
    - Less at first!
  - Stick to 3000 fb-1 for now
    - ~8 years to achieve, including ramp up
  - Safety factor of 2 for design/choice of components
    - Uncertainty in pp cross section, background rate modelling, qualification process (annealing etc.)

Nigel Hessey, *Steering Group Report*

Preview time-table

Upgrade PO

				Next action	
2006					
Nov	Thermal management	Preview	21/11/06	Follow-up	Mid 2007
Dec					
2007					
Jan	LUCID		30/01/06(tbc)	Agenda	
Feb	Sensors (incl. 3D)	Preview		Fix date	
Mar	FE Electronics	Preview & ASIC FDR			
Apr	Modules	Preview			
May	Readout system				
Jun	Power system				
Jul	Mech. support				
	Th. Man. Follow-up				
Aug					
Sep					
Oct	b-layer upgrade				
Nov					
Dec	ATLAS services & envelopes				

M. Tyndel, *Review Office*

Machine and Organisation

- Machine moving towards 50ns – with reduced changes to our forward region (and we might well need some of this space to solve our own problems)
- Most likely they do not need a long shutdown, and most likely the lum. upgrade can be more gradual than foreseen so far – adding uncertainty to our timescale
- We need to simulate 340 min bias overlaps
  - With a set of standard physics channels
- Probably too early to trust that 25 ns is not coming back in next round
- Design for 3000 fb-1 plus factor 2 safety

Layout and Simulation

ATLAS Tracker Upgrade Workshop

Wednesday 06 December 2006

Layout and Simulation (16:00 ->17:45) — **Chairperson:** Nigel Hessey (*NIKHEF*) **Location:**

16:00	**Layout Options** (25') (Slides)	Abraham Seiden (*University of California*)
16:25	**Layout Software Update** (15') (Slides)	Jeffrey Tseng (*Nuclear Physics Laboratory*)
16:40	**Lessons from b-tagging Performance of ATLAS Pixel Layout** (15') (Slides)	Alexandre Rozanov (*Faculte des Sciences de Luminy*)
16:55	**Vertexing with Inner Detector** (15') (Slides)	Vadim Kostyukhin (*Istituto Nazionale di Fisica Nucleare (INFN)*)
17:10	**ATLAS Inner Tracker Layout Studies for the SLHC Based on FATRAS** (15') (Slides)	Oliver Kortner (*Max-Planck-Institut für Physik München*)
17:25	**EndCap Layout** (20') (Slides)	Carmen Garcia (*Instituto de Fisica Corpuscular (IFIC) UV-CSIC*)

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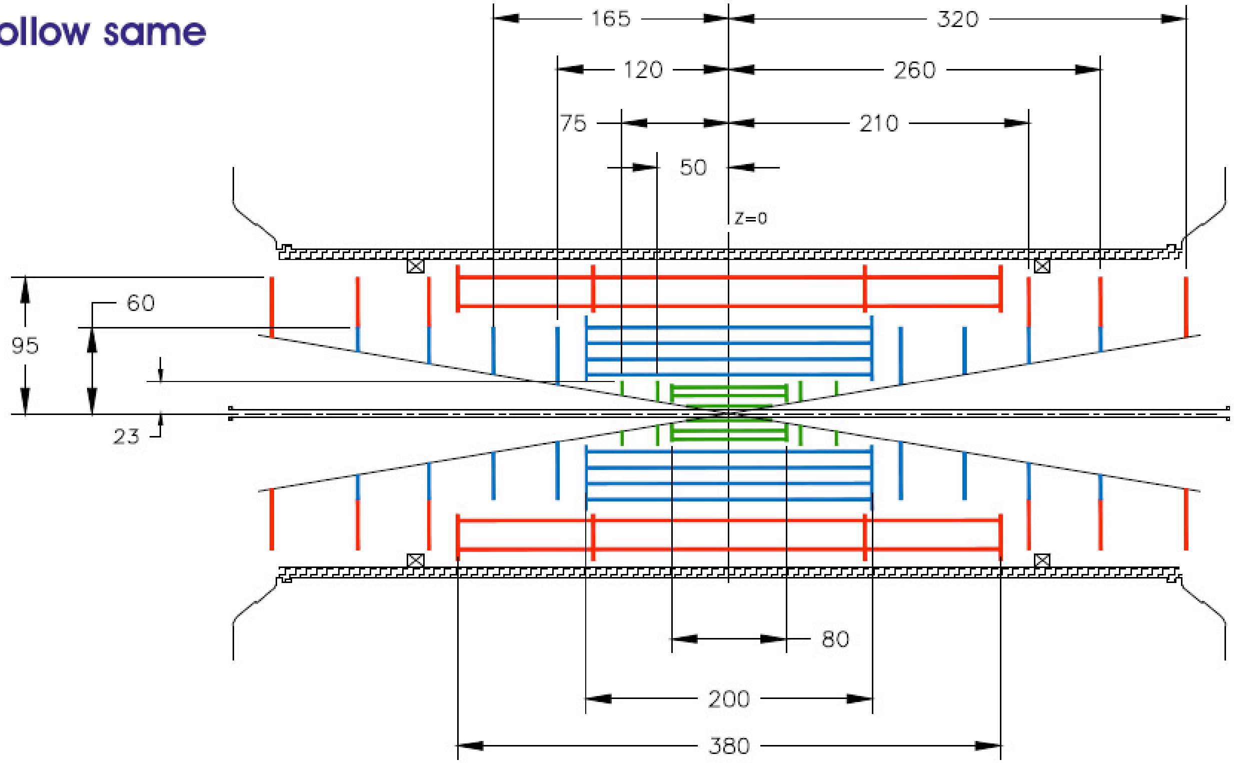
Strawman Layout: Projective Geometry

- Three Pixel Layers (Green) 3-
- Four Short Strip Layers (Blue) 4-
- Two Long Strip Layers (Red) 2
- End Cap disks follow same color schemes

3-4-2 Projective

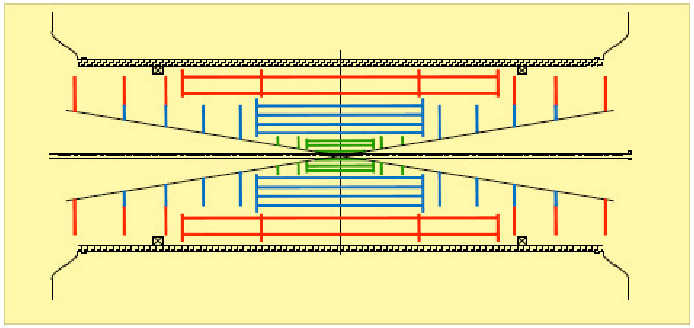


D. Lynn, *Mechanical Support for Barrel Staves*

Some Alternative Layouts

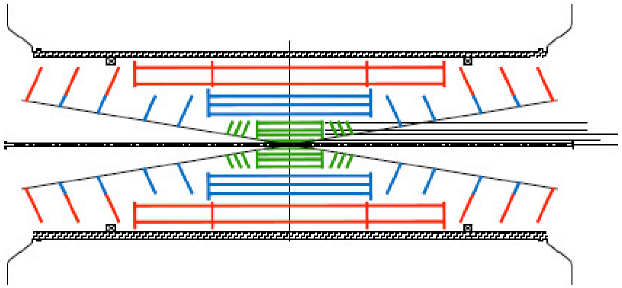
3-4-2 Projective

Long Staves/ Multi-bend Services



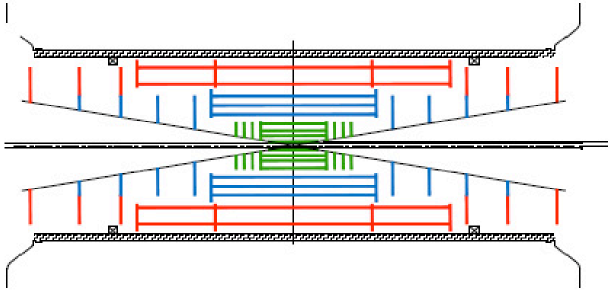
3-4-2 Angled Endcaps

Long Staves/Complex Services/Structure



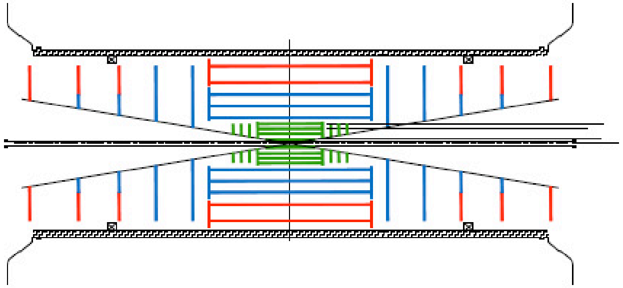
4-3-2 Projective

Long Staves/ Multi-bend Services



4-3-2 SS/LS Fixed Length

Short Staves/ Simpler Services



Barrel structure in the different variants is the same conceptually.
We will update the calculations to the new strawman that emerges from this workshop.

D. Lynn, *Mechanical Support for Barrel Staves*

The layouts have:

9 hits covering 2.5 units of y, using:

3 or 4 pixel layers,

4 or 3 short strip layers (sensor length about 3 cm),

2 long strip layers (sensor length 10 to 12 cm).

Outer radius is 95cm, followed by 5 to10 cm of neutron absorber.

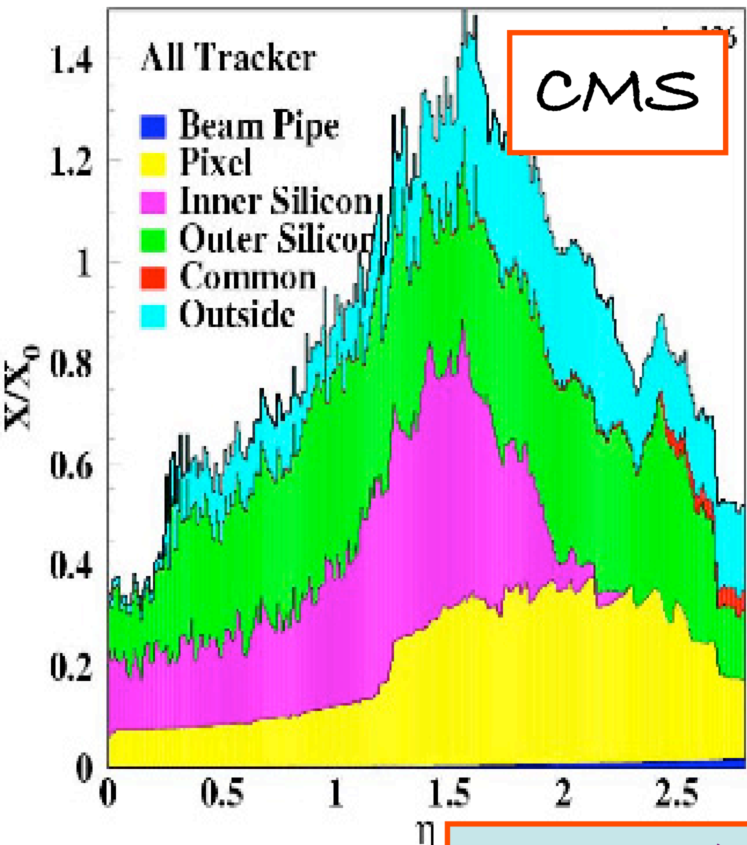
Inner radius is as close as we can get (for vertexing), limited by occupancy and radiation damage.

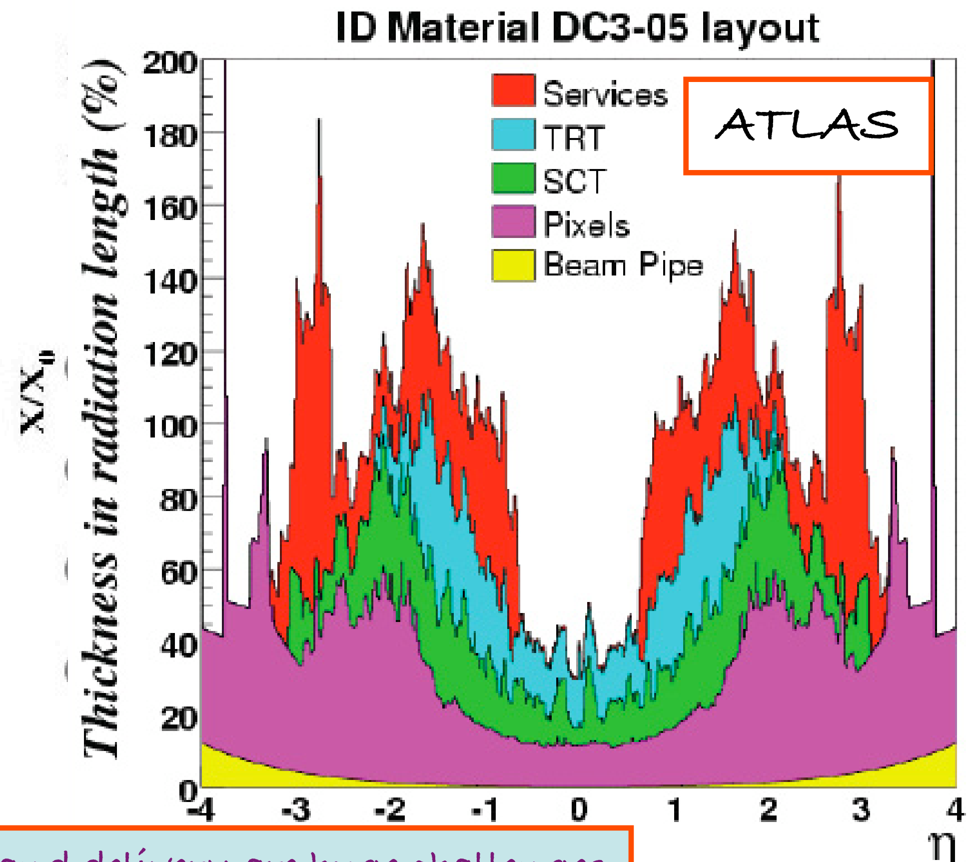
The bunch crossing rate (options are 25 nsec or 50 nsec) is not yet final so the overall granularity of the detector elements is also still uncertain.

It is important to converge on an initial layout (straw-man) to be studied in more detail over the next year.

A. Seiden, *Layout Options*

But...material is not a myth...





Power reduction and delivery are huge challenges
This argues against many pixel layers...

CMS Tracker Upgrade : FNAL Pixel Workshop, October 10, 2006 J. Incandela (UCSB)

Barrel layouts

StrawMan Layout0:

	Technology	Radius(mm)	Pitch(μm)	Eff. Z pitch(mm)	Thickness
b	Pixel	50	50	0.4	3.5%
1	Pixel	120	50	0.4	3.5%
2	Pixel	180	50	0.4	3.5%
3	SS2d (uv)	270	80	2.	2.6%
4	SS2d (uv)	380	80	2.	2.6%
5	SS2d (uv)	490	80	2.	2.6%
6	SS2d (uv)	600	80	2.	2.6%
7	SS1d	700	80	90	2.6%
8	SS1d	950	80	90	2.6%

StrawMan Layout1:

	Technology	Radius(mm)	Pitch(μm)	Eff. Z pitch(mm)	Thickness
b	Pixel	50	50	0.2	3.5%
1	Pixel	120	50	0.2	3.5%
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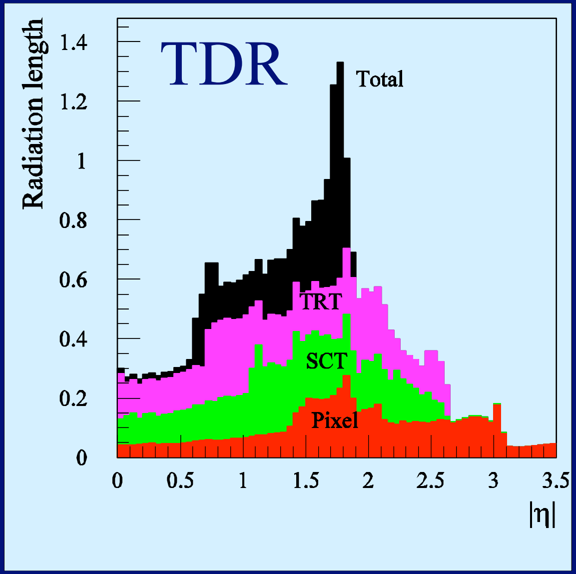
5	SS2d (uv)	490	80	2.	2.6%
6	SS2d (uv)	600	80	2.	2.6%
7	SS1d	750	80	90	2.6%
8	SS1d	950	80	90	2.6%

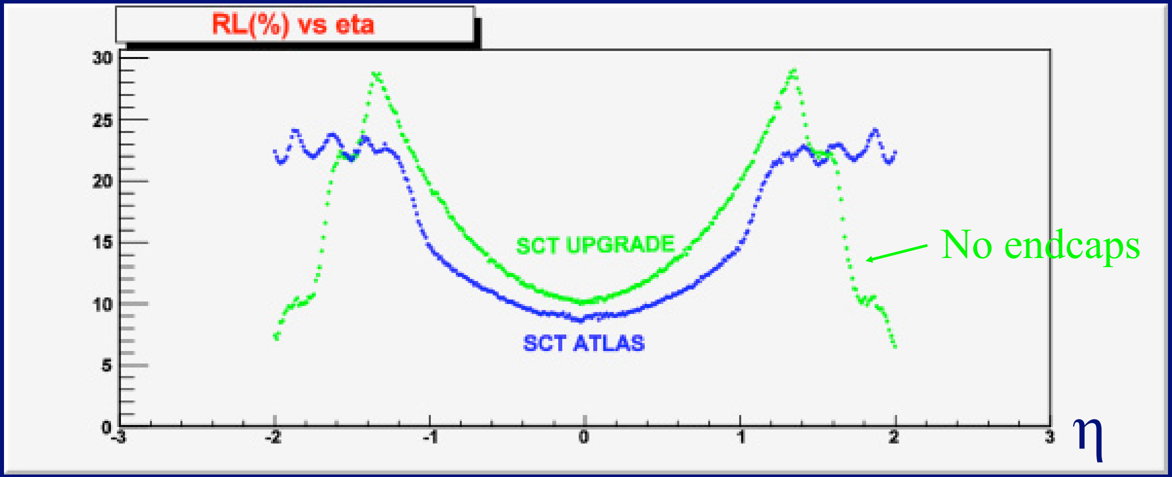
Pixel Layout:

	Technology	Radius(mm)	Pitch(μm)	Eff. Z pitch(mm)	Thickness
b1	Pixel	40	50	0.2	2.6%
b2	Pixel	60	50	0.2	2.6%
1	Pixel	120	50	0.4	3.5%
2	Pixel	200	50	0.4	3.5%
3	Pixel	280	50	0.4	3.5%
4	SS2d (uv)	380	80	2.	2.6%
5	SS2d (uv)	490	80	2.	2.6%
6	SS2d (uv)	600	80	2.	2.6%
7	SS1d	700	80	90	2.6%
8	SS1d	950	80	90	2.6%

- All layouts have beam pipe.
- Radiation thicknesses are taken from current ID simulation

Material distribution



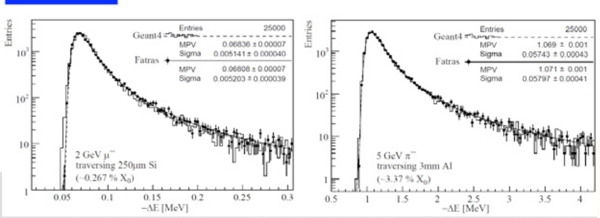


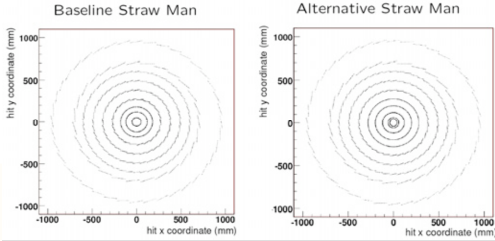
- Comparison of 11.2.0 SCT: lighter than TDR
  - Pixel system left untouched
  - Confirmed by those looking into SCT geometry
- This upgrade adds 10-25% more material
  - One more layer than SCT
- 11.2.0 has been useful for software prototyping, but need more flexibility and control for results

Conclusions

- The fast simulation programme "FATRAS" has been modified to allow for comparisons of different layouts of the inner detector for SLHC.
- The FATRAS programme was shown to be able to predict cluster sizes and occupancies.
- Features of FATRAS:
  - All important physics processes for interactions of particles with matter are included.
  - Easy change of the detector layout.
  - Capability of reading Monte-Carlo generator files.
  - Fast simulation: 1000 tracks in 10 seconds on a 1.4 GHz Intel Centrino processor.

Energy loss





O. Kortner

Lessons from b-tagging at ATLAS

Performance equivalences

- Decrease of the b-layer radius from 5 cm to 4 cm (20% effect)
- Decrease of the z-pitch in b-layer from 400 um to 200 um
- Decrease of the material in b-layer by 0.6%
- Loss of 1% / 2% pixel module/chip inefficiency in b-layer
- Partial (2/3) missing the intermediate pixel layer (R=9cm)
- Pile-up of 10^{34} $cm^2 s^{-1}$ without muon pointing to primary vertex.

Conclusions

- Full simulation and full reconstruction is needed for SLHC design.
  Results can be formulated in the form of derivatives to design parameters
- Continue study of the performance derivatives of ATLAS and Straw-man layouts
- Follow evolution of the physics as new physics may be will need new layout solutions
- High p_T physics may need new approach both in hardware and in the algorithms
- b-tagging performances with pile-up of 10^{35} $cm^2 s^{-1}$ still to be demonstrated

A.Rozanov ATLAS ID Upgrade for SLHC 6-8 December 2006

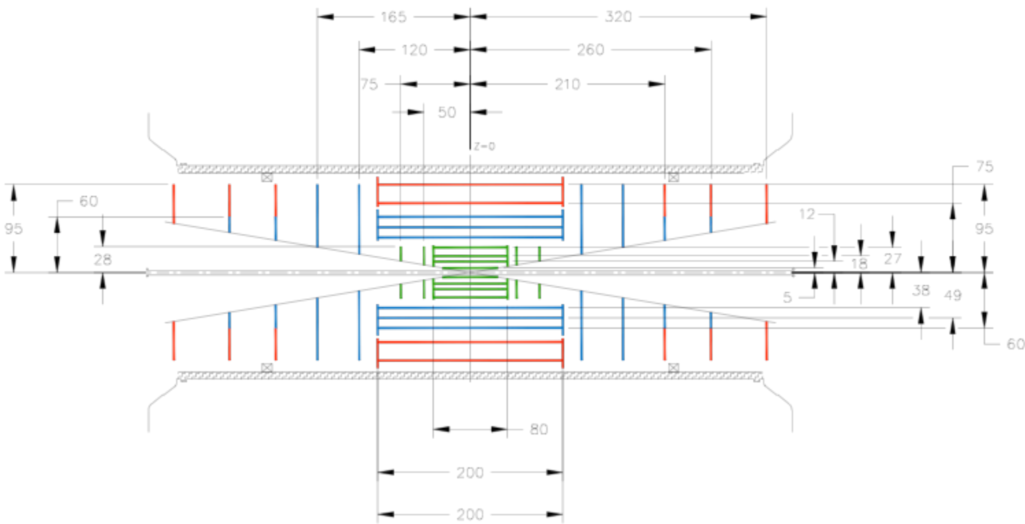
Summary and conclusions

1. Vertexing is important for b-tagging and b-physics.
2. Developed semi-analytical model gives reasonable description of ID tracking resolutions. Model allows to test any proposed layout even with very complicated geometry quite easily.
3. Barrel part of "StrawMan0" layout has performance quite similar to current ID design both for coordinate and momentum resolutions.
4. "Pixel" layout provides a ~30÷40% improvements in Z resolution, ~10-20% improvements in Rϕ resolution with momentum resolution close to "StrawMan0" layout one. "StrawMan1" precisions are between "StrawMan0" and "Pixel".
5. Thinning of Pixel part of ID allows to increase significantly ID resolutions.
6. For any given amount of sensitive layers and their thickness' some optimization of layers positions may give nonnegligible improvement in performance.

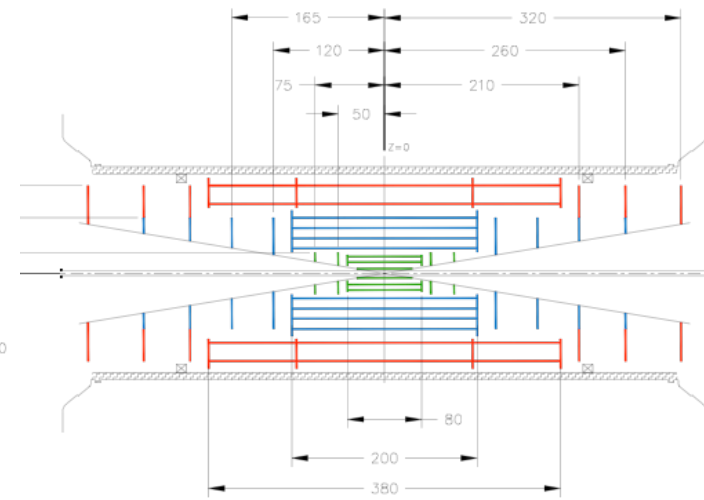
EndCap "Straw-Man" Layouts

- Input for out studies:

Fixed length barrel



Projective barrel



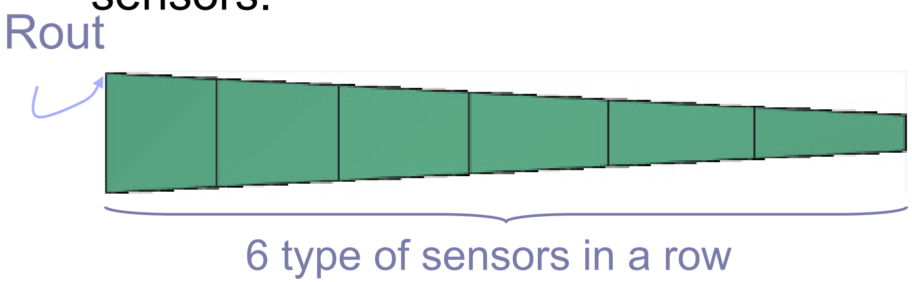
5 disks SS and LS @ z= 320,260,210,185 and 120 cm
Inner-r: η=2.5

Fixed length barrel	Projective barrel
Outer-r: 5 disks @ 950 mm	Outer-r: 3 disks @ 950 mm 2 disks @ 600 mm

Carmen Garcia, ***EndCap Layout***

Staves

- Follow the barrel approach.
- Goal is to investigate how to group the sensors.



Up width (cm)	Bot. width (cm)	height (cm)	pitch (μm)
10,8	9,6	10,3	78,3
9,6	8,3	11,3	68,7
8,3	7,0	12,3	58,2
7,0	5,5	13,1	46,9
5,5	3,9	13,7	35,0
3,9	2,3	14,1	22,7

- Location of the hybrid is an issue since sensors are much narrower at lower radii:
  - For short strips we may need 3x10 ASICs, each of ~0.75 cm^2, which is > 20 cm^2 + hybrid.
  - Still, could one envisage to place them on one side (TAB, double metal layer, ...) ?
- Pitch too small for the inner radii.
- *To mount them with stereo-angle (few cms at the edges) → very few choices left: implement it on the wafer ?.*

Pitch > 50μm to avoid micro discharge at high voltages and charge sharing:

- Change the number of channels (< 1280/wafer)
- Different hybrid for each ring

Carmen Garcia, ***EndCap Layout***

Issues in Layout and Simulation

- Strawman should be adapted – need a reference point for further developments and comparisons
- What strip layers are double sided or single sided?
- Simulation work started with some results
- EC work started

Modules – Inner Radius Layers (1)

ATLAS Tracker Upgrade Workshop

Thursday 07 December 2006

Module Integration Session (08:30 ->13:00)

Chairperson: Phil Allport (*U. of Liverpool*)
Location:

08:30	Multi-Chip-Modules Deposited Experiences Made in the R&D Phase of the ATLAS Pixel Detector (20') (Slides)	Tobias Flick (*Bergische Universitaet Wuppertal*)
08:50	Wafer Level System Integration (30') (Slides)	Ehrmann
09:20	Pixel Module Concepts (20') (Slides)	Mauricio Garcia-Sciveres (*Physics Division*)
09:40	R&D for a Novel Pixel Detector for the SLHC (25') (Slides)	Hans-Günther Moser (*Max-Planck-Institut*)
10:05	GOSSIP: A New and Potentially Better Vertex Detector for ATLAS (25') (Slides)	Harry Van Der Graaf (*NIKHEF*)

Outline (1)

- **Organisation**
  - News from the machine (bunch spacing, low β - hardware ...)
  - LAr forward region - impact of high luminosity; modifications/upgrade - necessary/possible (?)
  - Steering group - Status of R&D, timetable 2007
- **Layout & Simulation**
  - Layout versions ⇔ material, services (not compromising functionality)

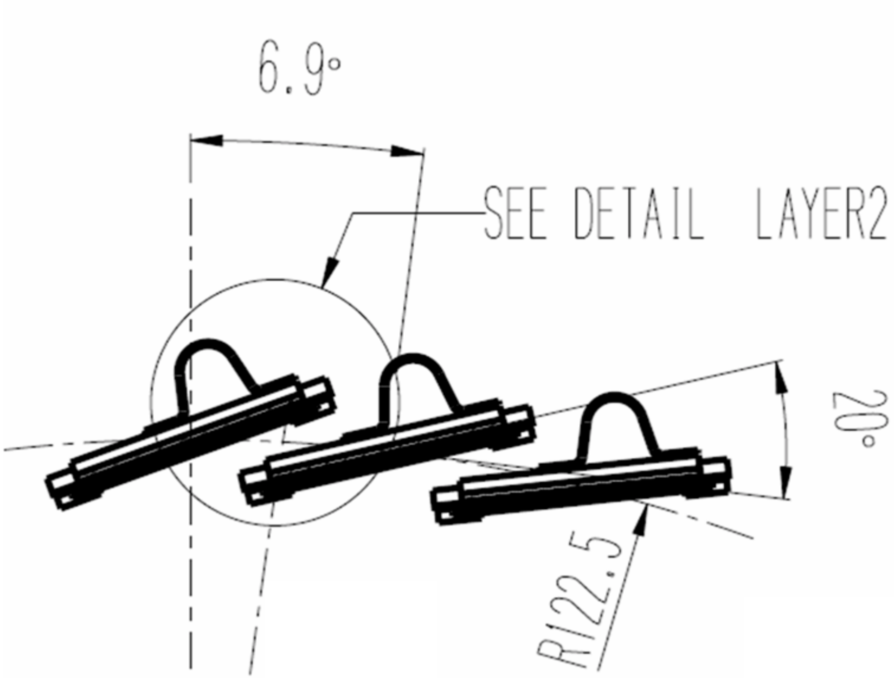
    - innovations unavoidable
  - Simulation (material, performance ...) - some progress, FATRAS (MPI); Full simulation and reconstruction needed;
    ⇒ pixel layout provides improvements, thin Si sensors!

    ⇒ new support structures
- **Module Integration - Inner Layers (Pixel)**
  - Elimination of inefficiencies - active edge silicon detectors (thinner)
  - Development: thinner, new interconnection of FE-electronics - sensors; trend 3D structures: less material, less power consumption, faster R/O;
    - following the progress of chip makers, using new technologies
  - GOSSIP: a new and potentially better vertex detector for ATLAS

Issues

- Material & active area coverage
  - There are inefficiencies in the present system caused by the desire to have no acceptance gaps as well as overlaps for internal alignment.
- Cost & speed of assembly
  - Number of sequential steps
  - Complexity
  - Yield requirements and testing
- Focus on modules for barrel use

Present Area coverage (barrel)

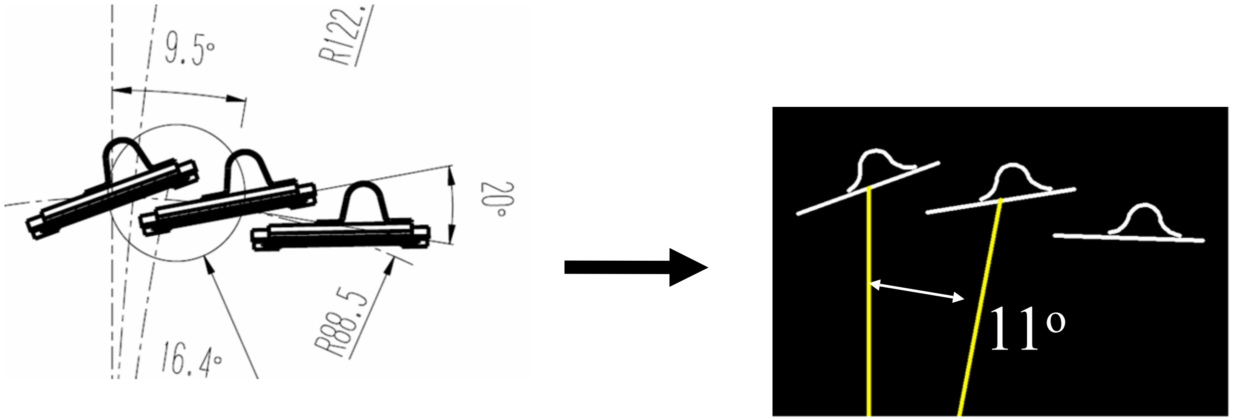


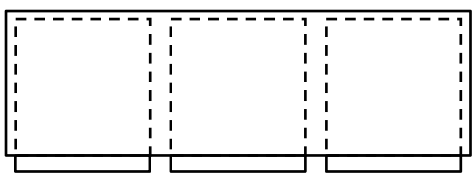
Layer	Z x Sensor width / R.dϕ	Z x Chip width / R.dϕ	1/cosine tilt angle
B	1.34	1.54	1.06
1	1.32	1.52	1.06
2	1.31	1.51	1.06
Z	1.03	0.99	1.00

(Z = factor from overlap along Z)

Effective silicon thickness for 1 layer,
260μ*1.32 + 200μ*1.52 = 680μ

Active edge sensors





- Module looks the same, but there is no dead margin on the sensor perimeter, allowing less overlap.
- Still 2 pixel radial overlap in phi.
- This could be a good baseline starting point.

	NOW	**Big chips**	**Active edges**
Z x Sensor width / R.dϕ	1.32	1.32	1.11
Z x Chip width / R.dϕ	1.52	1.31	1.14
Effective Si thickness	680μ	605μ	515μ

M. Garcia-Sciveres, ***Pixel Module Concepts***

Radical alternatives

- So far have shown incremental changes to present design
- Could also consider completely new directions
- But what more could there be to gain after coverage factor ~1.00?
- Reduce the mechanical support structure by having the active silicon serve mechanical functions.
- Example: the ideal pixel layer:

1-2mm silicon thickness, but provides 2 hits

•A silicon tube, which is active
•Cables attach to outer surface.
•Cooling also on outer surface.

- A not yet proposed assembly concept shown in appendix
- "Reasonable" only for small radius (4cm or less- less is better).

Radical alternatives

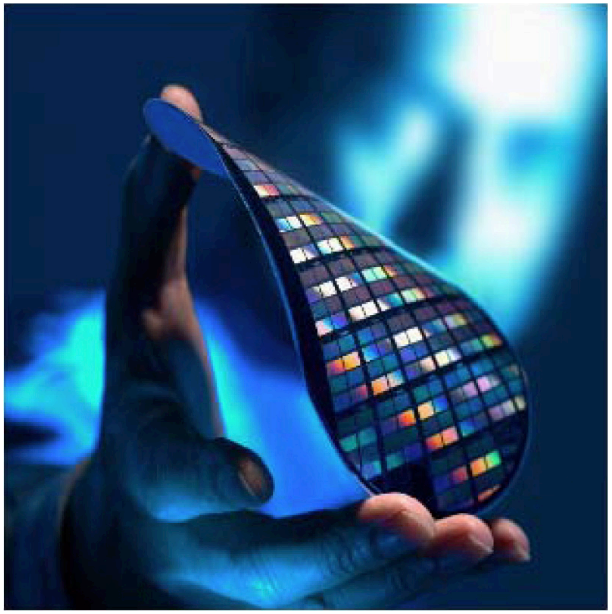
- So far have shown incremental changes to present design
- Could also consider completely new directions
- But what more could there be to gain after coverage factor ~1.00?
- Reduce the mechanical support structure by having the active silicon serve mechanical functions.
- Example: the ideal pixel layer:
- Next round of pixel modules can build on present generation by removing inefficiencies.
- Expect larger chips.
- Active edges seem like a key development.
- Fabrication process can be greatly simplified and better automated to allow covering larger areas with pixels.

Future Requirements:
Thin Silicon & New Interconnect Technologies

O.Ehrmann, *Wafer Level System Integration*,
TU-Berlin, Frauenhofer Institut IZM Berlin

Silicon becomes flexible when thickness is reduced down to less than 30µm

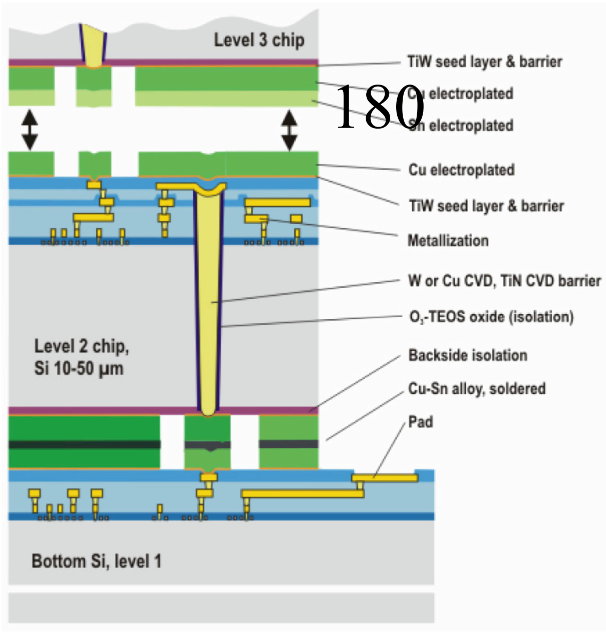
- bending radius 1mm / 1µm thickness
- fully flexible and ultra thin systems available
- best opportunities to proceed with FC and CSP technologies
- basis for 3D chip integration



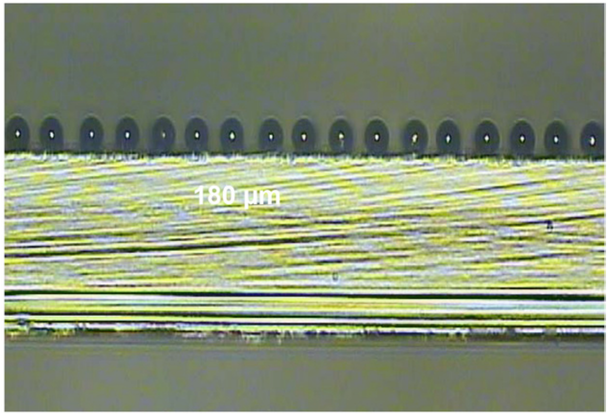
Cu/SnEutectic Bonding "ICV-SLID Technology"

Process flow–Fabrication of inter-chip vias with standard wafer process sequence–Simultaneous formation of electrical and mechanical connection

- Thin SLID layers (ca. 10 µm in total) with large area contacts
- Modular concept
- Suitable for chip-to-wafer stacking
- Integration densities up to 105cm^{-2}



Thinning of bumped wafers:



Technische Universität Berlin
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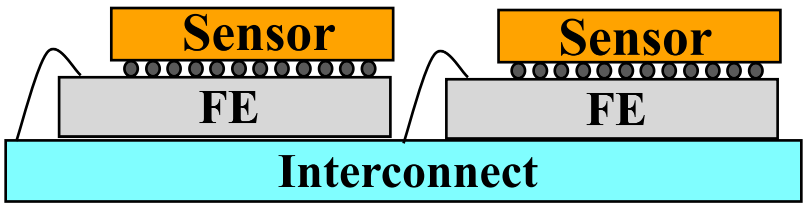
Department:
High Density Interconnect & Waferlevel Packaging
Phone: +49-(0)30-46403-124
Fax: +49-(0)30-46403-123
E-Mail: oswin.ehrmann@izm.fraunhofer.de

Hybrid Pixel Detector Module Incrediences

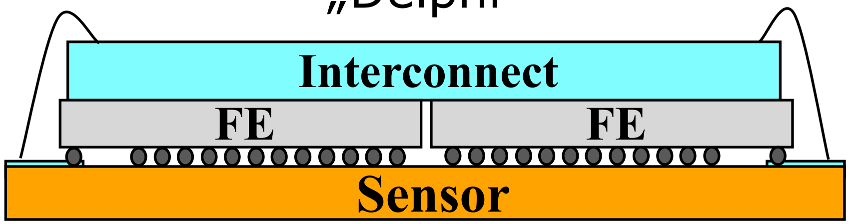
sensor
+
readout electronics
+
High Density Interconnects

But in which arrangement?

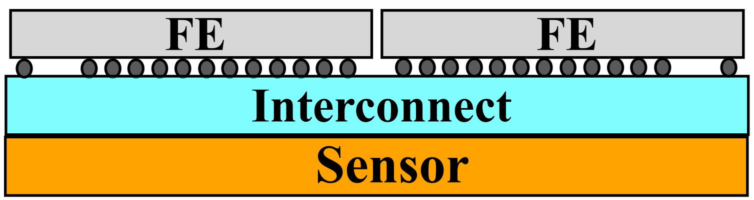
„Omega Halfplane", „ALICE"



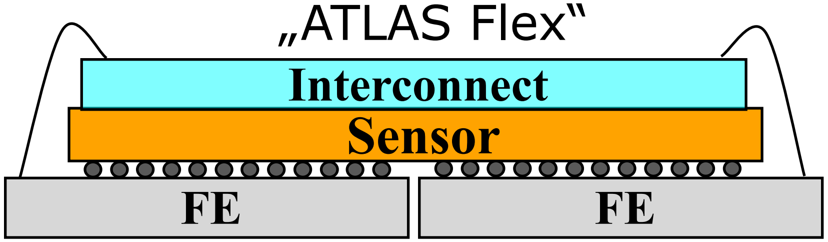
„Delphi"



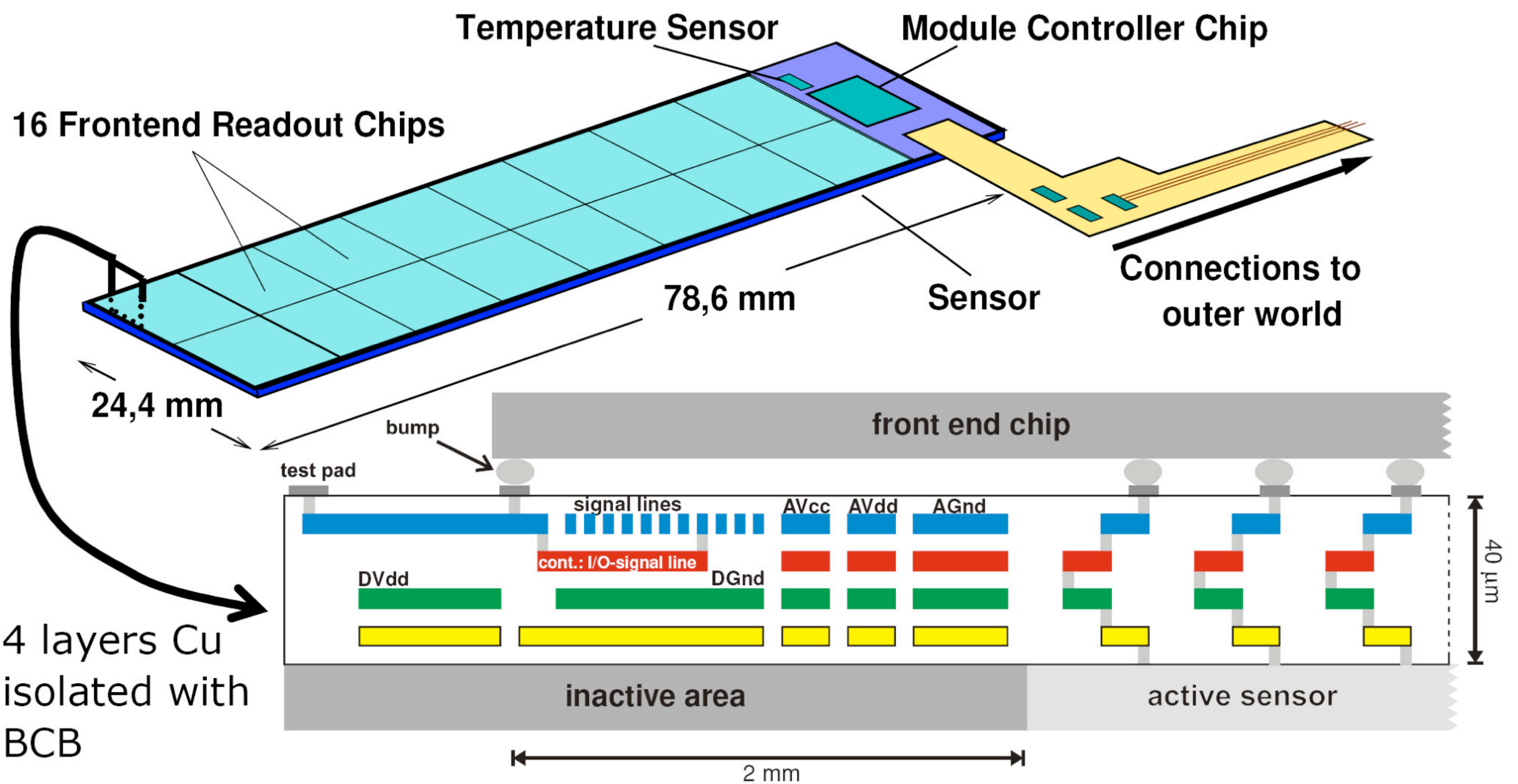
„ATLAS MCM-D"



„ATLAS Flex"

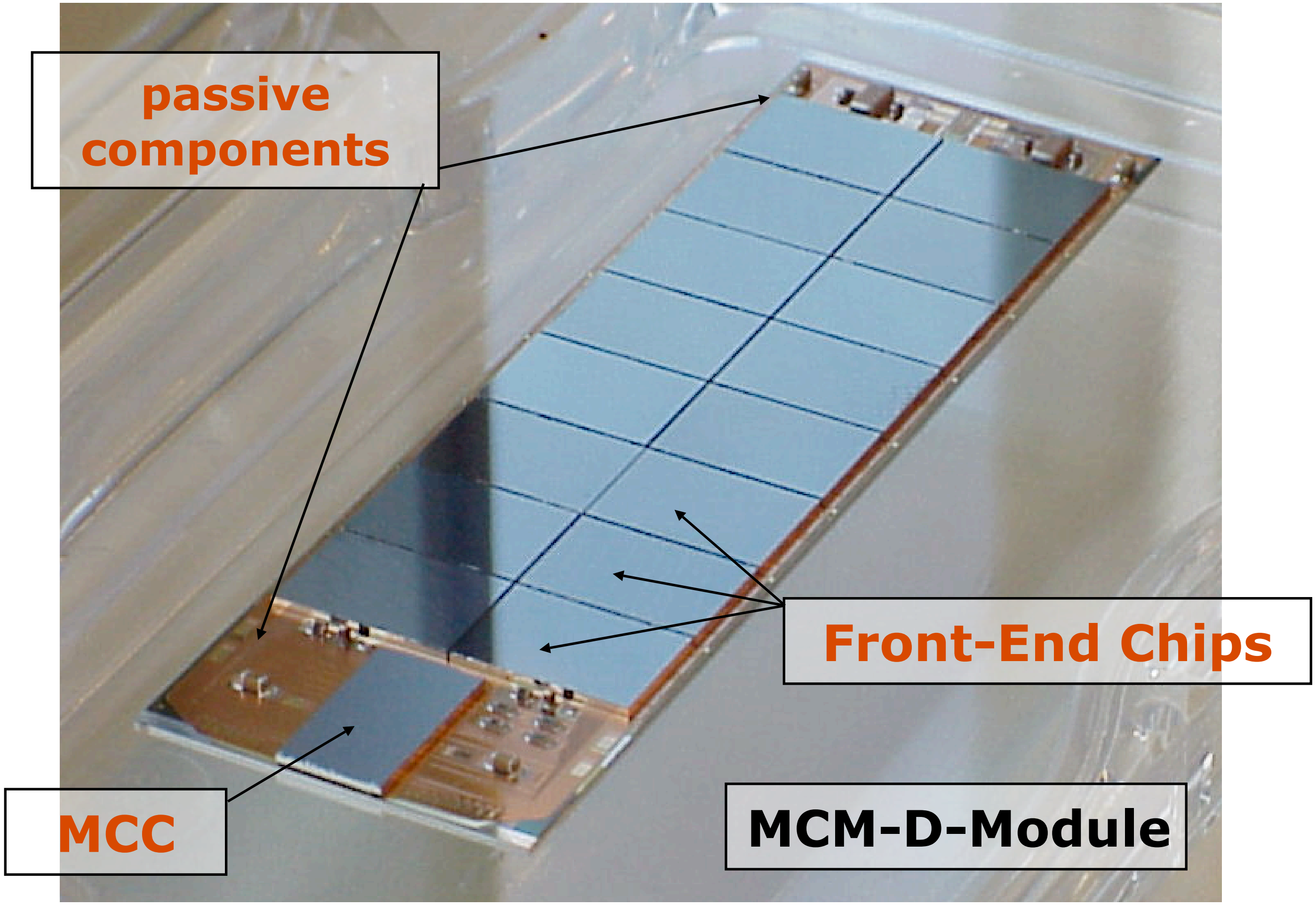


ATLAS Pixeldetector Module in MCM-D - Technology



4 layers Cu isolated with BCB

Module Prototypes



Summary & Outlook

- Basic idea and technology
- Tests:
  - Crosstalk between signal lines (< -30dB for f < 1 GHz)
  - Radiation hardness of BCB as expected
  - Capacity between feed throughs (O(fF))
  - Resistance of feed throughs and via's (O(mΩ))
  - Defects yield ($<10^{-5}$)
  - Crossing of feed throughs increases crosstalk only
- Equal size bricked geometry

Open questions:

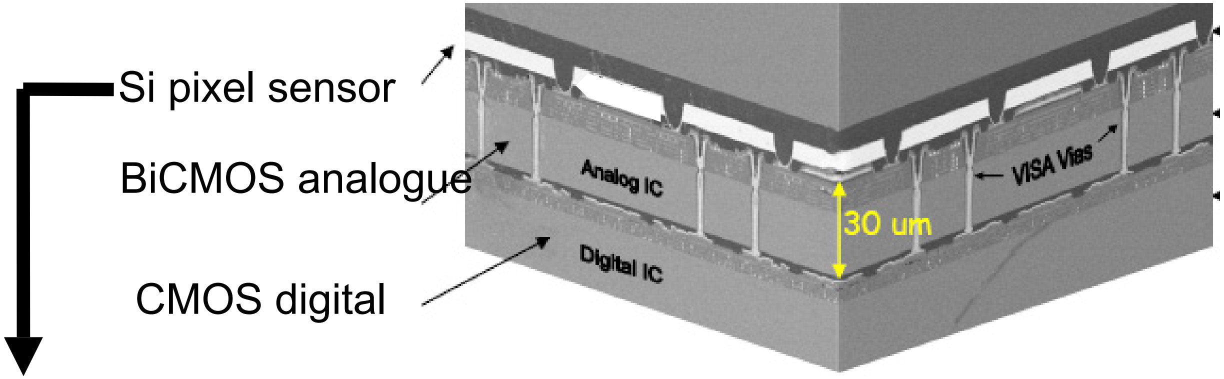
- How long may detector-signal lines be?
- Is it ok to run digital signal lines above sensor?
- Usage of meshed planes?

H.-G. Moser
Semiconductor Laboratory
MPI for Physics, Munich

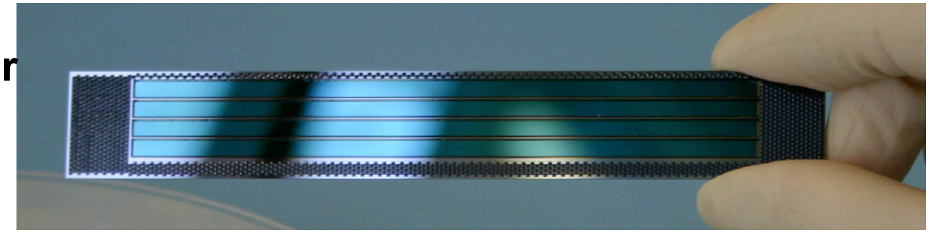
R&D for a novel pixel detector for SLHC

3D interconnection (sensor – electronics; electronics – electronics):

Alternative to bump bonding (fine pitch, potentially low cost?).
New possibilities for ASIC architecture (multilayer, size reduction).
Optimization of rad. hardness, speed, power.
Impact on module design (ultra thin ASICs, top contact, 4-side buttable).



R&D on thin (O(50μm) FZ silicon detectors:
Based on well known pixel sensor technology.
Can be operated at 10^{16} n/cm^2 (V_{dep}, I_{leak}, CCE).



Can lead to an advanced module design: rad hard with low material budget

ATLAS High Luminosity Tracker Upgrade Workshop, Liverpool, 6-8 Dec 2006

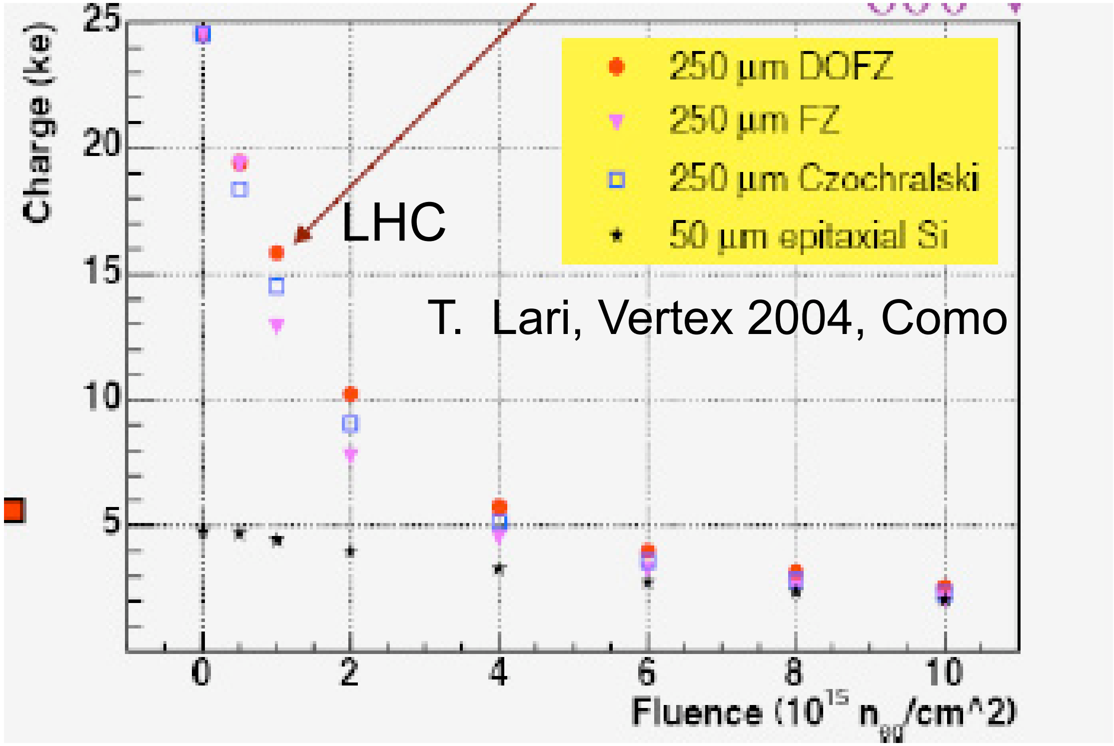
Motivation for Thin Detectors

H.-G. Moser
Semiconductor Laboratory
MPI for Physics, Munich

ATLAS High Luminosity Tracker Upgrade Workshop, Liverpool, 6-8 Dec 2006

After 10^{16} n/cm^2:

V_{dep} > 1000V (250 μm) -> operate partially depleted.
Large leakage currents.
Charge loss due to trapping (mean free path ~ 25 μm).
$I_e > I_h$ (need n-in-n or n-in-p) to collect electrons.



No advantage of thick detectors ->thin detectors: low V_{dep}, I_{leak} (and X_0)

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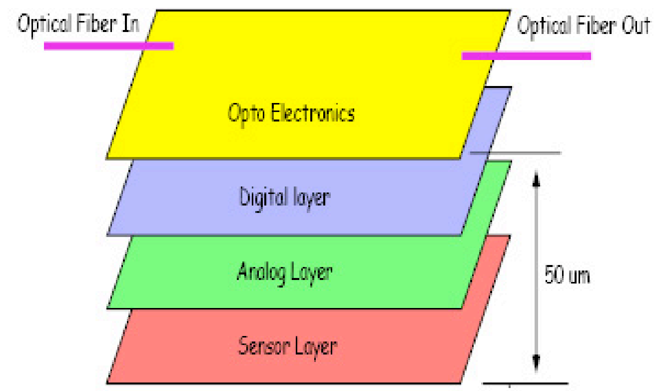
Semiconductor Laboratory
MPI for Physics, Munich

3D Interconnection

2 or more layers (="tiers") of thinned semiconductor devices interconnected to form a "monolithic" circuit.

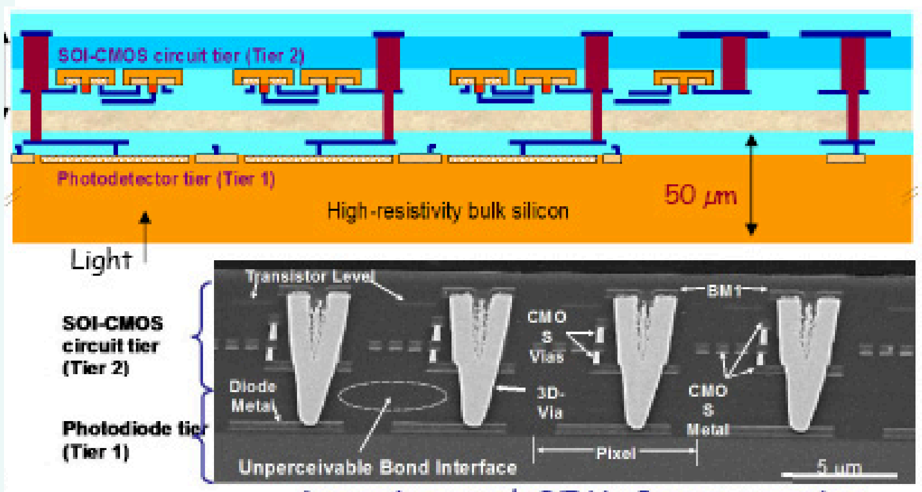
▪Different layers can be made in different technology (BiCMOS, deep sub-μ CMOS, SiGe,…..).

▪3D is driven by industry:
- ▪Reduces R,L and C.
- ▪Improves speed.
- ▪Reduces interconnect power, x-talk.
- ▪Reduces chip size.
- ▪Each layer can be optimized individually



Designer's Dream

For HEP: sensor layer: fully depleted Si
Example: 2-Tier CMOS Sensor, 1024 x 1024 pixel, pitch 8 μm by MIT-Lincoln Lab



Drawing and SEM Cross section

ATLAS High Luminosity Tracker Upgrade Workshop, Liverpool, 6-8 Dec 2006

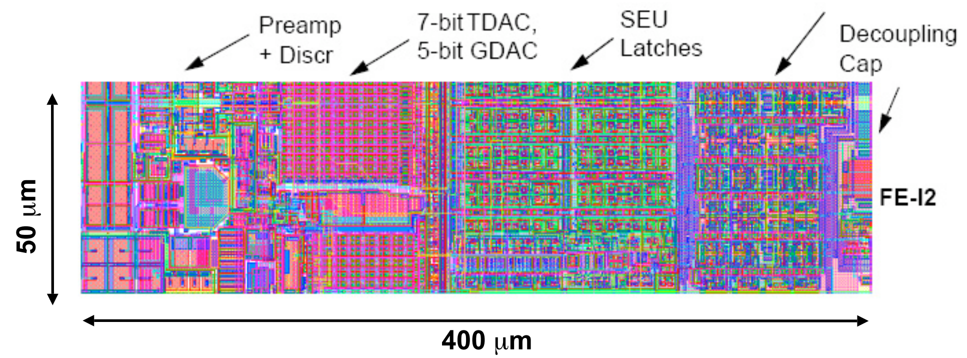
Advantages of 3D

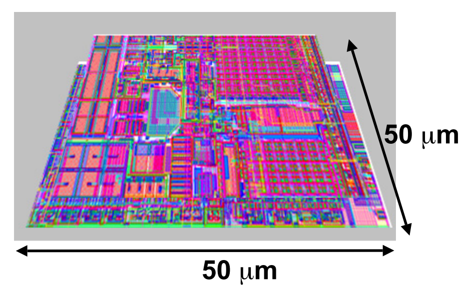
H.-G. Moser
Semiconductor Laboratory
MPI for Physics, Munich

Multilayer electronics:

Split analogue and digital part
Use different, individually optimized technologies:

-> gain in performance, power, speed, rad-hardness, complexity.
-> smaller area (reduce pixel size or add functionality).



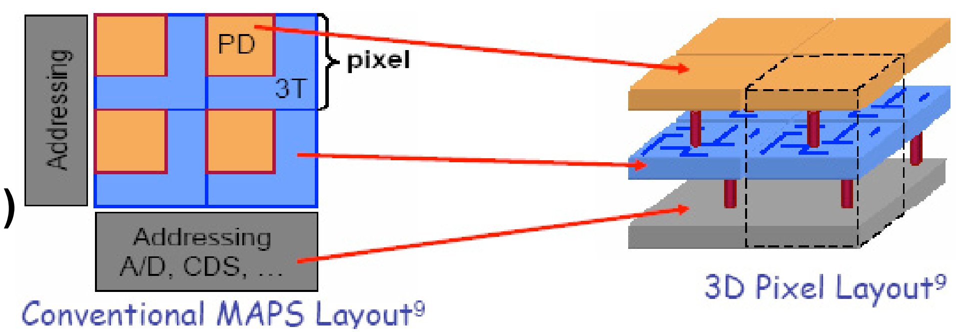


50 x 400 µm² (0.25 µm)
May shrink to ~ 50 x 50 µm² (130 nm)

4-side buttable devices:

-> no dead space.
-> simpler module layout.
-> larger modules.

(reduce complexity and material)



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MPI for Physics, Munich

World Wide Interest in 3D

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT,RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix

Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

Europe: Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

R. Yarema (Fermilab)

3D is discussed in the ITRS (International Technology Roadmap for Semiconductors) as an approach to improve circuit performance and permit continuation of Moore's Law.

R&D driven by industry.
Different approaches (solder, SOI, epoxy).

MPI will work with Fraunhofer IZM, Munich.

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

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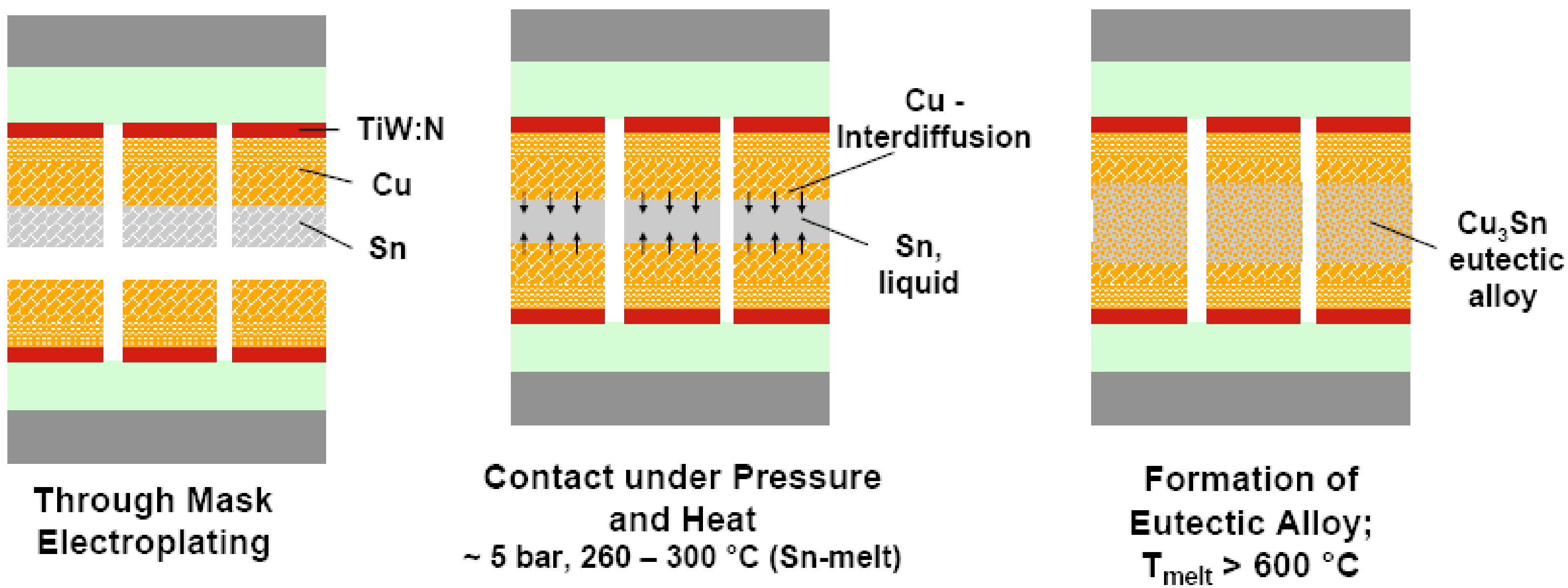
Semiconductor Laboratory
MPI for Physics, Munich

IZM SLID Process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps “low cost” (IZM)).
- Small pitch possible (< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

IZM
Fraunhofer Institut Zuverlässigkeit und Mikrointegration

H.-G. Moser
Semiconductor Laboratory
MPI for Physics, Munich

Summary

We propose an R&D program on:

- **3D interconnection:**
  - **Alternative to bump bonding.**
  - **Opening new possibilities for ASIC and module design.**
- **Thin FZ sensors (“standard” pixel sensors optimized for SLHC).**

Modular R&D:

- **Thin sensor can be used with standard hybrid pixel AISCs (bump bonded).**
- **3D Interconnection is an option for other sensor types (e.g. 3D detectors).**

Time Scale:

- **Thin Detectors: 2007.**
- **Simple 3D demonstrator (SLID, no thinning of ASICs): 2008.**
- **Advanced 3D demonstrator (ICV-SLID, vias, thinning): 2009.**

- **Resources at MPI: 150 kEuro/year (& one engineer).**

Other groups are invited to join (especially ASIC developers).

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Semiconductor Laboratory
MPI for Physics, Munich

Invitation Pixel Meeting

» Liebe Kollegen/innen,
» mit dieser mail moechte ich Sie auf ein Treffen am
» ---- Freitag den 16.2.2007, ca 10:00 - 17:00 ----
» in Muenchen im Rahmen der R&D Aktivitaeten fuer ein pixel detector upgrade fuer
» SLHC aufmerksam machen.

» Wie in Liverpool von Hans-Guenther Moser vorgestellt
» http://indico.cern.ch/materialDisplay.py?contribId=15&materialId=slides&confId=a063014
» arbeiten wir am MPP Muenchen zur Zeit an einem Konzept fuer einen Pixeldetektor
» fuer SLHC.

» Das Forschungsproposal hat die drei folgenden Hauptschwerpunkte:
» 1) Entwicklung duenner Pixel-Sensoren
» 2) Verwendung einer neuartigen Verbindungstechnologie, solid-liquid
» interdifusion bonding (SLID), als moeglichen Ersatz des bump bondings, in
» Zusammenarbeit mit dem Fraunhofer-Institut fuer Zuverlaessigkeit und
» Mikrointegration IZM, in Muenchen.
» 3) 3D-Systemintegration der Elektronik mittels inter-chip vias (ICV) und SLID.

» Parallel wollen wir Mechanik und Kuehlung studieren und auf ein Modulkonzept
» hinarbeiten.

» Wir formulieren gerade ein R&D proposal - Call of interest.

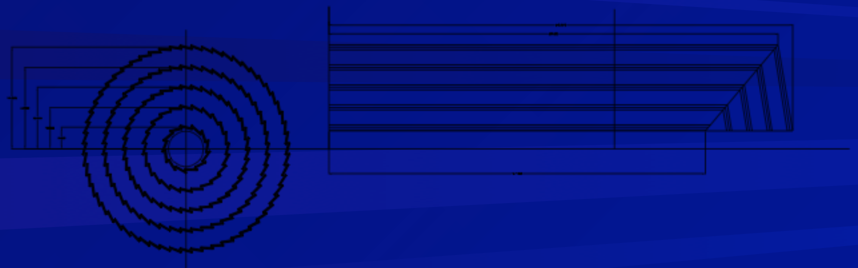
» Zum Ideenaustausch und evtl zum Aufbau einer Zusammenarbeit mit interessierten
» deutschen ATLAS Gruppen findet am Freitag den 16.2.2007 ein erstes Treffen in
» Muenchen statt.

» Ihre Teilnahme am Treffen zugesagt haben bereits die Gruppen aus Bonn, Dortmund
» und Wuppertal, eventuell auch Interesse hat Freiburg.
» Sollten Sie oder Ihre Mitarbeiter an diesem Treffen teilnehmen wollen, sind Sie
» hiermit herzlich eingeladen. Schicken Sie mir in dem Fall bitte eine kurze mail.
» Mit freundlichen Gruessen,
» Richard Nisius
» ------------------------------
» Dr. Richard Nisius
» Research Scientist
» Max-Planck-Institut fuer Physik
» Foehringer Ring 6
» D-80805 Muenchen, Germany
» Phone: +49-89-32354-474

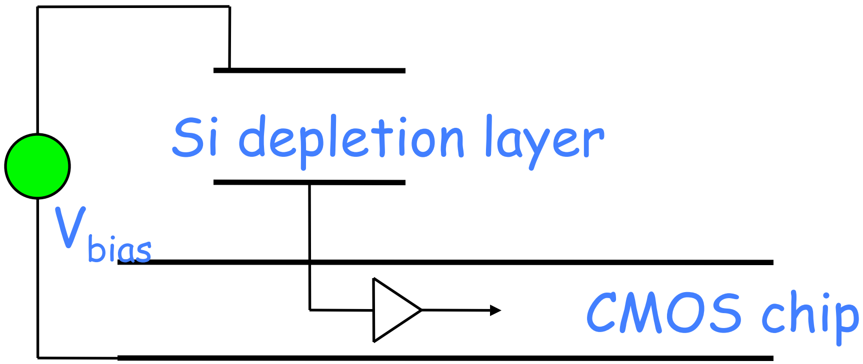
GOSSIP:
a new
and potentially better
vertex detector
for ATLAS

Harry van der Graaf
NIKHEF, Amsterdam

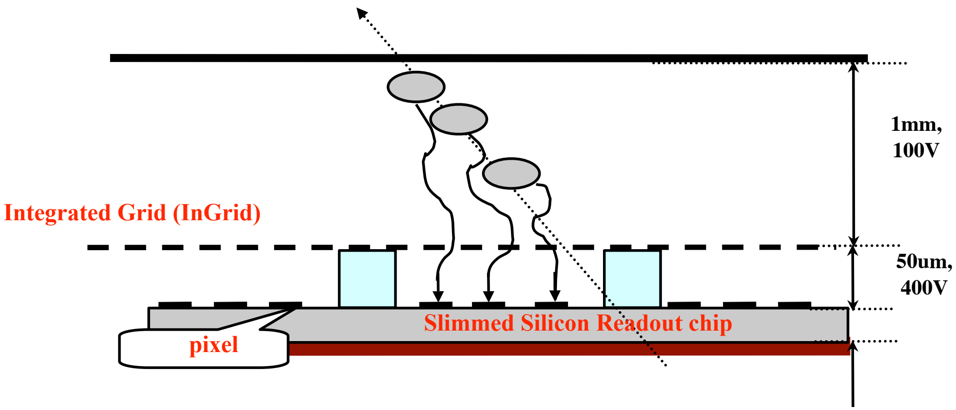
ATLAS Upgrade Workshop
Dec 7, Liverpool, 2006



Si (vertex) track detector GOSSIP



- Si strip detectors
- Si pixel detectors
- MAPs



Gas: 1 mm as detection medium

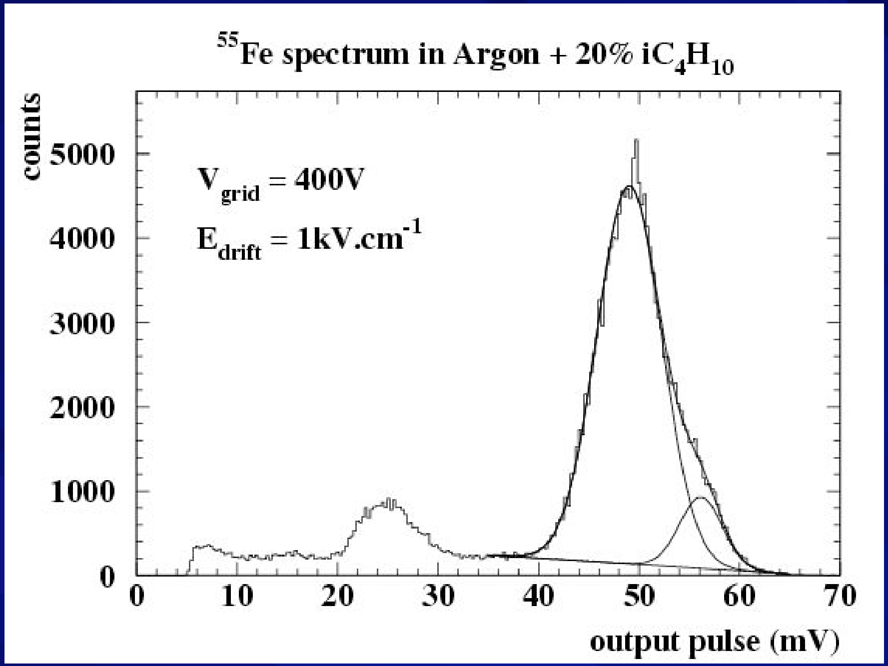
99 % chance to have at least 1 e-

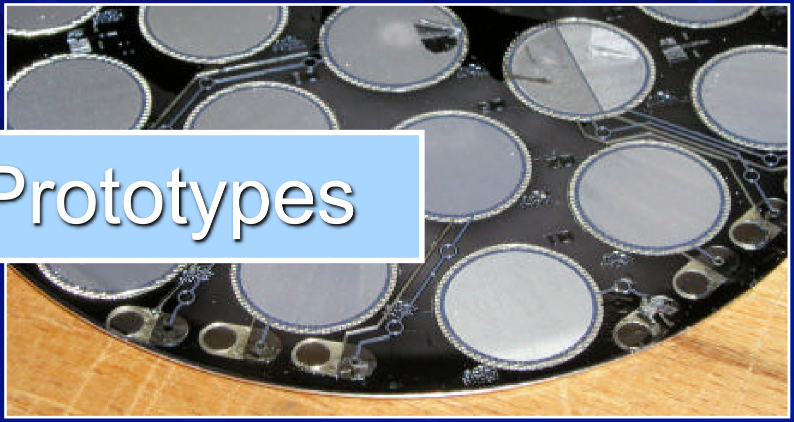
Gas amplification ~ 1000:

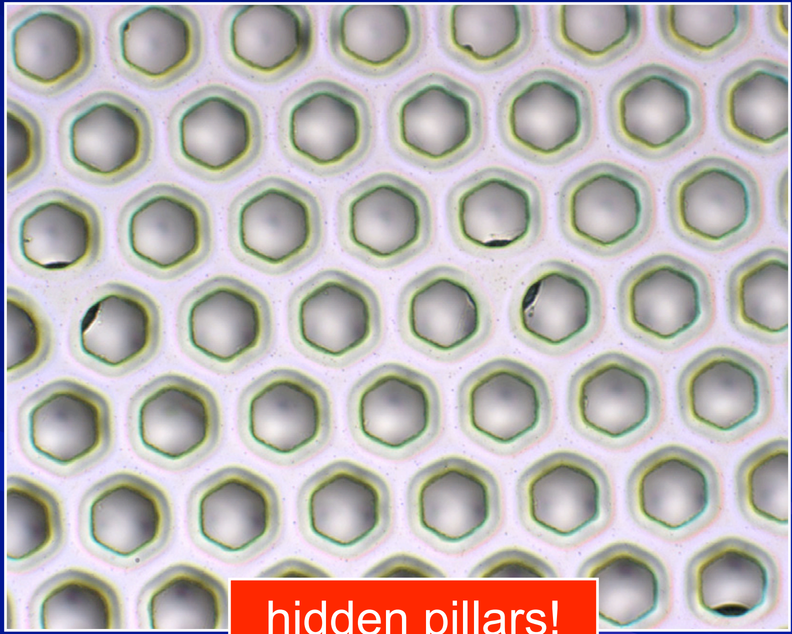
Single electron sensitive

All signals arrive within 16 ns

H. van der Graaf, *Gossip - Vertex Detector for ATLAS*







Very good energy resolution:

Very precise dimensions d < 0.1 μm

WPP Technology is ready to be applied

Gas instead of Si Pro

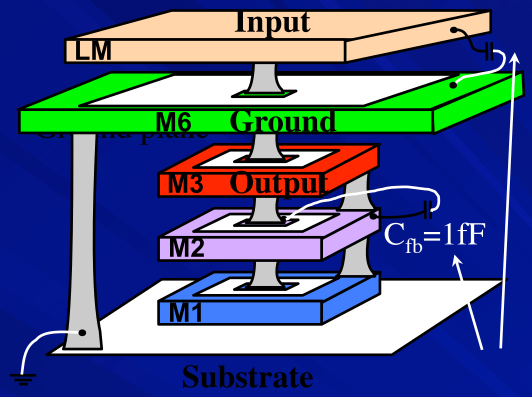
Low mass detector!

- low power: 2 μW/pixel (analog), 0.6 μW/pixel (digital)
  Total 2.6 μW/pixel ⇒ 0.1 W/cm^2 due to:

  - extremely low source capacitance (10 fF)
  - fast & arbitrary large charge signals
  - no bias current

  ⇒ little material required

  for power & cooling

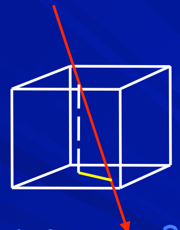


- Thinning (Slimming) of CMOS pixel chip
  to 50 μm

detection layer: only 0.06 % radiation length

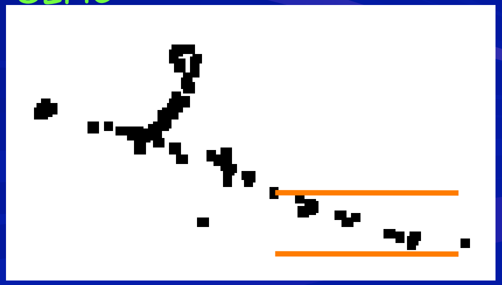
⇒ new vertex detector: 5 – 10 layers instead of 3

-a GOSSIP detector measures a track segment instead of a point-in-space:
  - single-electron sensitive (eff > 95 %)
  - ~ 10 e- along 1 mm track lengt spatial resolution: 50 μm / √10 = 15 μm



14 mm^3

- radiation hardness
  - gas is flushed
  - CMOS chip (130, 90, 45 nm technology): sufficiently radiation hard for SLHC
- very low sensitivity for neutrons, X-rays and gammas
- 'simple' CMOS chip:
  - modest (small area) analog input circuits
  - no bias current: simpeler input circuit
  - pixel area available for data storage & communication
- No detector bump bonding: only wafer post-processing (SiProt + InGrid)



Gas instead of Si Con

- GOSSIP has 1 mm detection layer:

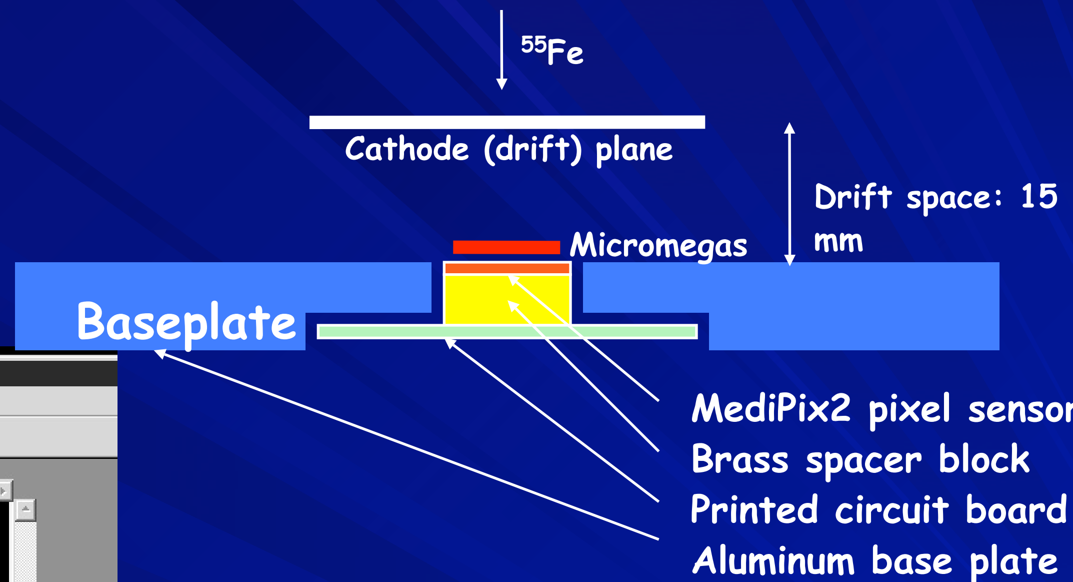
  - parallax error: elimination requires drift time measurement
  - ☺ with single-electron measurement: track segment data per layer!

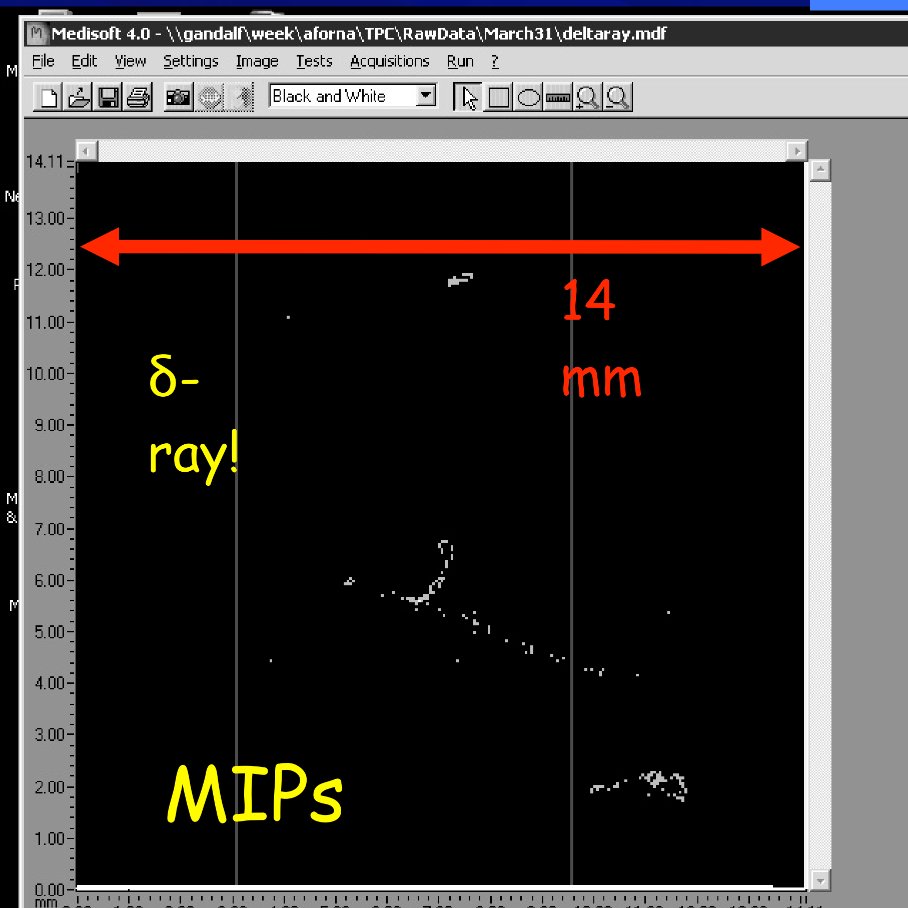
- Gas-filled detector:

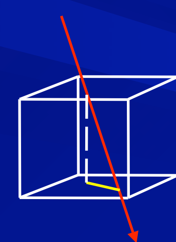
  - chamber ageing (deposit on electrodes)
  - discharges (sparks, too large signals) ruin CMOS chip

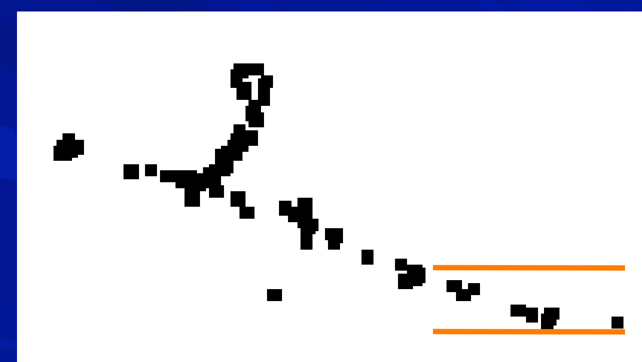
Spark issue must be solved FIRST!

April 2004 Micromegas + MediPix 2 NIKHEF/Saclay/Univ. Twente:

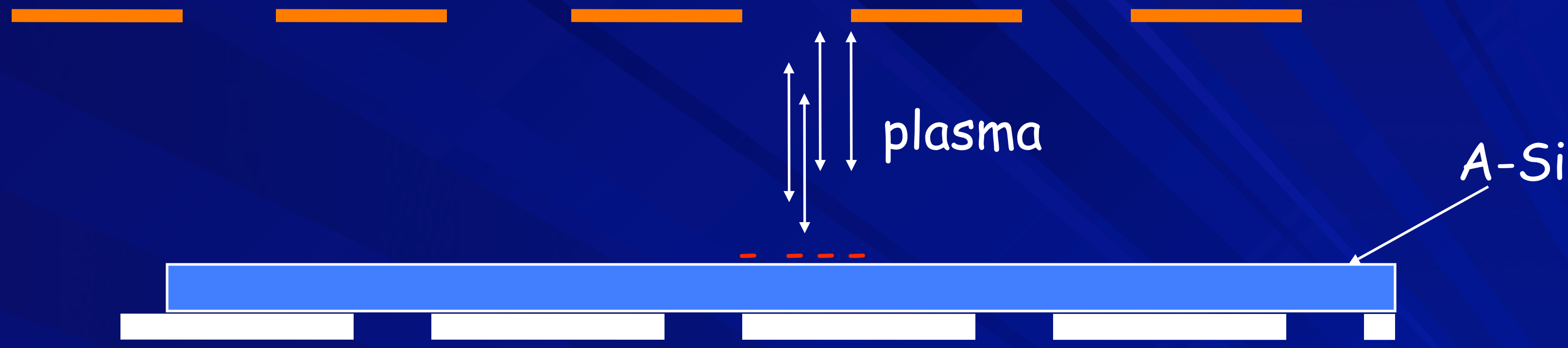








He/Isobutane
80/20
Modified MediPix



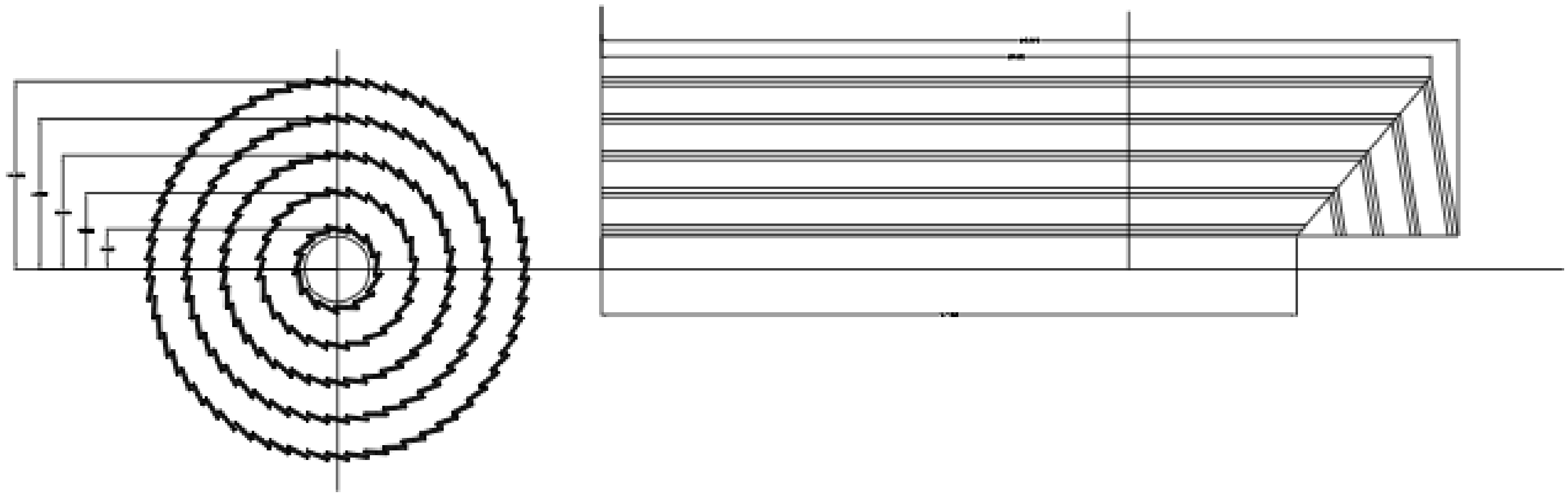
- RPC principle: reduction of local E-field
- Avalanche charge: electrostatic induction towards input pad
- Specific resistance: - high enough to 'block' avalanche charge
  - low enough to flow signal current
  - layer thickness 4 μm, R_{vol} > 0.2 – 100 GΩ/cm

Technology

A-Si deposit: standard wafer post processing, but wafers may get too hot

☺ Univ. of Neuchatel/IMT/P. Jarron (CERN) uses this for integrated X-ray sensor/convertor on MediPix 2

Virtual goal: ATLAS pixel vertex



- Ladder strings fixed to end cones
- Integration of beam pipe, end cones & pixel vertex detector
- 5 double layers seems feasible

H. van der Graaf, ***Gossip - Vertex Detector for ATLAS***

Modules – Inner Radius Layers (2)

ATLAS Tracker Upgrade Workshop

Thursday 07 December 2006

Module Integration Session (08:30 ->13:00)

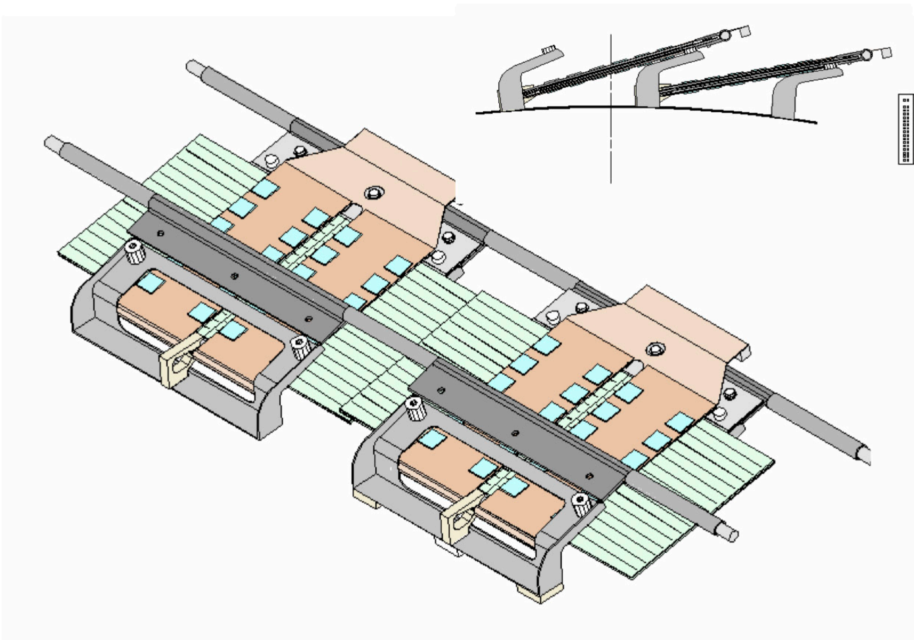
Chairperson: Phil Allport (*U. of Liverpool*)
Location:

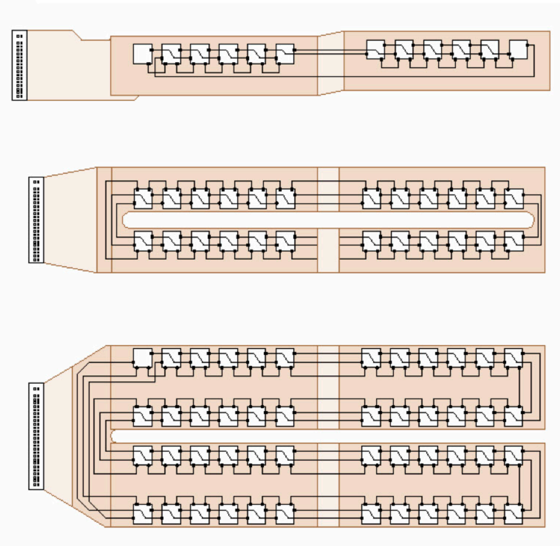
11:00	Module Development for ATLAS/SLHC (25') (Slides)	Yoshinobu Unno (*KEK*)
11:25	Stave Concept (25') (Slides)	Carl Haber (*Lawrence Berkeley National Laboratory (LBNL)*)
11:50	Negative Charge Measurements with ATLAS SCT Readout (15') (Slides)	Peter Kodys (*Charles University*)
12:05	Interconnects, Packaging and Power (25') (Slides)	Marc Weber (*Rutherford Appleton Laboratory*)
12:30	Serial Powering R&D for Pixels: Status and Plan (15') (Slides)	Markus Cristinziani (*Physikalisches Institut*)
✦ 12:45	Power Delivery of Low Voltage and High Currents for the SLHC ATLAS Tracker (15') (Slides)	Satish Dhawan (*Yale University*)

Outline (2)

- ***Module Integration - Inner Layers (Strips)***
  - ***New concepts of sensor integration, self-supporting stave structures***
  - ***Power supply: DC-DC near the sensors - new industrial developments; serial powering of staves***
- ***Engineering***
  - ***Radius of beam pipe probably unchanged - innermost pixel layer***
  - ***Carbon fibre/foam support structure; outstanding property - cooling***
  - ***Cooling - hot issue***
- ***Sensors and Electronics***
  - ***ASIC's design on new level of standardisation - e.g. tracker & LAr R/O; CMS co-operation (other partners?!); Very essential: costs!
Man power needed urgently for architecture design, controllers, protocol design***
  - ***3D pixel collaborators - good progress - 6 EOI - new groups joining; rad-hard, fast, highly integrated structures, time-table***
  - ***SSP group with new results***

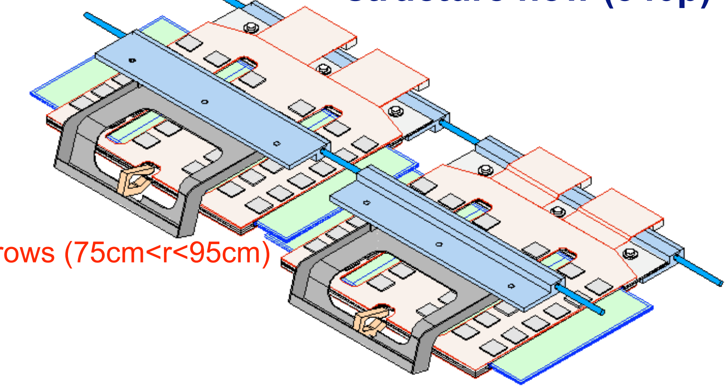
SLHC Module - A Proposal





- Presented at the Oct. workshop at CERN
- One module with 124x64mm^2 sensor
  - Segmented into 1, 2, and 4 striplets
  - Wrap-around hybrids with 1, 2, and 4 rows of ASIC's

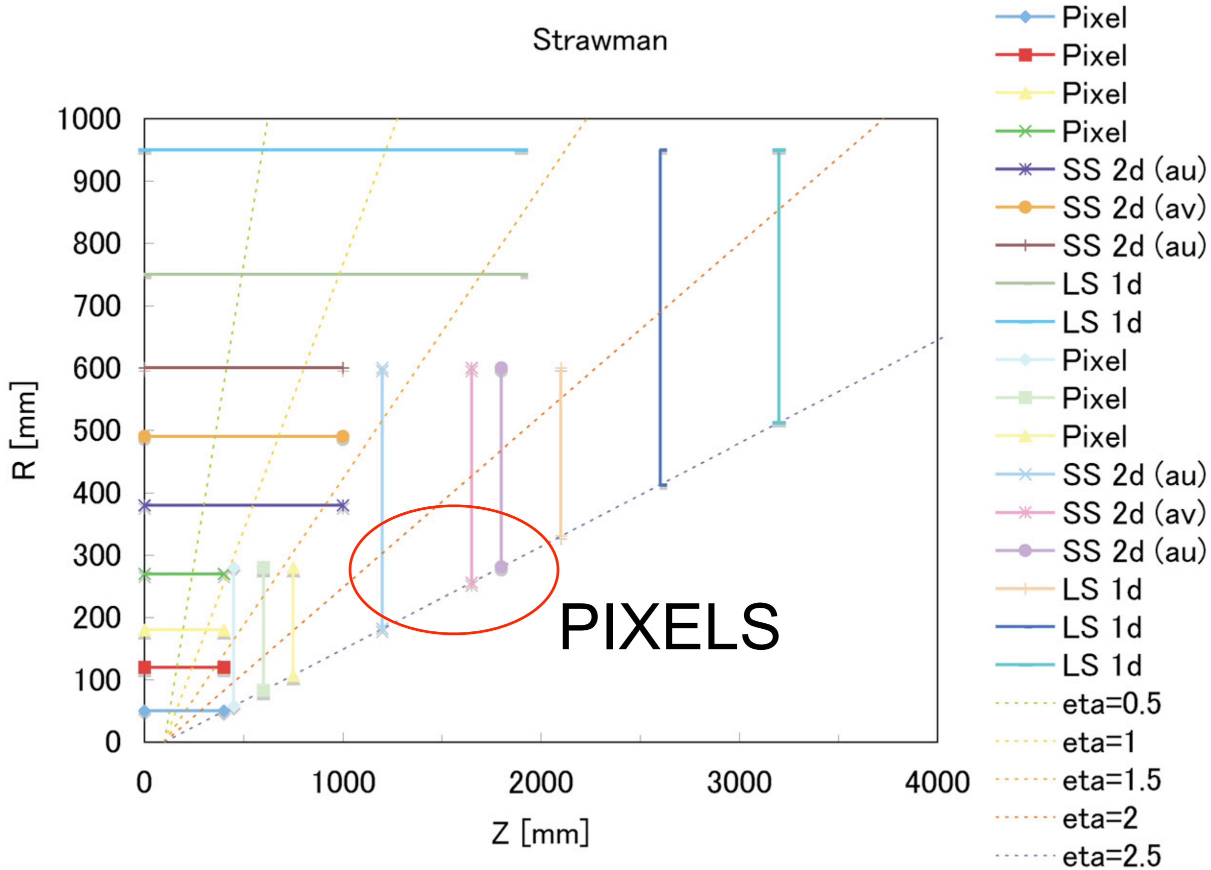
LS modules for barrel structure now (340p)



- Module concept
  - Sensor size: 124.68 mm x 63.68 mm
  - Three types: 6 rows (34cm<r<44cm) shown, 4 rows (44cm<r<75cm), 2 rows (75cm<r<95cm)
  - Edge "stay-clear" for overlapping (max. overlap 10 mm)
  - Straight cooling pipe (ready for high pressure CO_2)
  - Large area cooling plate, allowing high/low positions

Y.Unno, *Module Development for ATLAS at SLHC*

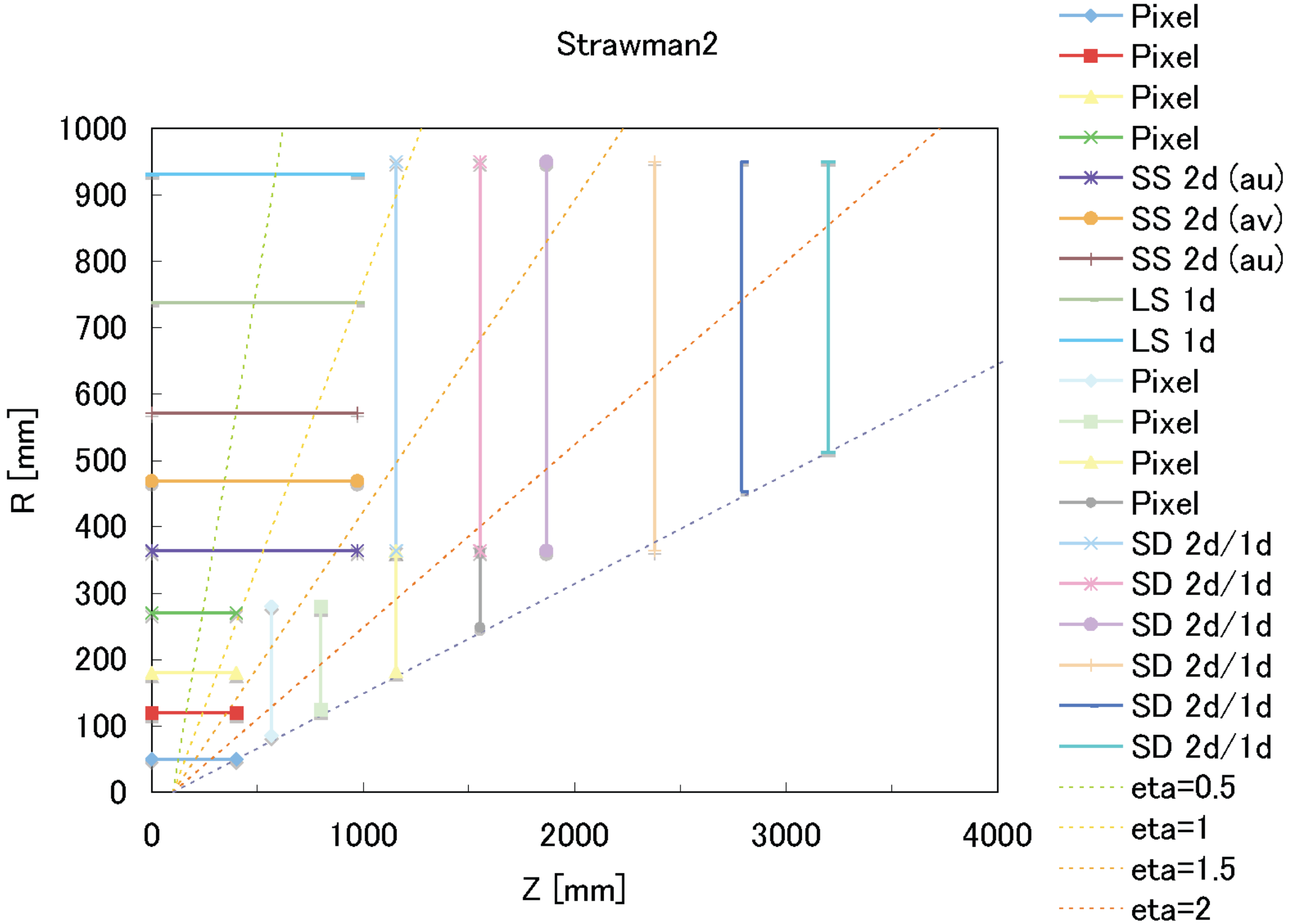
Strawman Layout?



- Our responses
  - R<30cm should be ALL pixels
  - No break between the strips and pixels?
  - Disc layout needs to be optimized

Y.Unno, ***Module Development for ATLAS at SLHC***

Strawman2 - Preliminary



- Need fine tuning yet

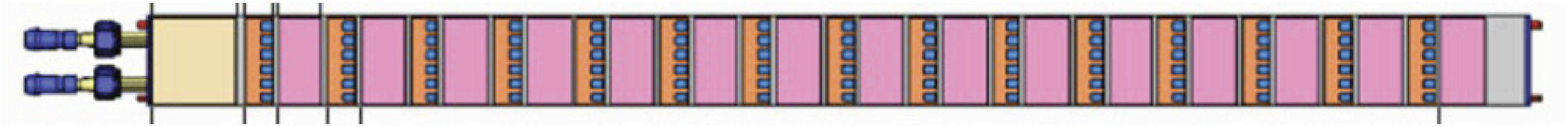
Y.Unno, *Module Development for ATLAS at SLHC*

R&D Proposal

- In preparation from EOI
- Participating Institutions
  - Open to new collaborators
  - KEK, Geneve, Freiburg, Melbourne, Valencia
- Schedule
  - 2007 Conceptual designs, themro-mechanical prototyping
  - 2008 Electrical prototyping, irradiation, beamtests
  - 2009 Final protoyping, Irradiation, beamtests
  - 2010 TDR
- Resources

Institution	Module	Hybrid	Structure	Prototyping
KEK	x	x	-	x
Geneve	x	-	x	x
Freiburg	x	x	-	x
Melbourne	x	-	-	x
Valencia	x	-	-	x

Y.Unno, ***Module Development for ATLAS at SLHC***

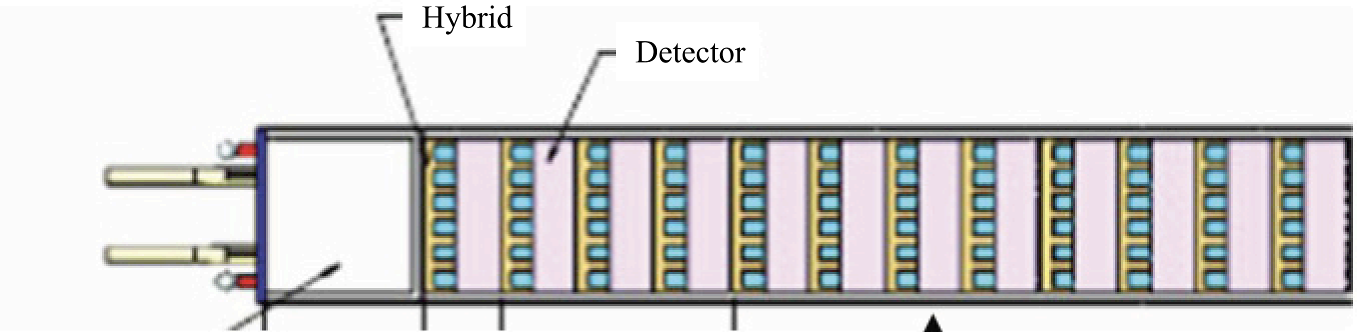


Integrated Structures

- Alternative to individual rigid modules on a rigid support: "super-modules" (or "staves") plus end-plates*.
- Minimize heat flow path lengths
- Eliminate mechanical redundancy
- Integrate support, cooling, electrical services
  - Increased integration implies decreased material
- Assembly sites build, test, & deliver these units
  - Final assembly is simplified
- Include alternative powering schemes – reduce services
- Create higher-value elements & assume greater risk

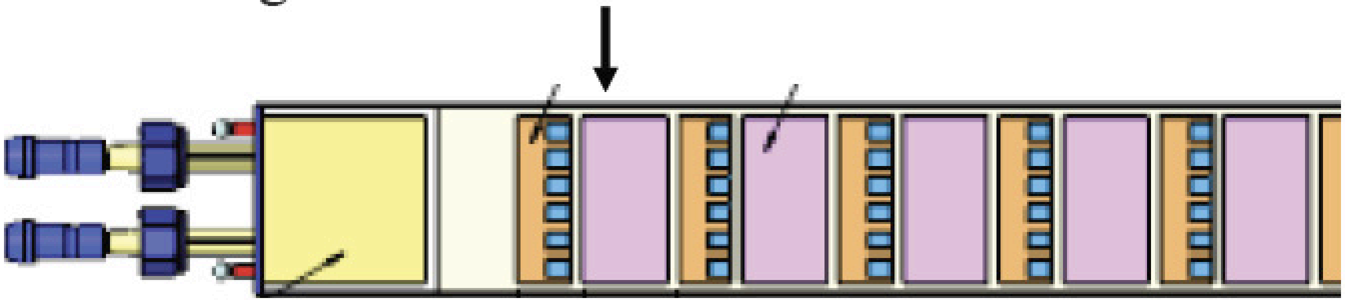
*see presentation of D.Lynn and other layout discussions

C.Haber, ***Stave Concept: Development of Large Area Integrated Tracking Structures***

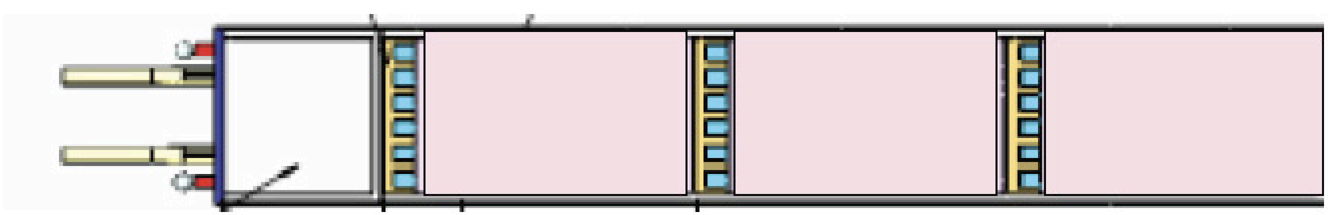


1 meter,
<u>Double sided,</u>
3 cm strip,
32 modules/side
192 Watts
2.5 % Xo

Naturally accommodate double sided (stereo) or singled sided short sensors



1 meter,
<u>Effective single sided,</u>
3 cm strip,
15 modules/side
108 Watts
1.7 % Xo

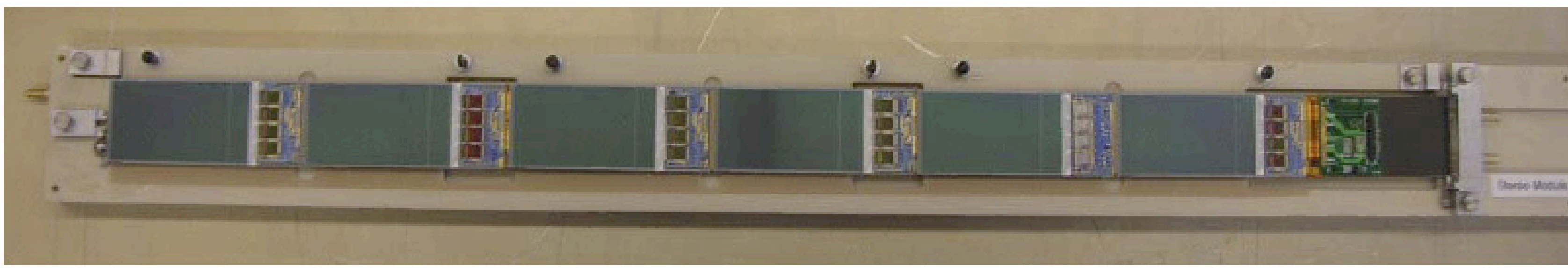


2 meter,
<u>Outer tracker,</u>
<u>Double sided,</u>
12 cm strip,
8 modules/side
1.7 % Xo

C.Haber, *Stave Concept: Development of Large Area Integrated Tracking Structures*

Electrical Tests

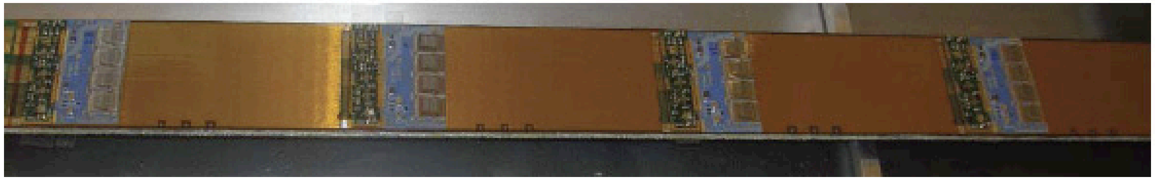
- Develop ATLAS hybrid specific for multi-module use
- 1 sensor + hybrid = 1 module (hybrid glued to Si); 6 modules per side
- Modules linked by **embedded bus cable**
- Total length 66 cm, 6144 channels
- Built around carbon fiber/foam laminate

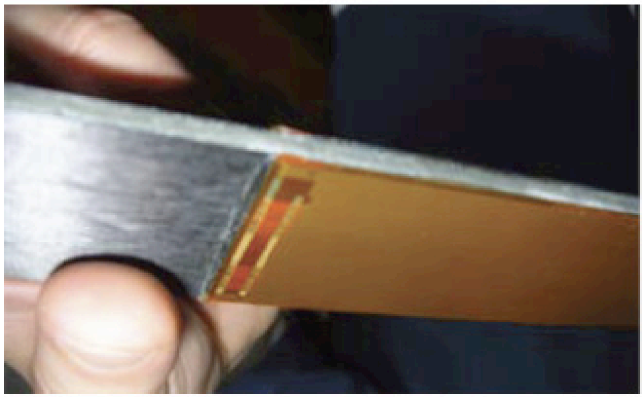


- Measure multi-module performance with ATLAS electronics
- Compare individual and serial powering
- A concrete stave example

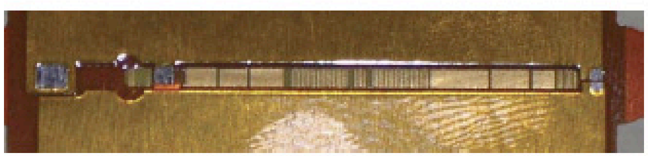
C.Haber, ***Stave Concept: Development of Large Area Integrated Tracking Structures***

Core + Bus Cable + Module

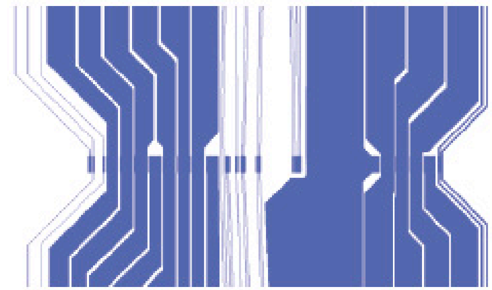




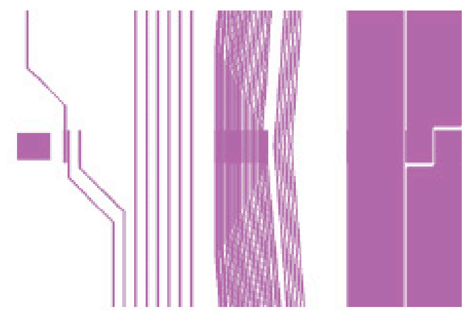
75 Ω differential stripline



Individual

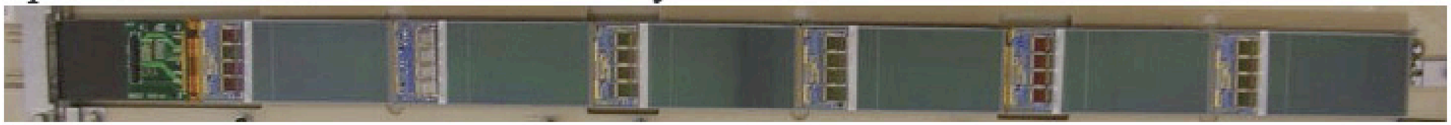


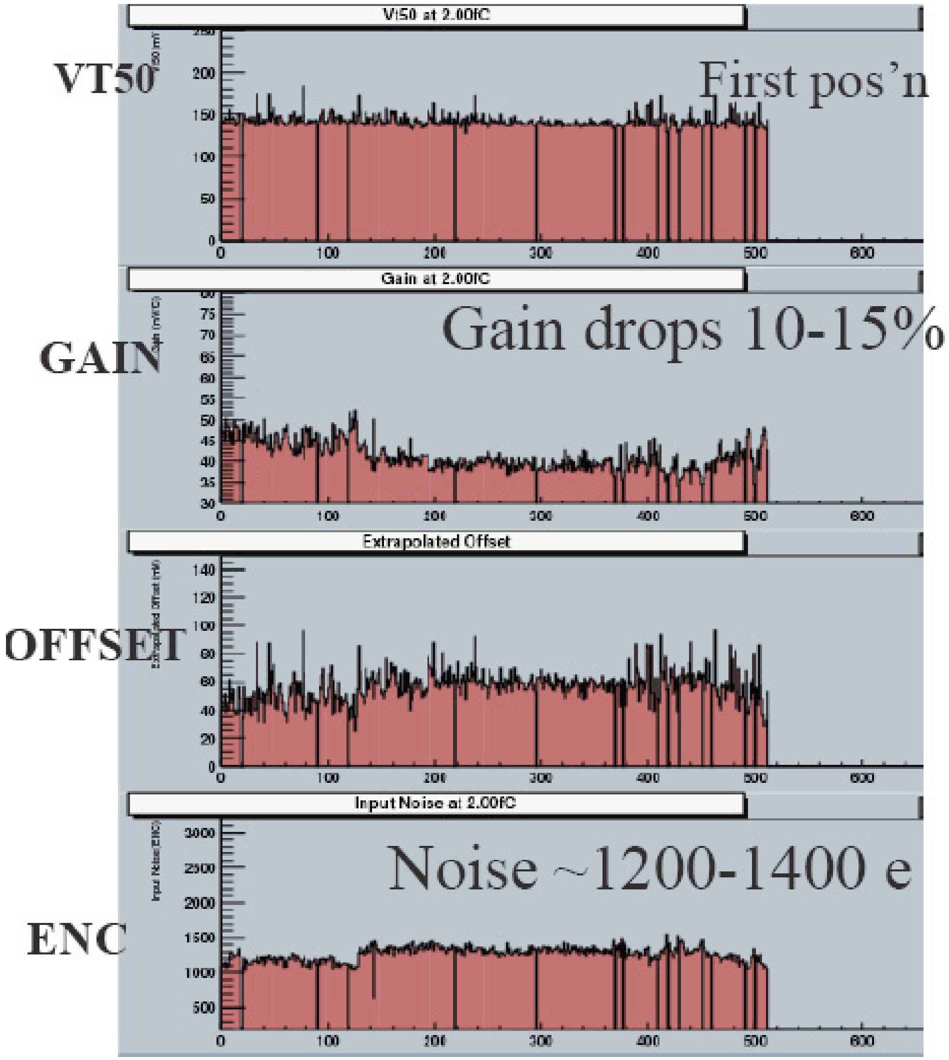
Serial



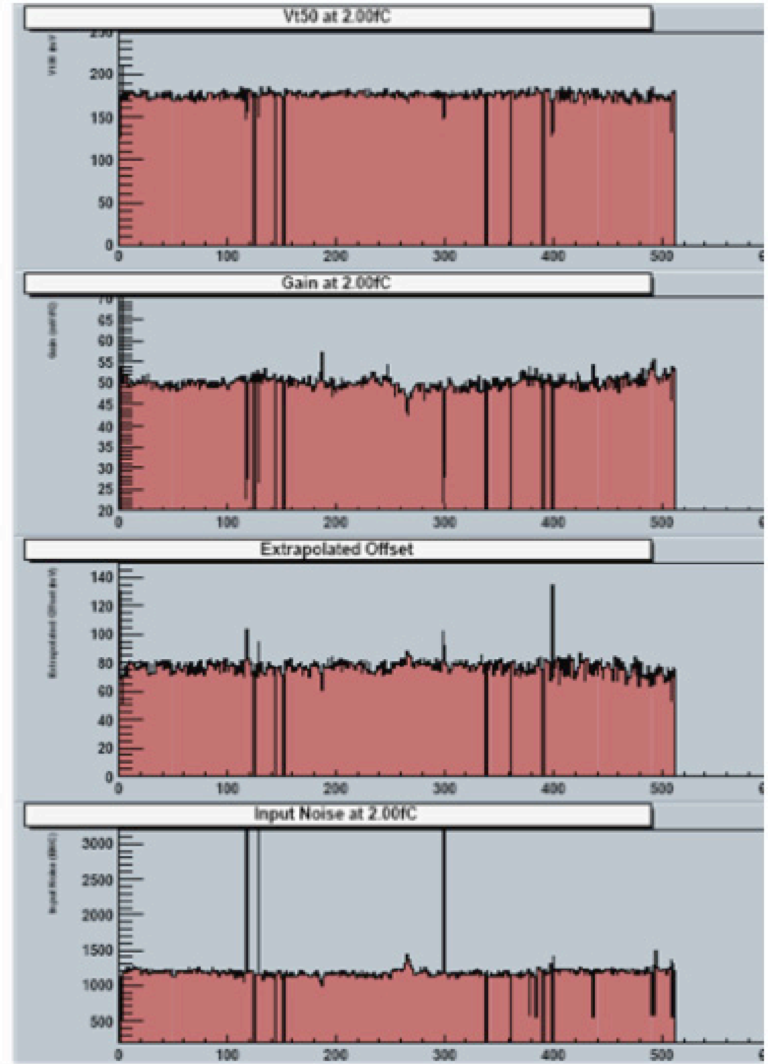
C.Haber, *Stave Concept: Development of Large Area Integrated Tracking Structures*

Serial powered modules on stave + 4 hybrids





Last pos'n



C.Haber, *Stave Concept: Development of Large Area Integrated Tracking Structures*

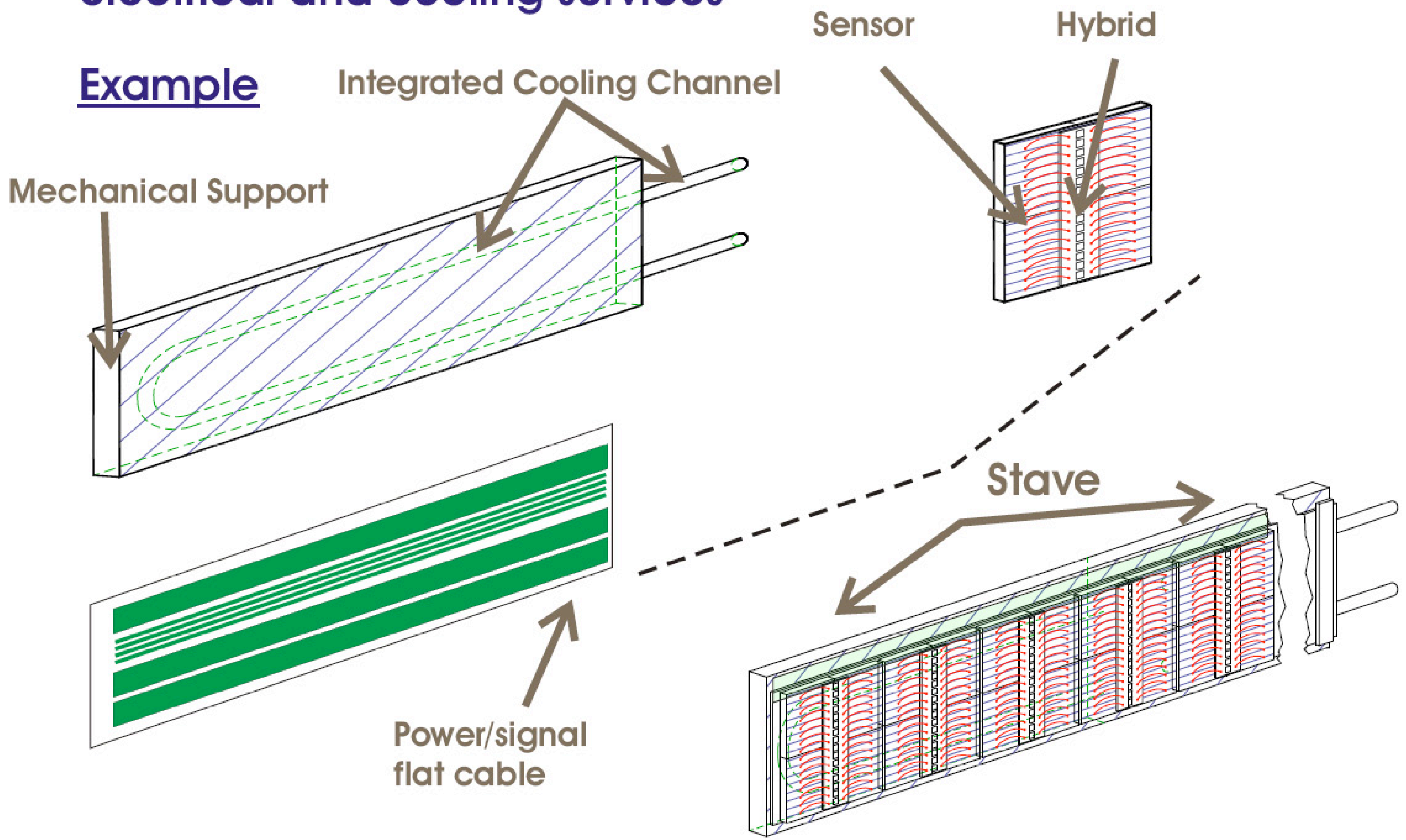
Plans

- Further study of serial powering…
- Develop a DC-DC test stave
- Preparation for an ATLAS SLHC 1 meter stave
  - Aim for construction and test in early 2007
  - Mechanical design and assembly fixtures
  - 3 cm ATLAS detectors
  - New bus cables and hybrid

C.Haber, ***Stave Concept: Development of Large Area Integrated Tracking Structures***

Stave Concept

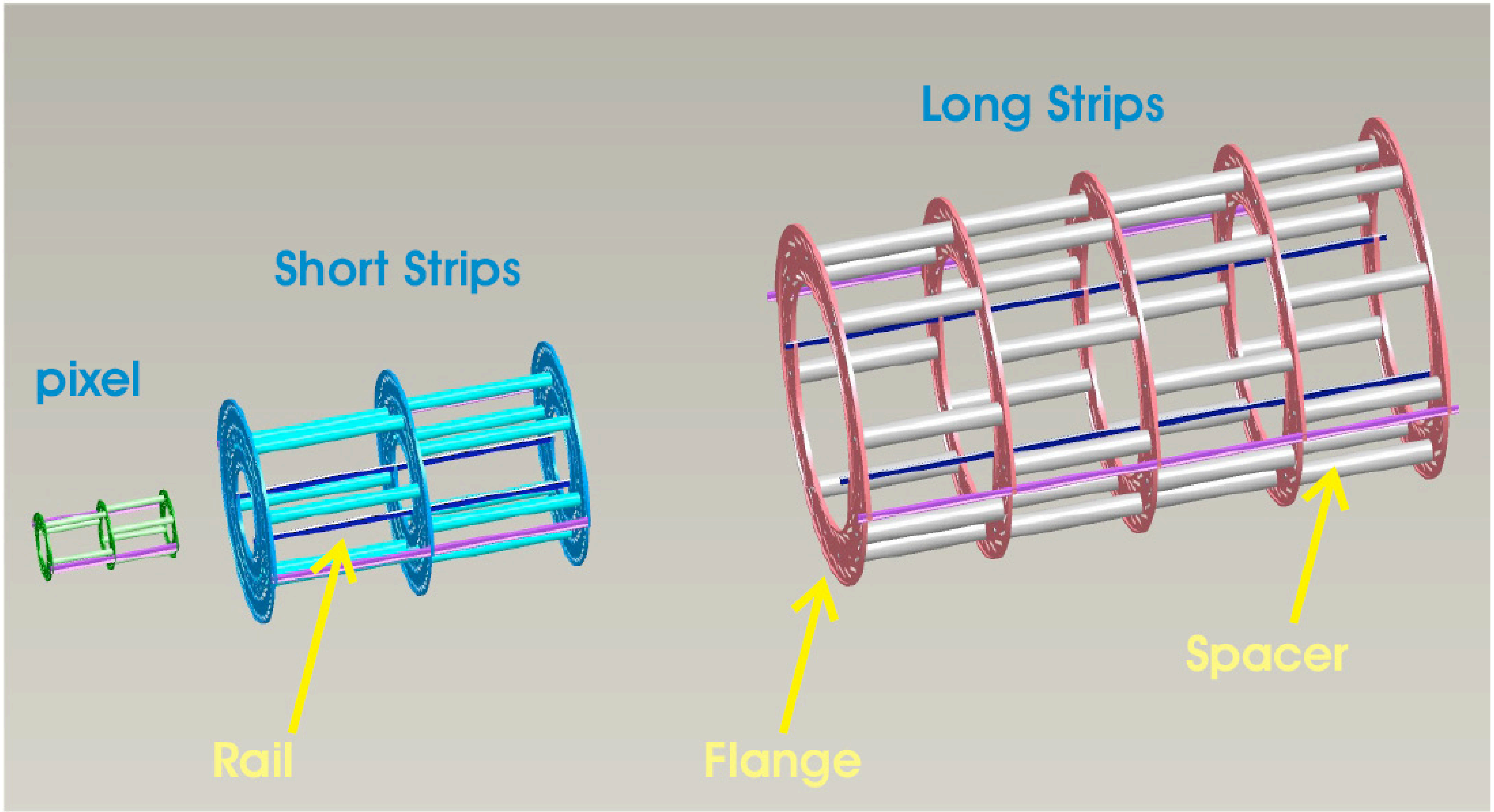
A multi Si-sensor unit with common integrated mechanical, electrical and cooling services



D.Lynn, *Mechanical Support for Barrel Staves*

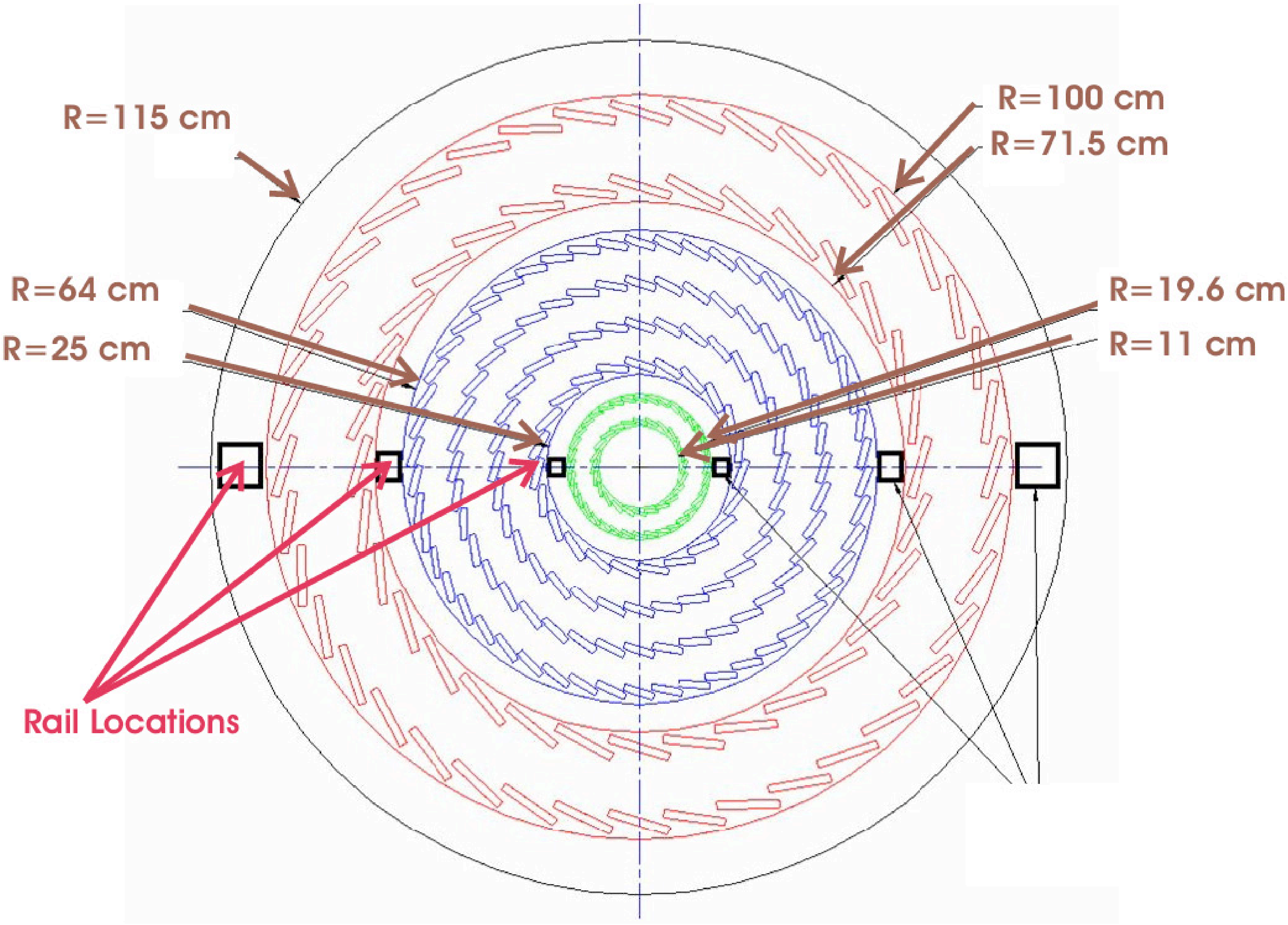
Currently Investigating a "Space Frame Approach"

- Short strip and Long strip flanges spaced 1 meter apart
- Pixel Flanges 40 cm apart
- Each sub-frame allows independent assembly of LS/SS/Pixel Barrels



D.Lynn, *Mechanical Support for Barrel Staves*

Flange Support Locations



D.Lynn, ***Mechanical Support for Barrel Staves***

Summary

- Space frame approach permits access during assembly
- Separate space frames for LS, SS, and pixels permit separate assembly
- Stiffness in Y provided by rails
- Loose tolerances on large flange structures; positioning accuracy may be provided by inserts
- CTE of staves decoupled from space frame
- Sag of staves limited via cantilevered mounting

Design will continue and evolve as we better understand requirements

D.Lynn, ***Mechanical Support for Barrel Staves***

Serial powering R&D for pixels: status and plans

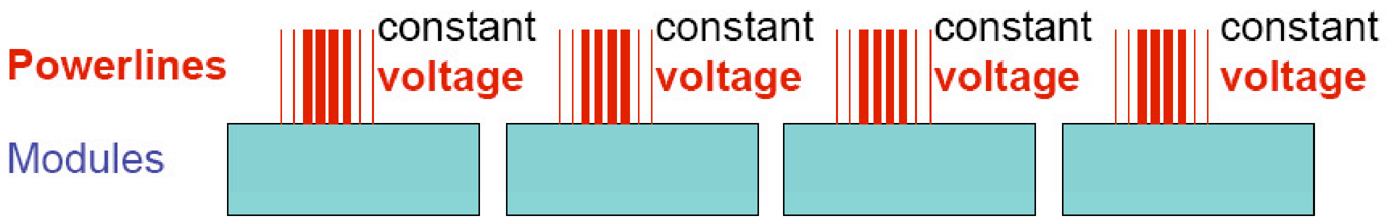
Markus Cristinziani, Andreas Eyring, Jörn Grosse-Knetter,
Hans Krüger, Walter Ockenfels, Norbert Wermes
Bonn U.

Susanne Kersten, Peter Kind, Peter Mättig
Wuppertal U.

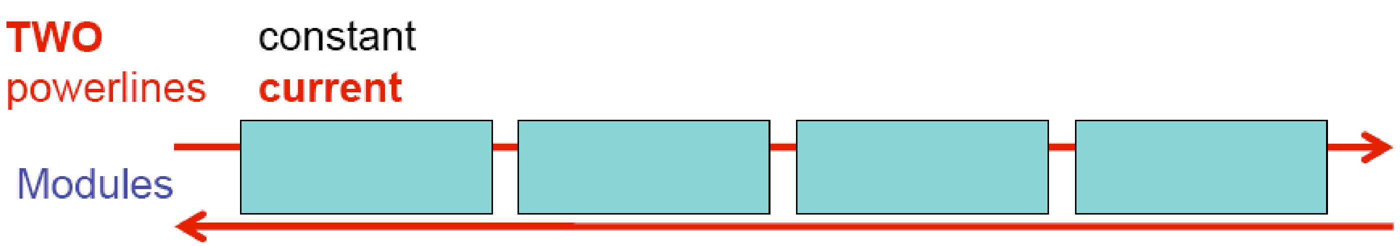
M. Cristinziani, ***Serial PoweringR&D for Pixels: Status and Plans***

Serial versus Parallel Powering

- Currently used in the pixel detector: **Parallel Powering:**



- The idea of **Serial Powering**:



M. Cristinziani, *Serial PoweringR&D for Pixels: Status and Plans*

Comparison

- Power loss in cables (V drop from power supplies to modules: 6.4V)
  - I(PP) = 2.0A, I(SP) = 2.2A
  - PP: 13 x 6.4V x 2A = 166W
  - SP: 6.4V x 2.2A = 14.1W (-91.5%)
- Power loss per module
  - PP: 1A x 2.0 V_d + 1.3A x 1.6V_a = 4080mW
  - SP1: 2.2A x 2.0V = 4400mW (+7.8%) SP2: 2.7x2.0= 5400mW (+32%)
- Total power loss
  - PP: 166W + 13 x 4.08W = 219W
  - SP: 14.1W + 13 x (4.4|5.4)W = 71W or 84W (-67.6% or -61.6%)
- Cable length inside detector:
  - PP: 8 cables x13 cables x 450mm/2 = 23.4m x/x0 = 0.073%
  - SP: 900mm = 0.9m x/x0 = 0.011%
- Cable length outside detector:
  - PP: 8x13x940mm = 97.8m total = 121.2m
  - SP: 2 x 940mm = 1.9m total = 2.8m

M. Cristinziani, ***Serial PoweringR&D for Pixels: Status and Plans***

Proof of principle demonstration

- A number of tests in Bonn with modified ATLAS pixel electronics and changes to the pixel module were made
  - New flex design suited for serial powering routing
  - AC coupled read-out
  - Usage of the on-chip regulators for powering (homogeneity tests)
  - Operation of serially powered module chains (up to six modules)
- Single module operation
  - Noise comparisons and threshold scan comparisons to PP
  - Irradiation tests (250 Mrad)
- Half-stave operation under near-real conditions
  - Cross-talk measurements
  - Add parallel load with voltage ringing applied at different frequencies
  - Test beam (2 serially powered modules)

M. Cristinziani, ***Serial PoweringR&D for Pixels: Status and Plans***

Naïve* extrapolation from SCT to SLHC

Assume 5 times more channels (one layer, barrel, normal impact):

Component	R.L. for SCT	Scaling factor*	R.L. for SLHC
Power cables, opto-links, etc.	**0.6 %**	**x 5**	**3 %**
MCM (hybrid)	0.4 %	**x 5**	2 %
Sensor	0.7 %	x 1	0.7 %
Cooling; CF cylinders; module baseboard; etc.	0.6; 0.4; 0.2 %	**x ≈3;** x 1; x 1	2.4 %
Total	**3 %**		**8 %**
Silicon fraction	23 %		9 %

*crude estimate; no innovation

too big ⇔ innovate!

Material budget will explode at SLHC without innovations in powering, packaging, and cooling

For 50 ns bunch crossing, 5 times more channels would be insufficient

M. Weber, *Interconnects, Packaging and Power*

Total power consumption

affects cooling, material budget, packaging and more

Electronics of ATLAS Semiconductor Tracker SCT

6 M channels; 4 mW/channel ⇔ 24 kW power (excl. cable losses)

Estimate for SLHC tracker (strips only)

if 30 M channels; 2 mW/channel ⇔ 60 kW power

if 60 M channels; 4 mW/channel ⇔ 240 kW power

This is a power station not a tracker !

Must make any effort to reduce power

(must also watch power efficiency, which for independent powering would be far too low)

M. Weber, *Interconnects, Packaging and Power*

How many barrel modules need to be served ?

Start from straw man; calculate module number for two sensor sizes; apply weighting factor ½ for 1d sensors; normalize to 2112 SCT barrel modules; compare with table on previous slide

Layer	Radius [cm]	Length [cm]	# of modules 6.3x12.5 cm^2	# of modules 10x10 cm^2
L4/SS 2d	38	100	606	477
L5/SS 2d	49	100	782	616
L6/SS 2d	60	100	957	754
L7/LS 1d	75	190	2274	1791
L8/LS 1d	95	190	2880	2268
Total 2d			2345	1847
Total 1d			5154	4059
Weighted total			4922	3877
SCT/SLHC			2.3	1.8

Compare with the previous table ⇔ there are more than enough SCT cables to serve new tracker

Conclusions: Material constraint and large channel density suggest that evolutionary improvements will not work in some critical areas

- need new power distribution schemes
- need new approach to slow control of temperature and module voltage/current

and possibly

- need new hybridization technologies (see his slides)

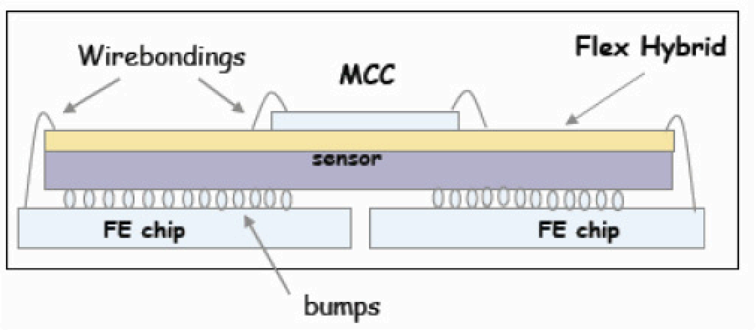
M. Weber, *Interconnects, Packaging and Power*

Packaging solutions

How to stack sensors; MCMs; chips; CF support; cables and cooling while connecting them electrically, thermally and mechanically ?

How to get the cables from hybrids to the end of the supermodule?

- **innovative example: ATLAS pixels**
  - sophisticated, crowded flex-hybrid
  - carbon-carbon support structures
  - bump-bonding of chips to sensors
  - direct cooling of chips



M. Weber, *Interconnects, Packaging and Power*

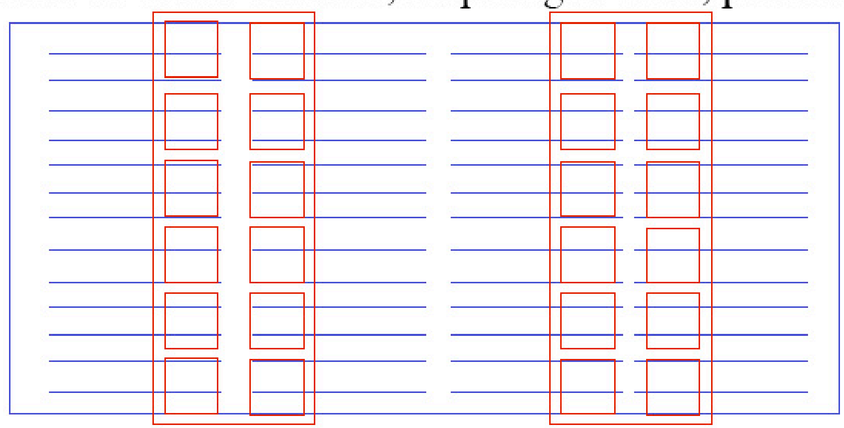
Packaging solution for SCT

Still very compact

- flex-hybrid with connectors
- separate optical readout for each module
- separate power for each module
- cooling pipes not integrated to structure

Sketch of a possible SLHC strip module

size: 63 mm x 125 mm; strip length: 3 cm, pitch 80 μm



The current solutions will simply not work anymore

M. Weber, *Interconnects, Packaging and Power*

Issues in Modules – Inner Radius Layers (2)

- Strip sensor sizes (… and may be above 1% can be negotiated in some cases)
- Modules and staves .. work together now to find common way forward
- Good focus on serial powering and DC/DC

Engineering

ATLAS Tracker Upgrade Workshop

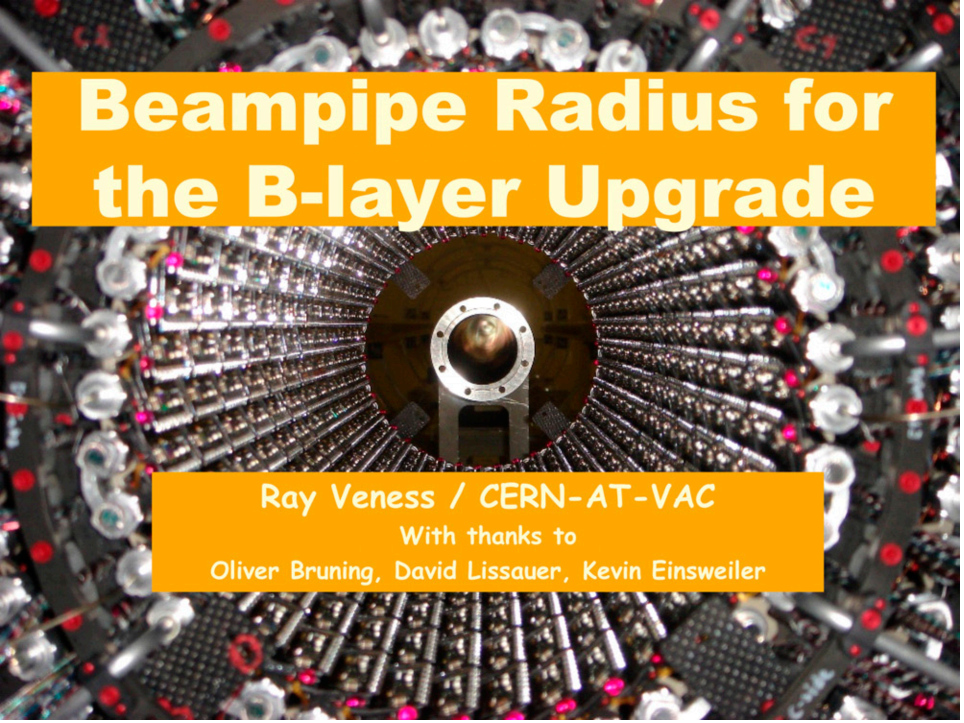
Engineering (14:00 ->17:40)

Chairperson: David Lissauer (*Department of Physics*)
Location:

	14:00	**Beampipe Radius for the ATLAS B-Layer Upgrade** (20') (Slides)	Raymond Veness (*CERN*)
	14:20	**An R&D Proposal for New Carbon Fibre Concepts to Simplify and Optimize the Thermal Management and Mechanical Design in the SLHC Pixel Detector** (20') (Slides)	Peter Mattig (*Physikalische s Institut*)
	14:40	**ATLAS - Barrel Constructions - Lessons** (25') (Slides)	Eric Perrin (*Section de Physique*)
	15:05	**EC - Mechanical Constructions** (25') (Slides)	Patrick Werneke (*NIKHEF*)
		15:30 TEA	
	16:00	**Mechanical Support for Barrel Staves** (20') (Slides)	David Lynn
	16:20	**Summary of Thermal Management Working Group Meeting** (30') (Introduction to Coolants ; Slides)	Georg Viehhauser
✦	16:50	**Assembly, Integration, Safety and Risk Management** (30') (Paper)	Heinz Pernegger (*CERN*)
✦	17:20	**Development of Involute Laminates for Integrated Module Support and Thermal Management** (20') (Slides)	Eric Anderssen (*Lawrence Berkeley National Laboratory (LBNL)*)

Outline (2)

- **Module Integration - Inner Layers (Strips)**
  - New concepts of sensor integration, self-supporting stave structures
  - Power supply: DC-DC near the sensors - new industrial developments; serial powering of staves
- **Engineering**
  - Radius of beam pipe probably unchanged - innermost pixel layer
  - Carbon fibre/foam support structure; outstanding property - cooling
  - Cooling - hot issue
- **Sensors and Electronics**
  - ASIC's design on new level of standardisation - e.g. tracker & LAr R/O; CMS co-operation (other partners?!); Very essential: costs!
    Man power needed urgently for architecture design, controllers, protocol design
  - 3D pixel collaborators - good progress - 6 EOI - new groups joining; rad-hard, fast, highly integrated structures, time-table
  - SSP group with new results



- Beam stay-clear 14mm
  - within the tracker region (±5 m) at injection
  - In forward regions, this may be higher for collision optics
- Survey Precision ~ 2.6mm
  - A given survey target in the tracker region was expected to be placed within 2.6mm of the nominal beam axis with a 2σ (95%) confidence, using the survey techniques planned for ATLAS
- Mechanical construction ~ 2.6mm
  - Tolerances on straightness, circularity, wall thickness, sag under self-weight etc
- Instabilities ~ 9.8mm
  - Stability of the cavern, movements due to electro-magnetic forces, thermal expansion

- Beampipe radius
  - An upgrade radius in the range 17~25 mm seems realistic
  - The most margin can be gained by understanding or even *controlling* the long term stability of the beampipe relative to the beam
- Beampipe – pixel clearance
  - Some, or all of the 9 mm clearance can be gained by design of the beampipe-pixel system
    - Heating during bakeout, mechanical stability, electro-magnetic effects may limit from the PIXEL side
- What to do?
  - Look at the mechanical stability of the beampipe in the first year
  - Follow-up on collimation, impedance, survey, vacuum physics, upgrade beam parameters
- When?
  - Some months with beam in ATLAS will be required to understand this mechanical stability issue… mid 2008 for a clear answer?

S.Stapnes, *Summary ID upgrade WS*

Aims of this proposal

- Simplify production, integration/less parts
- Reduce material
- Efficient thermal management

Directions of thinking:

Staves: alternative carbon materials

I. thermal conductivity in anisotropic fibres

II. carbon foam

Global support

III. Integration of stave and support

P.Mättig, *R&D Plan on (Pixel) Staves and Global Support*

I: Fibres - thermal conductivity

	Copper	Current	UHM fibres (K1100)	
		pixel	parallel	perpendic.
elasticity(Gpa)	125	97	931	6.9
density(g/cm**3)	8.9	1.73	2.2	2.2
thermal conduct. (W/mK)	400	27	1000	2.4

Note: depends on reinforcement content!

Ultra High Modulus fibres (UHM):

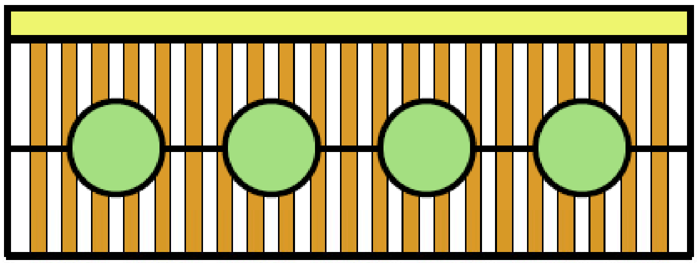
- heavy research for electronic packaging
- improved mechanical properties
- excellent thermal longitudinal conductivity (> Cu)

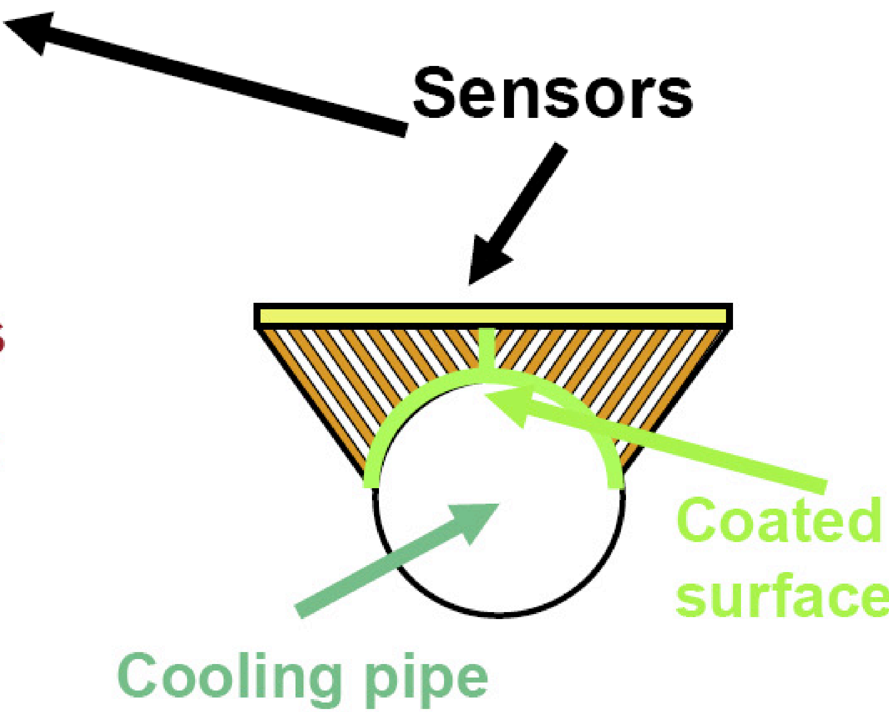
P.Mättig, *R&D Plan on (Pixel) Staves and Global Support*

I. Fibres: stave concepts

Early ideas as flavour

Currently discussing optimal geometry





Use anisotopic properties

- **Improved heat transport**
- **symmetric**
- **compact construction**

P.Mättig, *R&D Plan on (Pixel) Staves and Global Support*

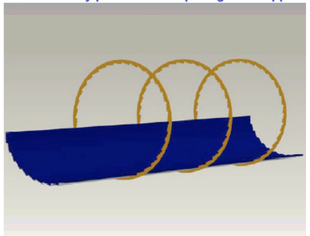
III. Global support

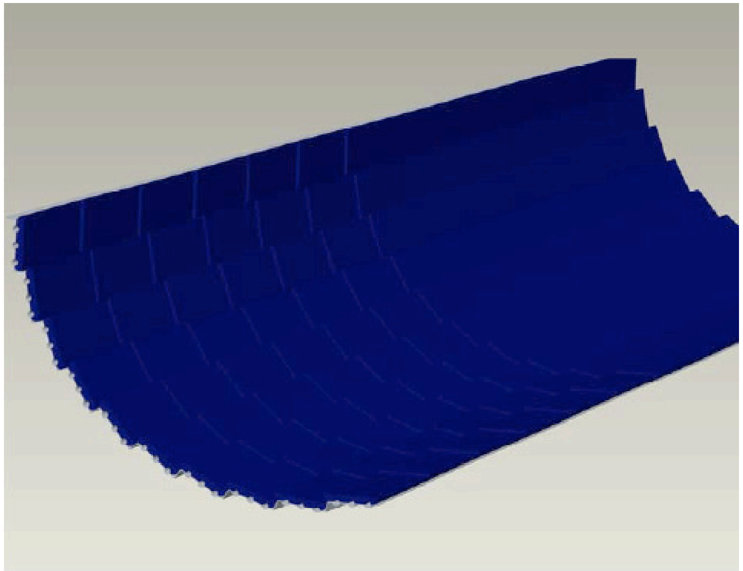
Increased stiffness and reduced weight of new material:

- omit separate shells
- staves themselves make the shell!

**==> less weight,
less material**

Staves held in place by stiffening rings
..... already part of current pixel global support





P.Mättig, *R&D Plan on (Pixel) Staves and Global Support*

Summary & Outlook

- Recent progress in carbon materials: lighter, more compact support structures

  IF works: reduce weight by factor 3 - 8
- R&D over next year:
  - Feasibility, production, pricing
- beyond 2007:
  - Full scale
  - optimization for detector & electronics design
- Should be there for SLHC (b-layer?)

P.Mättig, *R&D Plan on (Pixel) Staves and Global Support*

Summary of thermal management working group meeting, December 6

Presentations

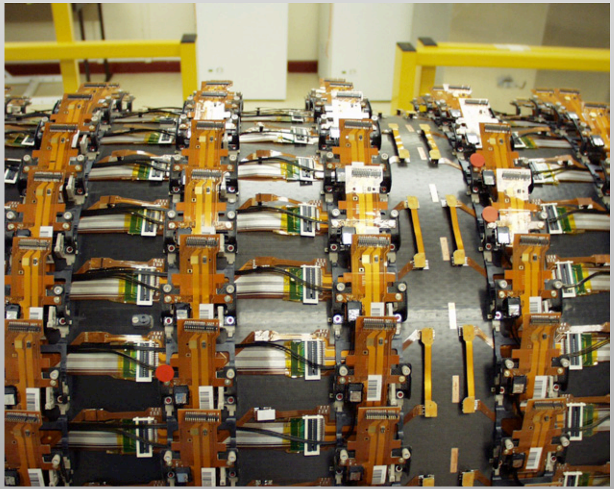
- Introduction (G. Viehhauser, Oxford)
- Reutilisation of present tubing plant (G.V.)
- Status reports for different coolants:
  - Light fluorocarbons (G. Hallewell, CPP Marseille)
  - CO_2 (A. Colijn, NIKHEF)
- Flow control with thermostatic expansion valves (N. Hessey, FOM/NIKHEF)
- Recent experience from cooling system commissioning (R. Bates, Glasgow)
- From current cooling installation to future CS upgrade for ATLAS ID (V. Vacek, CTU, Prague)
- Thermal Management Issues for Stave Structures (C. Haber, LBNL)

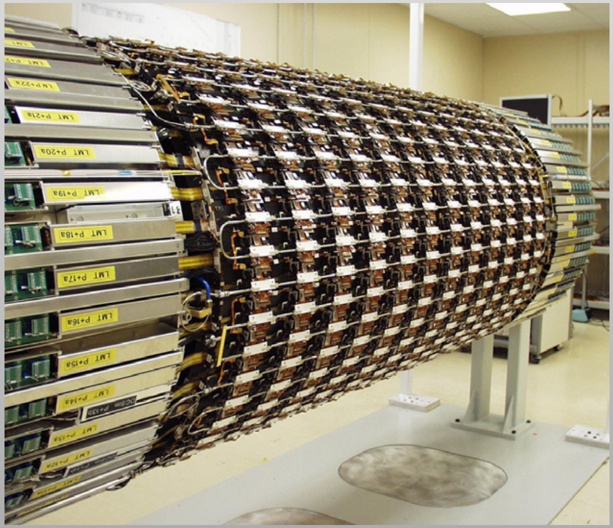
Conclusions

- Cooling has not been a high profile part of the project
  - Considered a service that should just work
- However, the cooling of the SCT/pixels is complex and vital to run the systems
- More earlier testing of all components should have been performed
  - Time in the schedule should have been made for system tests
  - Space in SR1 should have been available for reception testing
- We will get there: but if something will go wrong – it has

Overview of assembly steps

- Add brackets (Uni-Genève)
    - 8 flavours (2 per barrel) CFRP laminate
- Add harnesses (RAL)
- Add cooling units (RAL)





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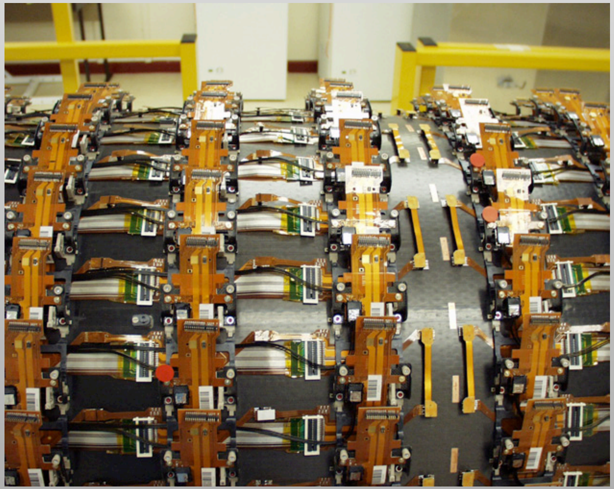
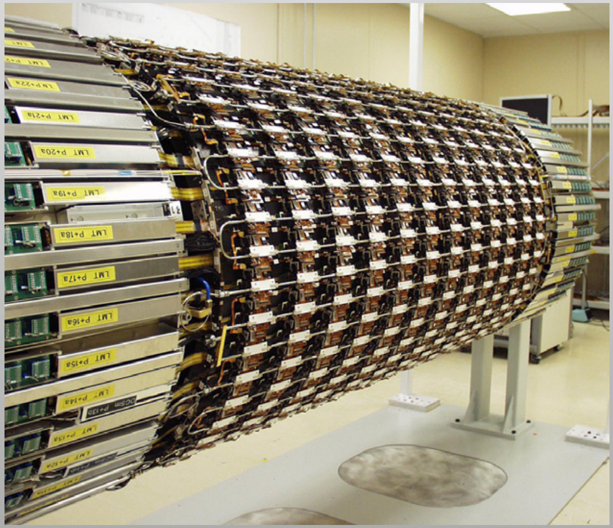




Conclusion

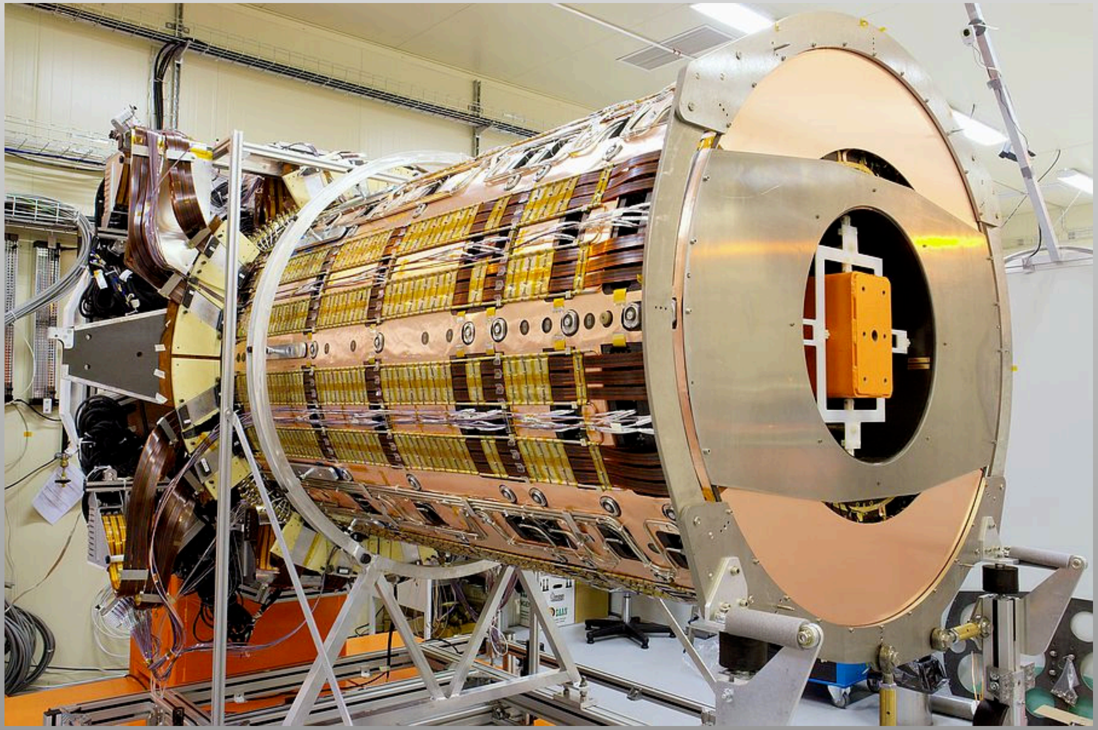
We have to use past experience in new designs.

Barrel structures for the upgrade are certainly feasible.

SCT EC Mechanical Construction

Summary:

The SCT EC is a state of the art detector. And I would not hesitate to copy most of the designs and techniques used for the Upgrade



Issues in Engineering session

- Thermal management and cooling working group well underway
- Engineering can slowly start with the strawman layout – but very limited since almost all engineers are fully engaged in the installation

Sensors and Electronics

ATLAS Tracker Upgrade Workshop

Friday 08 December 2006

Sensors and Electronics (08:30 ->13:00)

Chairperson: Nanni Darbo (*Universita degli Studi di Genova Dipart. di Fisica*)
Location:

08:30	**Summary of FE Electronics** (35') (Slides)	Philippe Farthouat (*CERN*)
09:05	**Towards a Next Generation Pixel FE Chip** (30') (Slides)	Kevin Einsweiler (*Lawrence Berkeley National Laboratory (LBNL)*)
09:35	**ABC - Next Status Report** (30') (Slides)	Wladyslaw Dabrowski (*AGH Univ. of Science & Technology Phys.&Appl.Comp.Sc.*)
10:05	**Radiation Hardness Evaluation of the Silicon on Sapphire Technology and the Design of the Link-on-Chip** (25') (Slides)	Jingbo Ye, Ping Gui (*SMU*)
10:30	COFFEE	
11:00	**3D Status and Summary** (30') (Slides)	Cinzia Da Via' (*Brunel University*)
11:30	**Preliminary Results with Miniature Microstrip p-type Detectors after Neutron Irradiation to SLHC Doses** (15') (Slides)	Gianluigi Casse (*Department of Physics*)
11:45	**P-type Sensor Development and Irradiation** (15') (Slides)	Kazuhiko Hara (*Institute of Physics*)
12:00	**Development of Non-inverting Silicon Strip Detectors for the ATLAS ID Upgrade** (30') (Slides)	Hartmut Sadrozinski
12:30	**CMS Perspectives for a Tracker Upgrade** (30') (Slides)	Tilman Rohe (*Nuclear and Particle Physics Department*)

Outline (2)

- ***Module Integration - Inner Layers (Strips)***
  - ***New concepts of sensor integration, self-supporting stave structures***
  - ***Power supply: DC-DC near the sensors - new industrial developments; serial powering of staves***

- ***Engineering***
  - ***Radius of beam pipe probably unchanged - innermost pixel layer***
  - ***Carbon fibre/foam support structure; outstanding property - cooling***
  - ***Cooling - hot issue***

- ***Sensors and Electronics***
  - ***ASIC's design on new level of standardisation - e.g. tracker & LAr R/O; CMS co-operation (other partners?!); Very essential: costs!***
    Man power needed urgently for architecture design, controllers, protocol design
  - ***3D pixel collaborators - good progress - 6 EOI - new groups joining; rad-hard, fast, highly integrated structures, time-table***
  - ***SSP group with new results***

Electronics session

Electronics Session

Wednesday 06 December 2006
from **09:00** to **13:00**
at **Oliver Lodge Laboratory (*Video Conference Suite*)**
chaired by: ***Alex Grillo, Philippe Farthouat***

Wednesday 06 December 2006 |

Wednesday 06 December 2006

top

09:00	Presentation and discussion of the document on R&D (1h00') (Slides ; document)	Philippe Farthouat (*CERN*) , Alexander A. Grillo (*Santa Cruz Institute for Particle Physics, University of California, Santa Cruz*)
10:00	R&D program at CERN (30') (Slides)	Francis Anghinolfi (*CERN*)
10:30	Effect of power schemes on material budget (30') (Slides)	Marc Weber (*Rutherford Appleton Laboratory*)
11:00	Coffee break	
11:15	New techniques for galvanic isolation of control signals (30') (Slides)	Satish Dhawan (*Yale University*)
11:45	Organising the measurement effort of SiGe processes (30') (Slides)	Mitchell Franck Newcomer (*Departm.of Physics & Astronomy*)
12:15	Irradiation test results of OKI SOI technology (20') (Slides)	Yoichi Ikegami (*High Energy Accelerator Research Organization (KEK)*)
12:35	ABCnext presentation (30') (Slides)	Francis Anghinolfi (*CERN*)

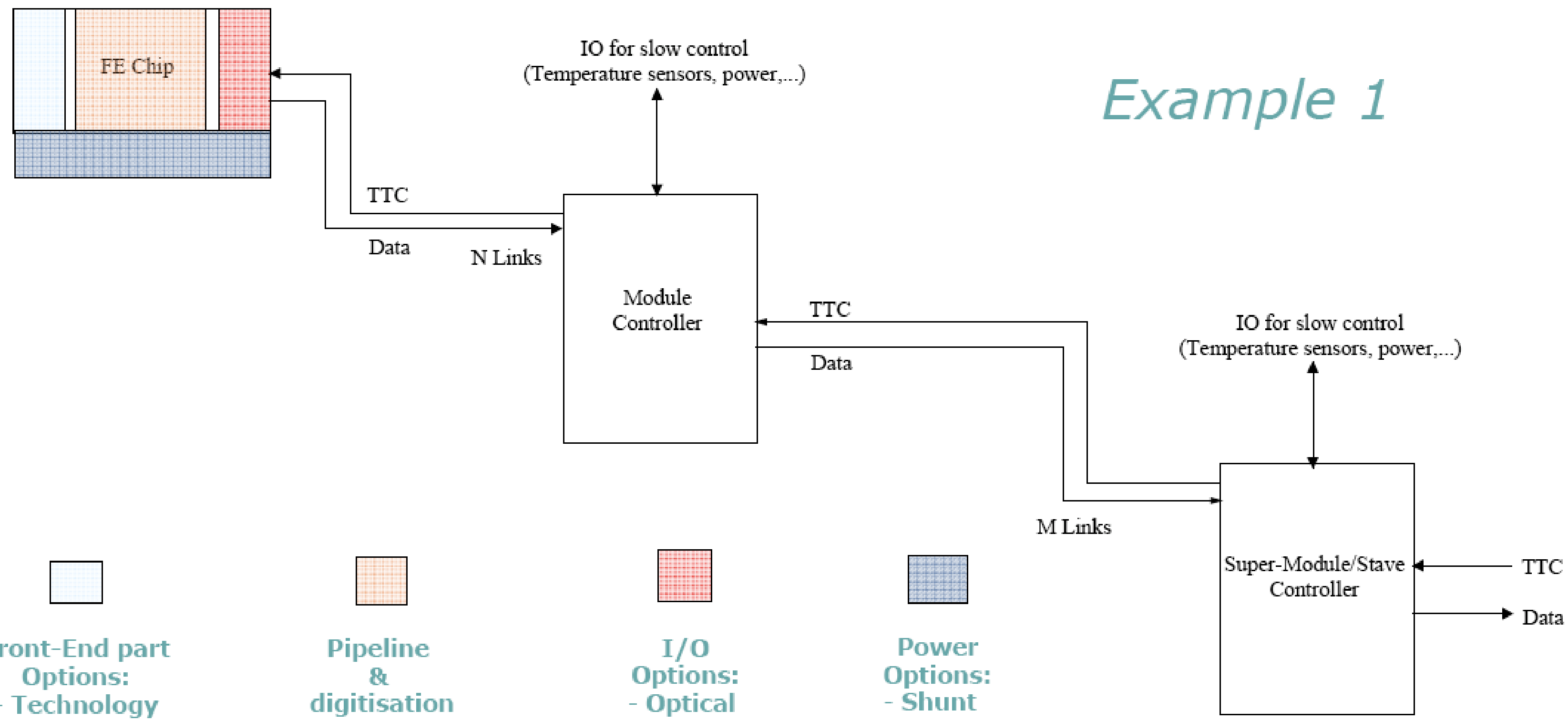
- More than 20 people attended

Constraints for Upgrade

- We have to fit in an existing detector
  - Limits the solutions
  - May need to use existing services
- New ASICs needed
  - Tracker
  - Calorimeter if an upgrade is to be done
- New technologies have very high NRE costs
  - Reduce the number of ASICs to be designed
    - At least the number of mask sets
  - Points towards common solution as much as possible
    - Including with other experiments

Basic Building Blocks

Example 1



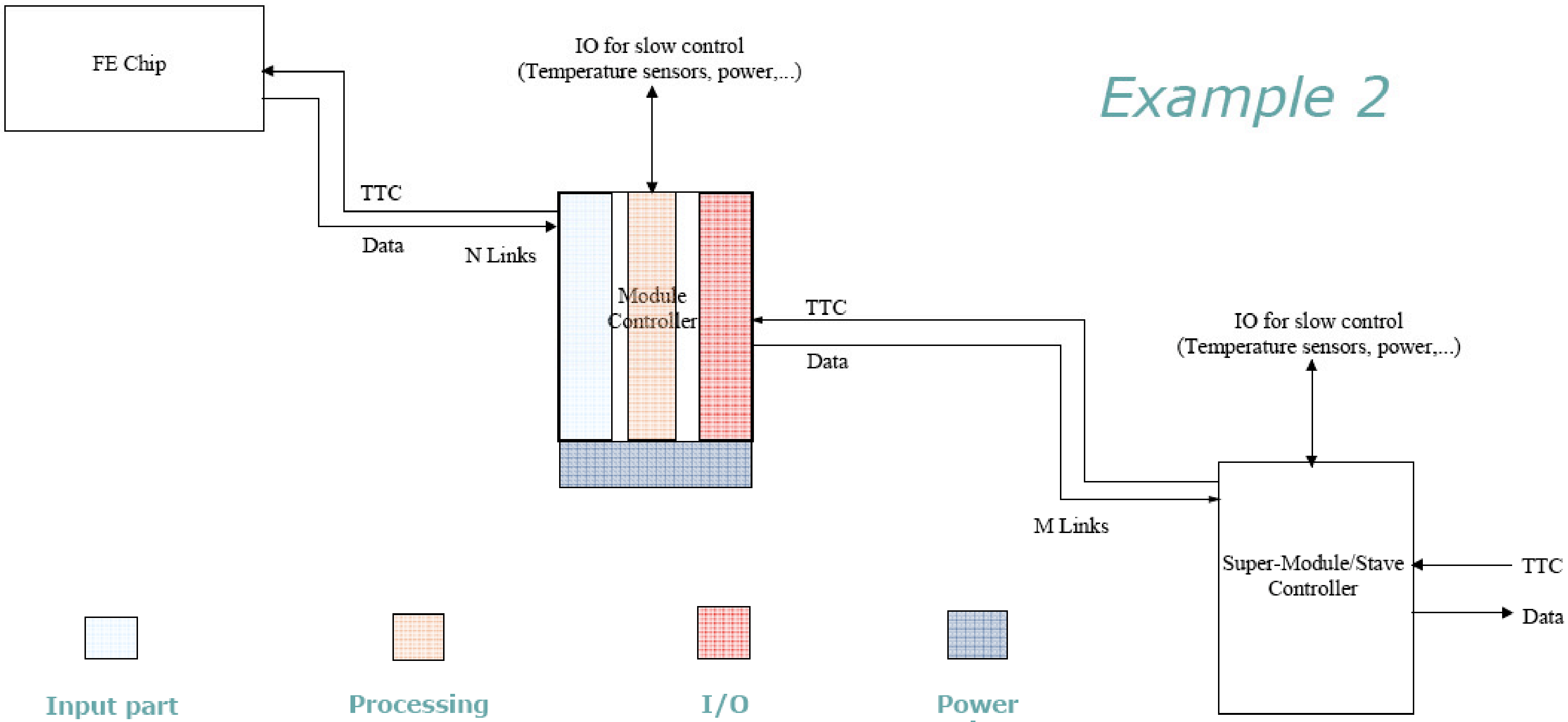
Front-End part
Options:
- Technology (CMOS, SiGe)
- Pixel/Strip

Pipeline & digitisation
Options:
- Analog or digital pipeline
- Binary vs Digital
- #bits?
- Data compression
- Data Format

I/O
Options:
- Optical vs Copper
- Serial/Parallel
- AC or DC coupling
- Bandwidth
- TTC interface
- Slow Control Interface

Power
Options:
- Shunt or Linear Regulators
- DC-DC

Basic Building Blocks



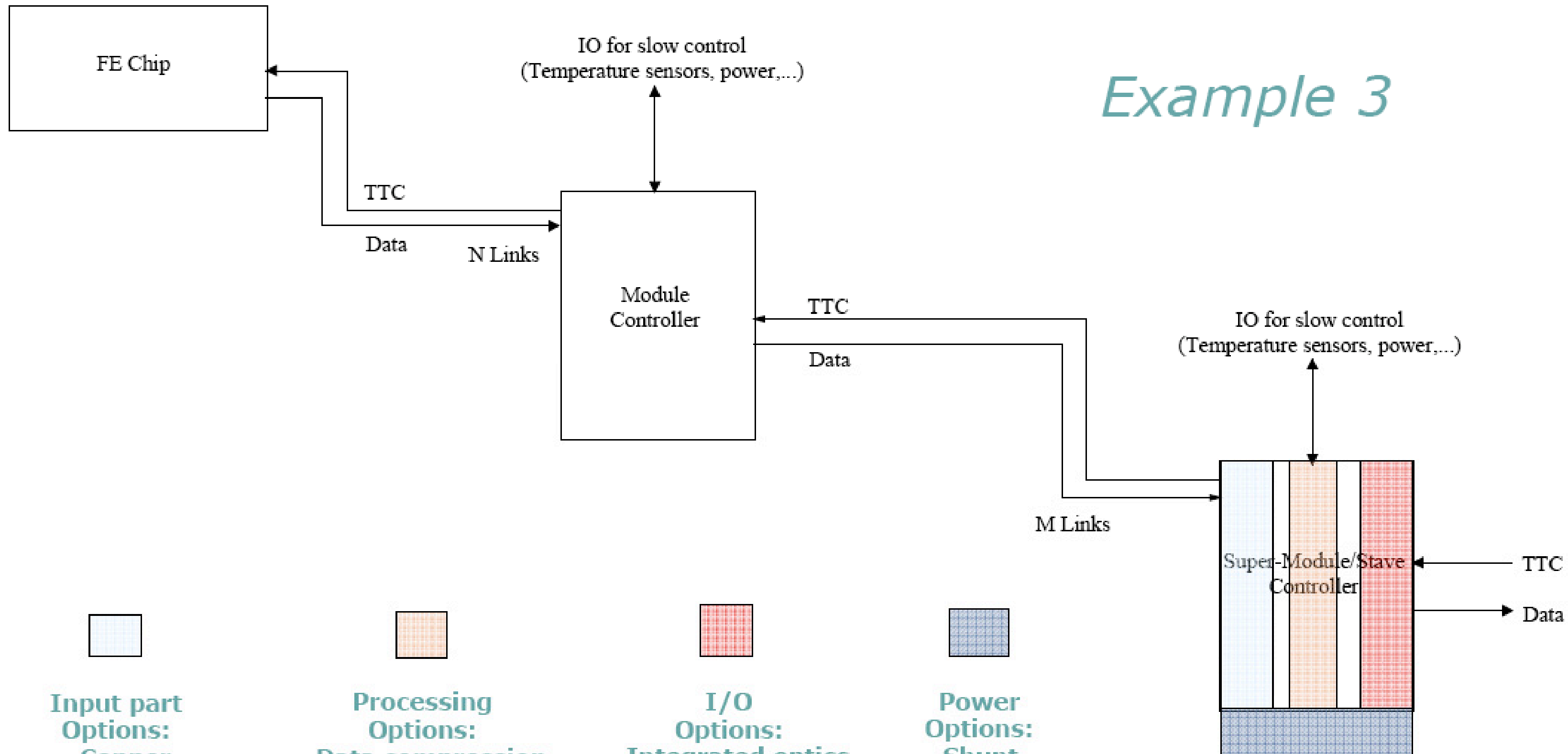
Input part
Options:
- Copper
- Optical
- Bandwidth
- Serial vs parallel

Processing
Options:
- Data compression
- Data Format
- DCS stuff

I/O
Options:
- Optical
vs
Copper
- Serial vs Parallel
- etc.

Power
Options:
- Shunt
or
Linear
Regulators
- DC-DC

Basic Building Blocks



Input part
Options:
- Copper
- Optical
- Bandwidth
- Serial vs parallel

Processing
Options:
- Data compression
- Data Format
- DCS stuff

I/O
Options:
- Integrated optics
- Several Gbit/s Serial
- Parallel
- Redundancy
- Error correction

Power
Options:
- Shunt
or
Linear
Regulators
- DC-DC

Rough Schedule

Detector ready					*Beginning Y (01-01-2016)*
Production start				*Beginning Y-4 (01-01-2012)*	
Final design			*Y-6 and Y-5 (2010 and 2011)*		
Decision		*End of Y-7 (31-12-2009)*			
R&D	*Now → end Y-7 (2007 → 2009)*				

On-going R&D in ATLAS

- Radiation test of opto-electronics devices
- ABC-Next (including a 130 nm chapter)
- SiGe evaluation (tracker + calorimeter)
- Power distribution (EoI)
- Missing:
  - Architecture
  - "Controllers"
  - Protocols (data, control and timing)
  - ***Needed before final ABC-Next or Pixel chip design start***

Next

- CMS is facing the same kind of problems
- There will be a common workshop ATLAS-CMS devoted to electronics
  - 19-21 March 2007 at CERN
  - Announcement and program before Xmas
    - Introduction - Machine, ATLAS plans, CMS plans
    - Power systems, opto-links, services
    - Tracker read-out architectures
      - On-going R&D
      - Triggering with trackers
    - Calorimeters, muons, trigger/DAQ
    - Identify/plan potential common building blocks

Summary

- NRE costs for new ASICs push us to minimise the number of different designs and to try and find common solutions
- ATLAS to organise itself to make sure that all R&D needs in electronics are covered and that we get what's needed from non purely ATLAS R&D efforts
- Several R&D on electronics started. Missing work on architecture, controllers, ...

Electronics Summary

- NRE costs for new ASICs push us to minimise the number of different designs and to try and find common solutions
- ATLAS to organise itself to make sure that all R&D needs in electronics are covered and that we get what's needed from non purely ATLAS R&D efforts
- Several R&D on electronics started. Missing work on architecture, controllers, ...

3D-Atlas meeting

Expression of interest from several institutes and Fabrication Laboratories

Organisers: G. Darbo, C. DaVia. Discussion chair M. Tyndel

2006

ATLAS 3D Sensor R&D Meeting

Date/Time: Wednesday 06 December 2006 from 09:00 to 13:10
Location: Chadwick Building, 42 (Barkla Lecture Theatre)
Chairperson: Cinzia Da Via (*Brunel University*) ,Nanni Darbo (*Universita degli Studi di Genova Dipart. di Fisica*) Giovanni Darbo & Cinzia Da Vià

Wednesday 06 December 2006 12:10->12:50 Round table (Barkla Lecture Theatre)

Wednesday 06 December 2006

09:00	Introduction and Welcome (05') (Slides)	Nanni Darbo (*Universita degli Studi di Genova Dipart. di Fisica*)
09:05	Next Steps and Issues of 3D R&D in ATLAS (20') (Slides)	Cinzia Da Via (*Brunel University*)
09:25	Latest results and future plans from Laboratories: Brunel/Mancester (15') (Slides)	Stephen Watts (*Brunel University*) , Cinzia Da Via (*Brunel University*)
09:40	Latest results and future plans from Laboratories: Stanford Nanofabrication Facility/SLAC (15') (Slides)	Chris Kenney (*Molecular Biology Consortium*) , Sherwood Parker (*University of Hawaii*)
09:55	Latest results and future plans from Laboratories: New Mexico (15') (Slides)	Sally Seidel (*University of New Mexico (UNM)*) , Martin Hoeferkamp (*Department of Physics and Astronomy*)
10:10	Latest results and future plans from Laboratories: CNM/Glasgow (15') (Slides)	Giulio Pellegrini (*Centro Nacional de Microelectronica (CNM-IMB)*)
10:25	Expression of Interest: Bonn (05') (Slides)	
10:30	Expression of Interest: Freiburg (05') (Slides)	Ulrich Parzefall (*Fakultaet fuer Physik*)
10:35	COFFEE	
11:00	Expression of Interest: Genova (05') (Slides)	Roberto Beccherle (*Sezione di Genova*) , Nanni Darbo (*Universita degli Studi di Genova Dipart. di Fisica*)
11:05	Expression of Interest: LBL (05')	Kevin Einsweiler (*Lawrence Berkeley National Laboratory (LBNL)*) , Mauricio Garcia-Sciveres (*Physics Division*)
11:10	Expression of Interest: Oslo (05') (Slides)	
11:15	Expression of Interest: Prague (05') (Slides)	Josef Uher (*Czech Technical University in Prague*)
11:20	Presentation from Industrial Partners: SINTEF (25') (Slides)	
11:45	Presentation from Industrial Partners: IRST (25') (Slides)	

http://indico.cern.ch/conferenceDisplay.py?confId=9185

~50 participants

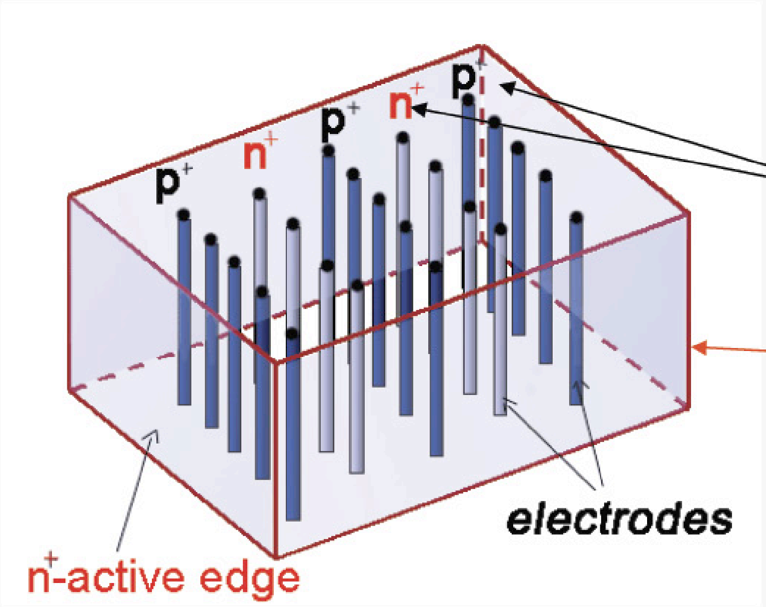
10 institutions presenting results and expression of interest for the future activities

4 processing facilities: CNM, IRST, SINTEF, Stanford

AIM: common 3D sensors R&D proposal for the upgrade (and possibly the B-layer replacement)

Basic 3D design: double column with active edges.
However alternative 3D sensor designs will also be explored

Some history..3D silicon sensors were originally proposed by Sherwood Parker and are presently fabricated at Stanford by J. Hasi (Brunel/Manchester) and C. Kenney (MBC)



Combine traditional VLSI processing and MEMS (Micro Electro Mechanical Systems) technology.

Both electrode types are processed inside the detector bulk instead of being implanted on the Wafer's surface.

The edge is an electrode (following an idea by C. Kenney). Dead volume at the Edge < 5 microns! Essential for forward physics experiments and material budget

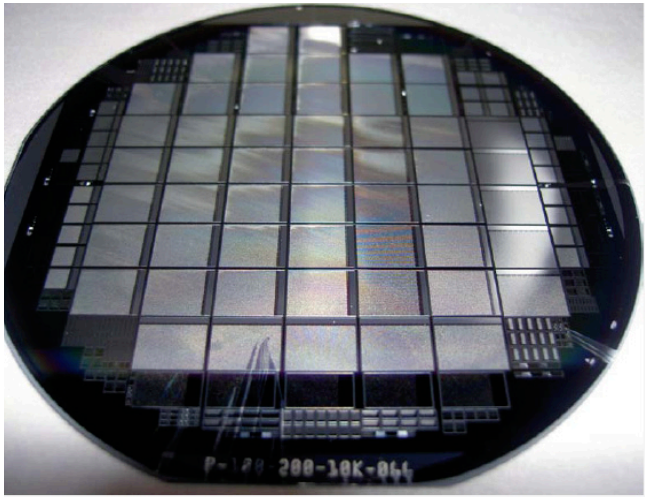
3DC collaboration was formed in January 06
Core Members: Brunel/Manchester, Hawaii Oslo University, Sintef and Stanford (MBC)

Ongoing successful collaboration with Praha Technical University, Bonn and LBL

1. NIMA 395 (1997) 328
2. IEEE Trans Nucl Sci 464 (1999) 1224
3. IEEE Trans Nucl Sci 482 (2001) 189
4. IEEE Trans Nucl Sci 485 (2001) 1629
5. IEEE Trans Nucl Sci 48 6 (2001) 2405
6. CERN Courier, Vol 43, Jan 2003, pp 23-26
7. NIM A 509 (2003) 86-91
8. MIMA 524 (2004) 236-244

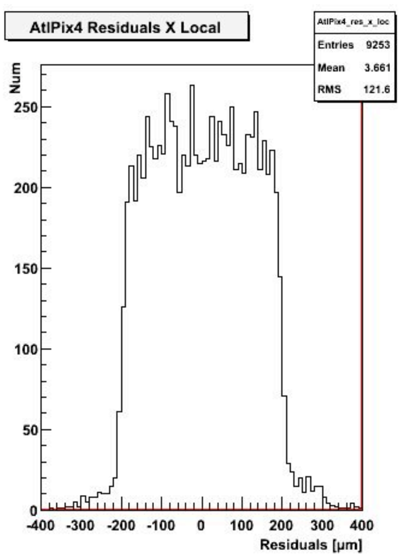
Very recently we produced some Encouraging results →

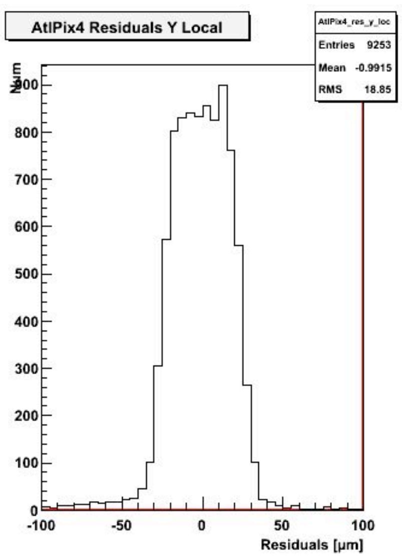
3D pixel testbeam



3D wafer

test beam setup



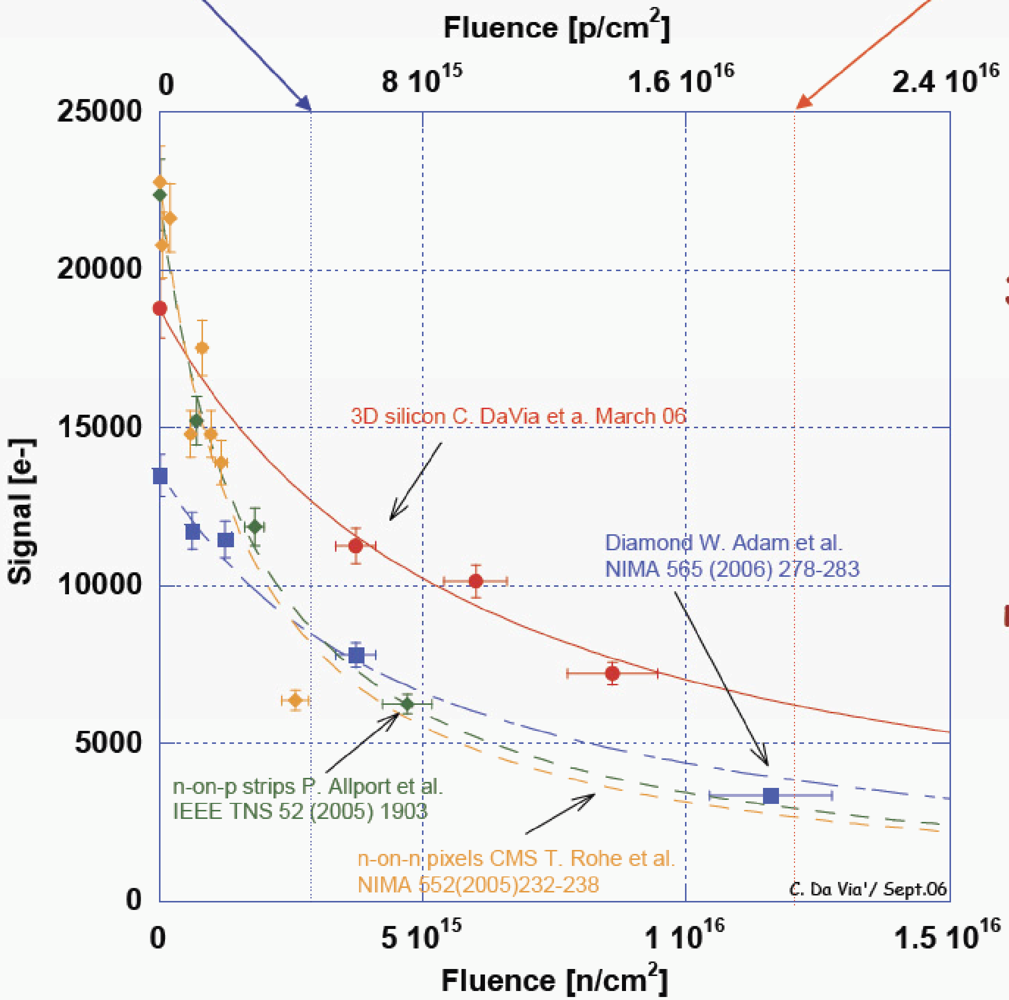


spatial resolution

Radiation Hardness

3×10^{15} p/cm^2 =
10 years LHC at 10^{34} cm^{-2}s^{-1}
At r=4cm and target for b-layer replacement

1.8×10^{16}p/cm^2 =
10 years SLHC at 10^{35}cm^{-2}s^{-1}
At r=4cm



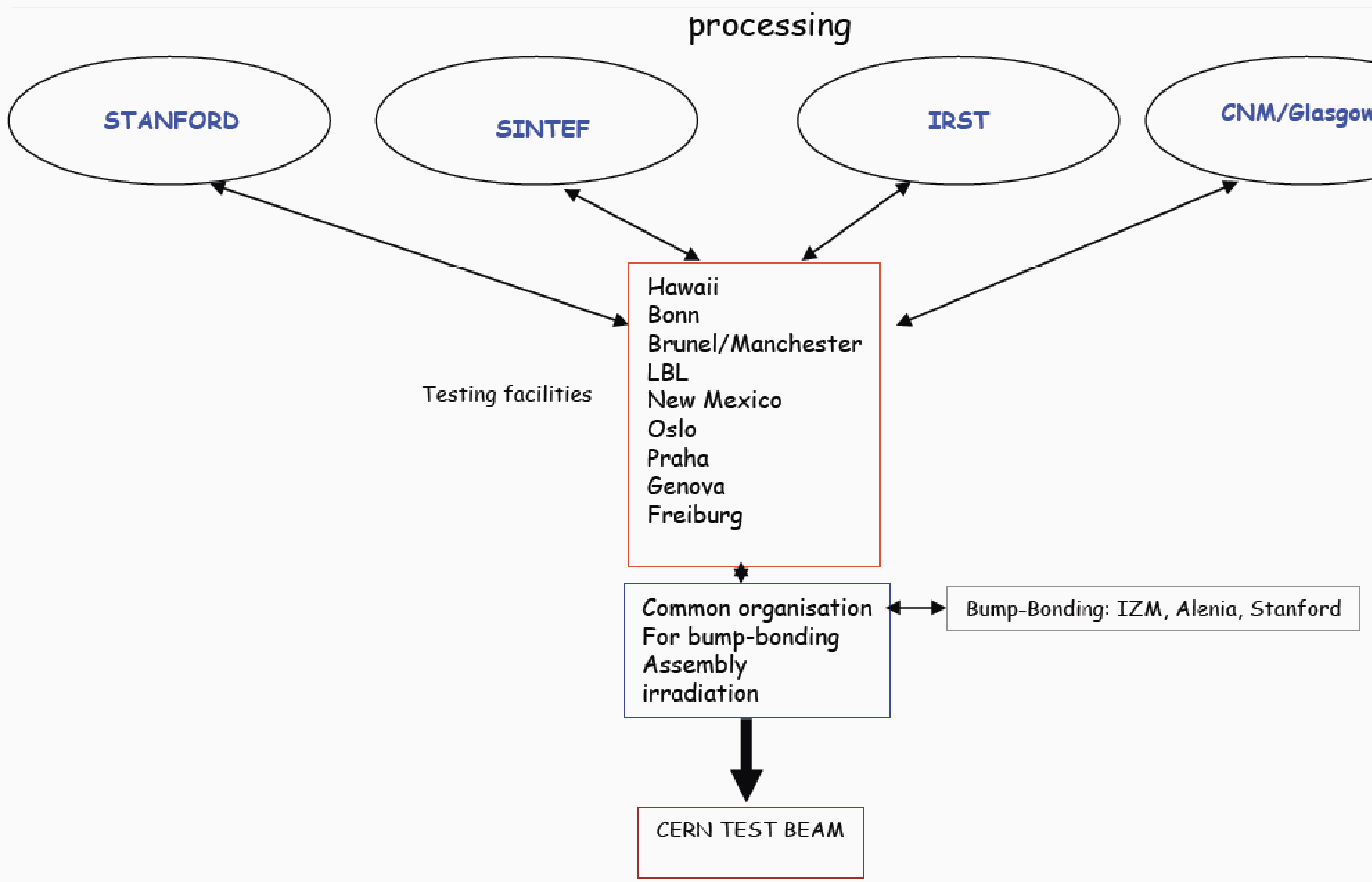
Fluence [n/cm^2]	Bias voltage [V]	
3D		
3.74×10^{15}	60	**B-layer**
5.98×10^{15}	100	
8.60×10^{15}	160	**upgrade**
n-on-n pixels CMS		
~3×10^{15}	600	

We can expect:

Twice as much charge
Factor 10 less bias

Cinzia Da Via' - Brunel/Manchester- Atlas 3D-summary Liverpool - December 2006

Project Structure



Dear All,

Some of us cannot attend the phone conference next week so we would suggest to postpone our meeting directly to Wednesday the 28th of February in the afternoon at Cern. The meeting would then take place during the Atlas ID week when, hopefully, most of us will already be physically in Geneva. The Agenda would then be:

-comments on the draft of the new 3D-upgrade proposal (which will be circulated shortly)
-share of responsibilities and strategies for the various tests
-status of the processing from industrial partners
-organization of the logistics for the test beam (group formation, contacts, beam area infrastructures, etc.)
contacts with bump-bonding industries, availabilities of boards-test benches vailability for pre-test)
-organization of the logistics for the radiation hardness tests (group formation, booking of radiation facilities, proposals for common tests)
-web page - organization, layout, url
-proposed dates for the next meetings and review of 3D calendar
-AOB

We hope this arrangement suits everyone better. The meeting room details will be circulated as soon as possible.

Cheers,

Giovanni and Cinzia

SSD Development for the ATLAS Upgrade Tracker

ATL-P-MN-0006 v.1

Development of non-inverting Silicon strip detectors for the ATLAS ID Upgrade

KEK, Tsukuba, Liverpool, Lancaster, Glasgow, Sheffield, Cambridge, QML, Freiburg, MPI, Ljubljana, Prague, Barcelona, Valencia, UC Santa Cruz, BNL, PTI

Presented by

Hartmut F.-W. Sadrozinski, SCIPP UC Santa Cruz

Organization of SSD R&D Project:

Coordination: **P. Allport, H. Sadrozinski, Y. Unno**

Specification / Procedures (1rst drafts exist)

Electrical characterization *(A. Chilingarov, K. Hara, H. Sadrozinski)*

CCE with mini.ion. Particles *(G. Casse, U. Parzefall, S. Marti)*

Laser set-ups *(P. Kodys, K. Hara)*

Procurement / Operations

Detectors (1rst drafts exist) *(P. Allport, M. Lozano, N. Unno, H. Sadrozinski)*

Irradiations *(S. Terada, M. Mikuz): p (CERN), n (Ljubljana), π (PSI)*

Beam Test *(Y.Unno, Z. Dolezal): DESY, LBNL(?), CERN*

Electronics / associated infrastructure *(J. Carter, Y. Ikegami, A. Grillo, W. Dabrowski)*

Pixel contact *n.n.*

H.F.-W. Sadrozinski, ***SSD Development for the ATLAS Upgrade Tracker***

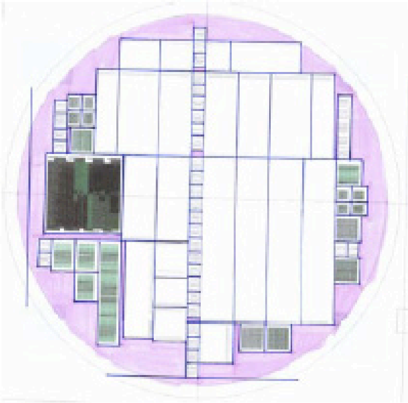
SSD Development for ATLAS Upgrade Tracker

Institution	P-type SSD	Strip Isolation	HV design	Modules constr.	Mech. Structures cooling	Hybrids,Readout	Electr. Char.	Laser CCE	CCE	Trapping	Oper. Param.
KEK	x	x	x	x	x	x	x	x	x	x	
Tsukuba						x	x	x	x	x	x
Liverpool	x	x		x	x		x	x	x	x	
Lancaster							x		x		x
Glasgow				x			x	x?	x	x?	
Sheffield					x	x	x		x		
Cambridge						x	x		x		
QML				x			x				
Freiburg				x		x		x	x		
MPI	x	x	x				x				
Ljubljana							x	x	x	x	
Prague							x	x	x		
Barcelona	x	x	x	x		x	x		x		
Valencia	x	x		x		x	x		x		
Santa Cruz									x	x	x
BNL	x	x	x								
PTI	x	x					x	x		x	

H.F.-W. Sadrozinski, *SSD Development for the ATLAS Upgrade Tracker*

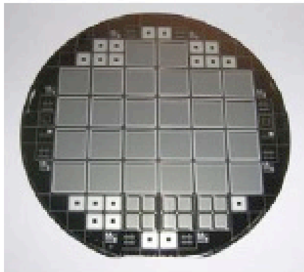
RD50 Test Sensors

6" : Micron

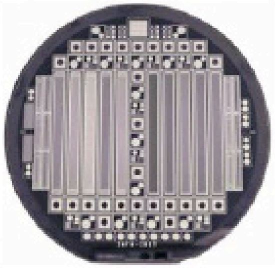


4" : Micron

CNM



IRST



RD50 Common Project with Micron (6")

Fab'd of (total)

Diameter	Type	Orientation	Silicon	Ohm-cm	Thickness (µm)	No. Of wafers	Structure
6 inch	P-Type	<100>	FZ	11000	300	7 (36)	N – P
6 inch	P-Type	<100>	MCZ	1000	300	7 (25)	N – P
6 inch	N-Type	<100>	MCZ	500	300	4 (20)	P – N
6 inch	N - Type	<100>	FZ	3000	300	(5)	P – N
6 inch	N - Type	<100>	MCZ	500	300	2 (5)	N – N
6 inch	N - Type	<100>	FZ	3000	300	2 (5)	N - N

Expect Micron sensors as X-mas 2006 presents

H.F.-W. Sadrozinski, *SSD Development for the ATLAS Upgrade Tracker*

SSD Development Road Map (dates depend on funding)

a) Technology development

Using existing test SSD or existing masks (RD50, HPK)

Decide on wafer type and isolation.	Summer 2007

b) Demonstrator Short Strip Sensor & Mechanical Prototypes

Verify technology (radiation campaign).

Supply sensors for module construction.	Fall 2007
Decide technology and geometry for short and long strips.	Spring 2008
c) Mechanical Prototypes for short/long strips	Fall 2007

d) Prototype electrically active sensors for modules (“pre-production”)

long sensors	
“Final” geometry, tested for module integration	Winter 2009
Radiation campaign	Summer 2009
wedge sensors	
“Final” geometry, tested for module integration	Winter 2009
Radiation campaign	Summer 2009
short sensors	
“Final” geometry, testedfor module inegration	Spring 2009
Radiation campaign	Summer 2009

H.F.-W. Sadrozinski, *SSD Development for the ATLAS Upgrade Tracker*

Sensors

- 3D interesting
- New measurements for n on p
- What about planar PIXEL sensors?

Summary of summary of some summaries

The Upgrade Work is so far successful fulfilling some of overall goals behind it:

- An ATLAS framework for R&D work such that ATLAS expertise continue to work to improve the experiment
- Well integrated with current detector work and TC – a healthy focus on some of the more difficult topics
- Useful for outside groups for funding requests and work planning
- We can interface to the machine, CMS and various planning committees in a coherent way
- But clearly not yet uniformly attended in ATLAS …. leading to some concerns

Lot of good initiatives, seeing R&D proposals, first results and good talks

- A framework for an ID layout (strawman) and a schedule appearing
- We have to accept that there are underlying uncertainties relate to physics goals, machine parameters, detector performance and ultimately the detector changes needed
- Need further unification in module/stave concepts I think and a more developed B-layer plan – and more development of the engineering - but let us get the current ID under control first

- *Organisation*
  - *News from the machine (bunch spacing, low β - hardware ...)*
  - *LAr forward region - impact of high luminosity; modifications/upgrade - necessary/possible (?)*
  - *Steering group - Status of R&D, timetable 2007*
- *Layout & Simulation*
  - *Layout versions ⇔ material, services (not compromising functionality)*
    - innovations unavoidable
  - *Simulation (material, performance ...) - some progress, FATRAS (MPI);*
    Full simulation and reconstruction needed;
    ⇒ pixel layout provides improvements, thin Si sensors!
    ⇒ new support structures
- *Module Integration - Inner Layers (Pixel)*
  - *Elimination of inefficiencies - active edge silicon detectors (thinner)*
  - *Development: thinner, new interconnection of FE-electronics - sensors;*
    trend 3D structures: less material, less power consumption, faster R/O;
    - following the progress of chip makers, using new technologies
  - *GOSSIP: a new and potentially better vertex detector for ATLAS*
- *Module Integration - Inner Layers (Strips)*
  - *New concepts of sensor integration, self-supporting stave structures*
  - *Power supply: DC-DC near the sensors - new industrial developments;*
    serial powering of staves
- *Engineering*
  - *Radius of beam pipe probably unchanged - innermost pixel layer at 4-5cm*
  - *UHM fibre/foam support structure; outstanding property - cooling*
  - *Cooling - hot issue*
- *Sensors and Electronics*
  - *ASIC design on new level of standardisation - e.g. tracker & LAr R/O;*
    CMS co-operation (other partners?!); Very essential: costs!
    Man power needed urgently for architecture design, controllers, protocol design
  - *3D pixel collaborators - good progress - 6 EOI - new groups joining;*
    radiation hard, fast, highly integrated structures, time-table
  - *SSP group with new results - established sub-collaboration*

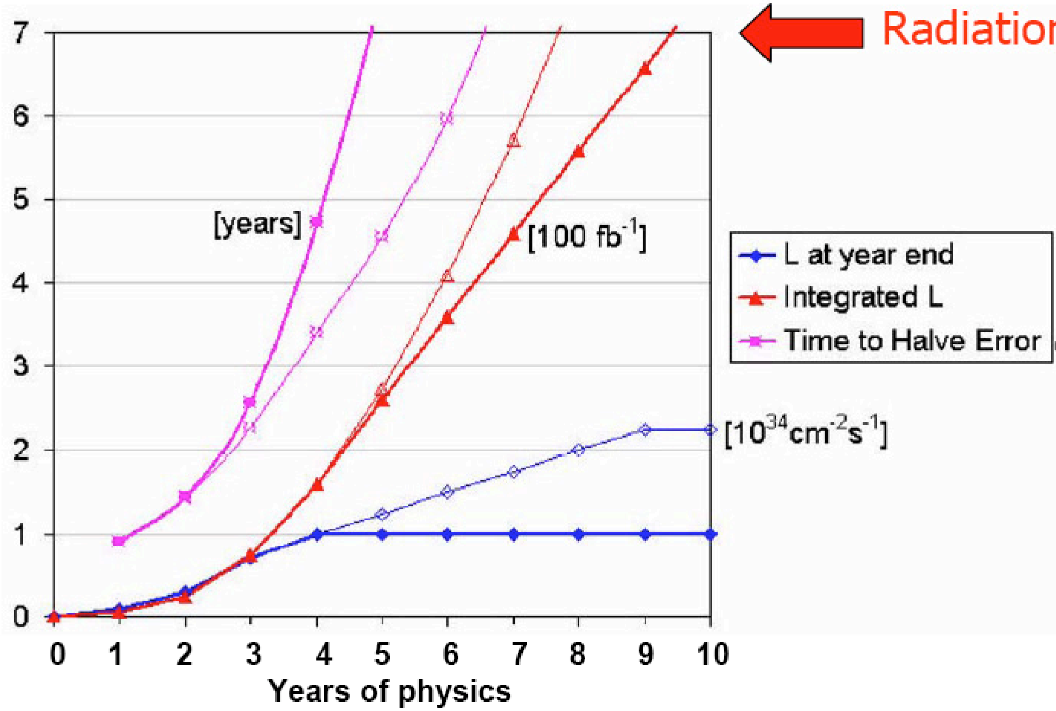
Backup

Maximize the integrated luminosity (1/6)

Getting fast the maximum integrated luminosity in LHC

⇒ implementing fast the SLHC

⇒ R & D for the SLHC is urgently needed !



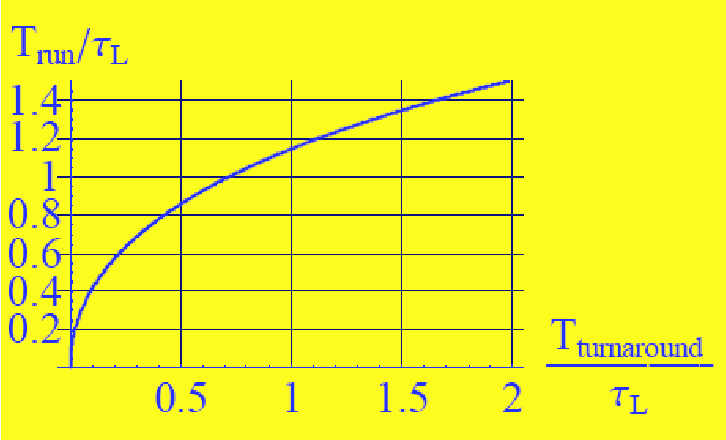
- Due to the high radiation doses to which they will be submitted, the life expectancy of LHC IR quadrupole magnets is estimated to less than 10 years
- Depending on the luminosity evolution, the error "halving time" will exceed 5 years after 4-5 years.
- Therefore **it is reasonable to plan an LHC luminosity upgrade based on new low-β IR magnets after ~ 7 years.**

Courtesy Jim Strait

Importance of reducing the "turn around time"

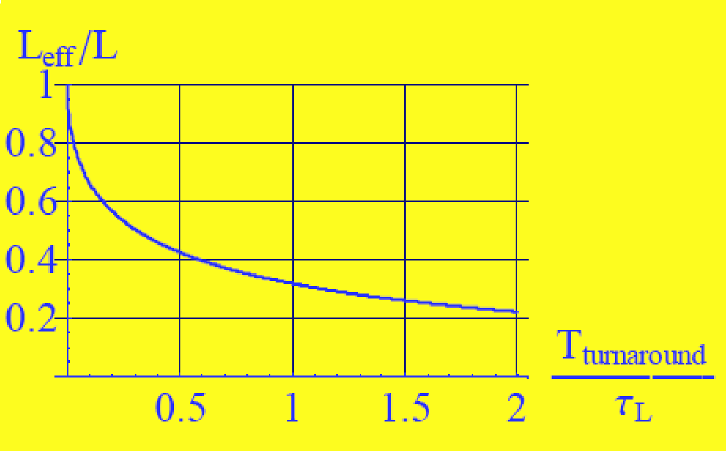
- Machine parameters and initial luminosity L_0, determine the luminosity life-time τ_L
- For a given $T_{turnaround}/\tau_L$ there is an optimum T_{run} maximizing $\int L dt$
- It is always worthwhile to reduce $T_{turnaround}$, and even more so when L_0 is increased because τ_L is decreased

$$T_{\rm run}\ (\text{optimum}) \Rightarrow \begin{cases} 1+\dfrac{T_{\rm run}+T_{\rm turnaround}}{\tau_{\rm L}} = e^{\frac{T_{\rm run}}{\tau_{\rm L}}} \\ Average(L) = L_0 \times \dfrac{\tau_L}{T_{\rm run}+T_{\rm turnaround}+\tau_{\rm L}} \end{cases}$$



Examples with τ_{gas} = 85 h and τ^x_{IBS}= 106 h (nom) ⇒ 40 h (high-L)

L_0 [cm^{-2}s^{-1}]	τ_L [h]	$T_{turnaround}$ [h]	T_{run} [h]	$\int_{200\ days} L\ dt$ [fb^{-1}]	gain
10^{34}	15	10	14.6	66	x1.0
10^{34}	15	5	10.8	85	x1.3
10^{35}	6.1	10	8.5	434	x6.6
10^{35}	6.1	5	6.5	608	x9.2



LHC performance and parameters

Parameter [units]	Nominal	Ultimate	Short bunch	Long bunch
No. of bunches n_b	2808	2808	5616	936
$p^+ \times$ bunch N_b [10^{11}]	1.15	1.7	1.7	6.0
Bunch spacing Δt_{sep} [ns]	25	25	12.5	75
Beam current [A]	0.58	0.86	1.72	1.0
E_{beam} [MJ]	366	541	1085	631
Beta at IP β^* [m]	0.55	0.50	0.25	0.25
Xing angle θ_c [μrad]	285	315	445	430
Bunch length [cm]	7.55	7.55	3.78	14.4
Piwinski ratio $\theta_c \sigma_s/(2\sigma^*)$	0.64	0.75	0.75	2.8
L lifetime τ_L [h]	15	10	6.5	4.5
L_{peak} [$10^{34}cm^{-2}s^{-1}$]	1.0	2.3	9.2	8.9
$T_{turnaround}$ [h]	10	10	5	5
Events per Xing	19.2	44.2	88	510
$\int_{\text{one year}} L\,dt$ [fb^{-1}]	66.2	131	560	410

ε_n = 3.75 mm in all the options

27 June 2006 - EPAC 06 W.Scandale, LHC luminosity and energy upgrades