# Implementation of GigE Vision Standard and Applications in MicroTCA

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Hamburg, 06.12.2018

MicroTCA TECHNOLOGY LAB

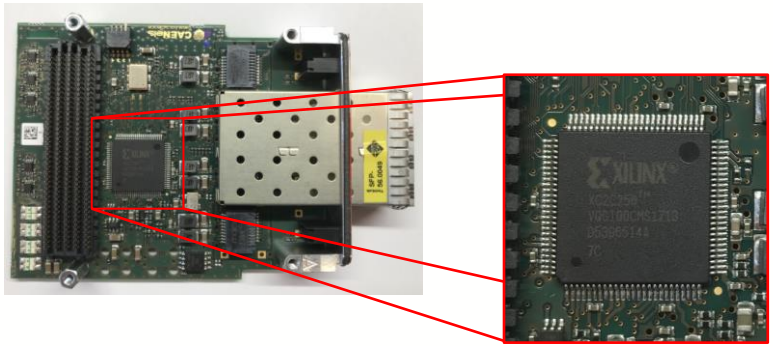
DESY.

# AGENDA

1. GigE Vision Camera Support – Why?
2. FPGA IP-Core Advantages
3. System Realization
4. GigE Vision Implementation
5. Application Concepts

# Why GigE Vision Camera Support?

- Integrate into existing control system
- Outsource image processing to FPGA
- Algorithms can run in parallel
- Flexibility is same as in software

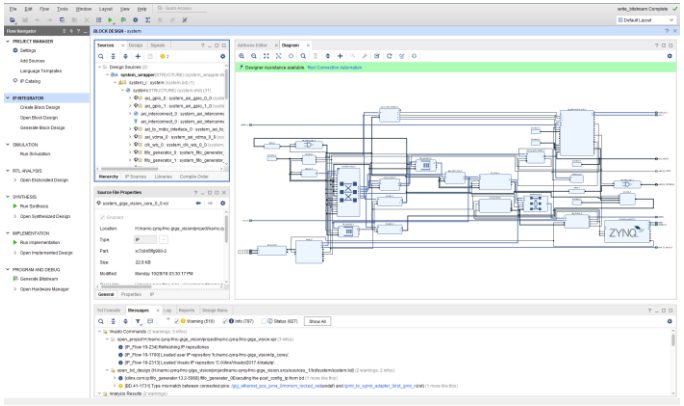




- Simple cabling (up to 100 m, PoE)
- Faster transfer rate than Firewire
- ROI definition is possible
- Device precision time protocol (IEEE1588)

# FPGA IP- Core Advantages

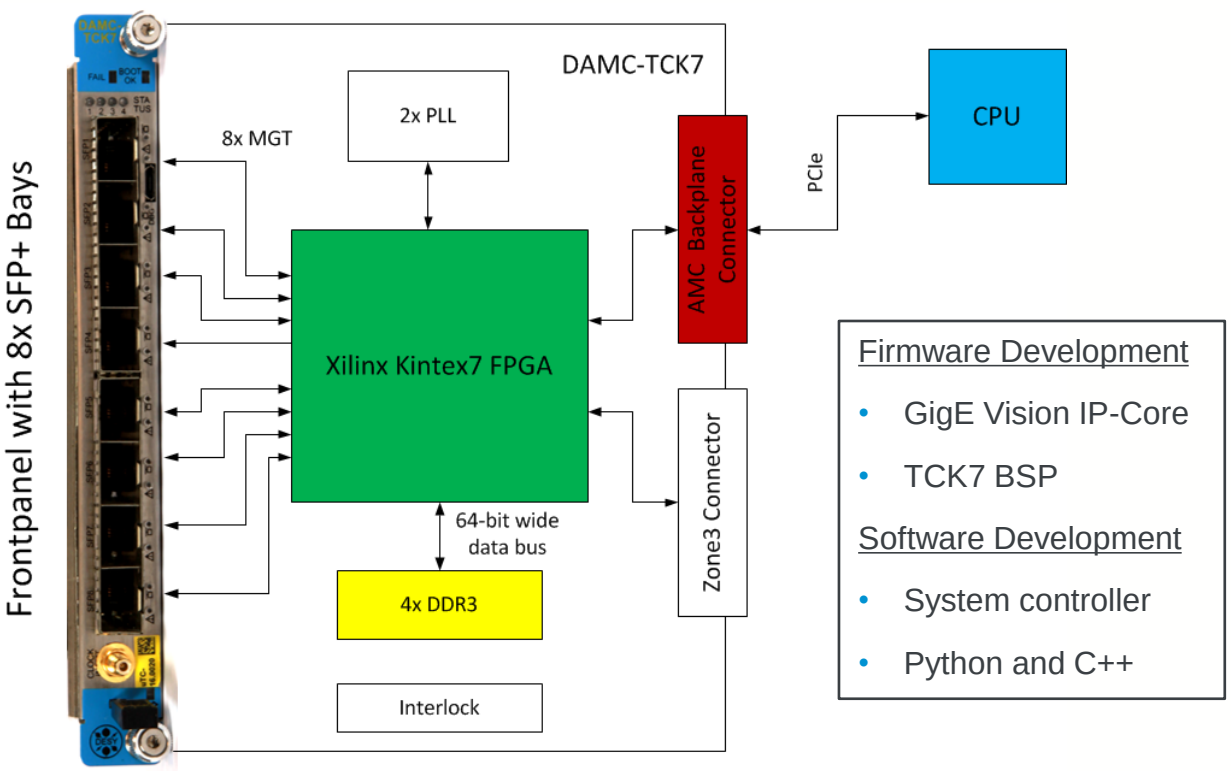
Target product:

- Firmware that is modular, scalable and widely usable
- IP-Core for Vivado Design Suite integration
- AXI4 / AXI-Stream compliant



- Basically MTCA independent
- Xilinx 7Series, Ultrascale, Ultrascale+, SoC and MPSoC compliant
- Licensing as official GigE Vision product by AIA is ongoing

# System Realization

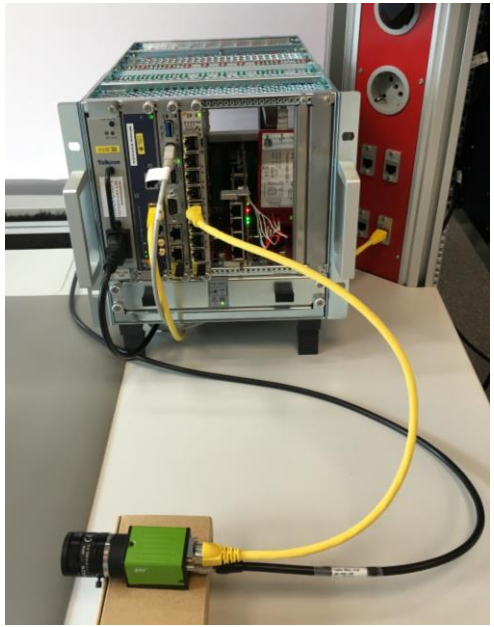



Firmware Development

- GigE Vision IP-Core
- TCK7 BSP

Software Development

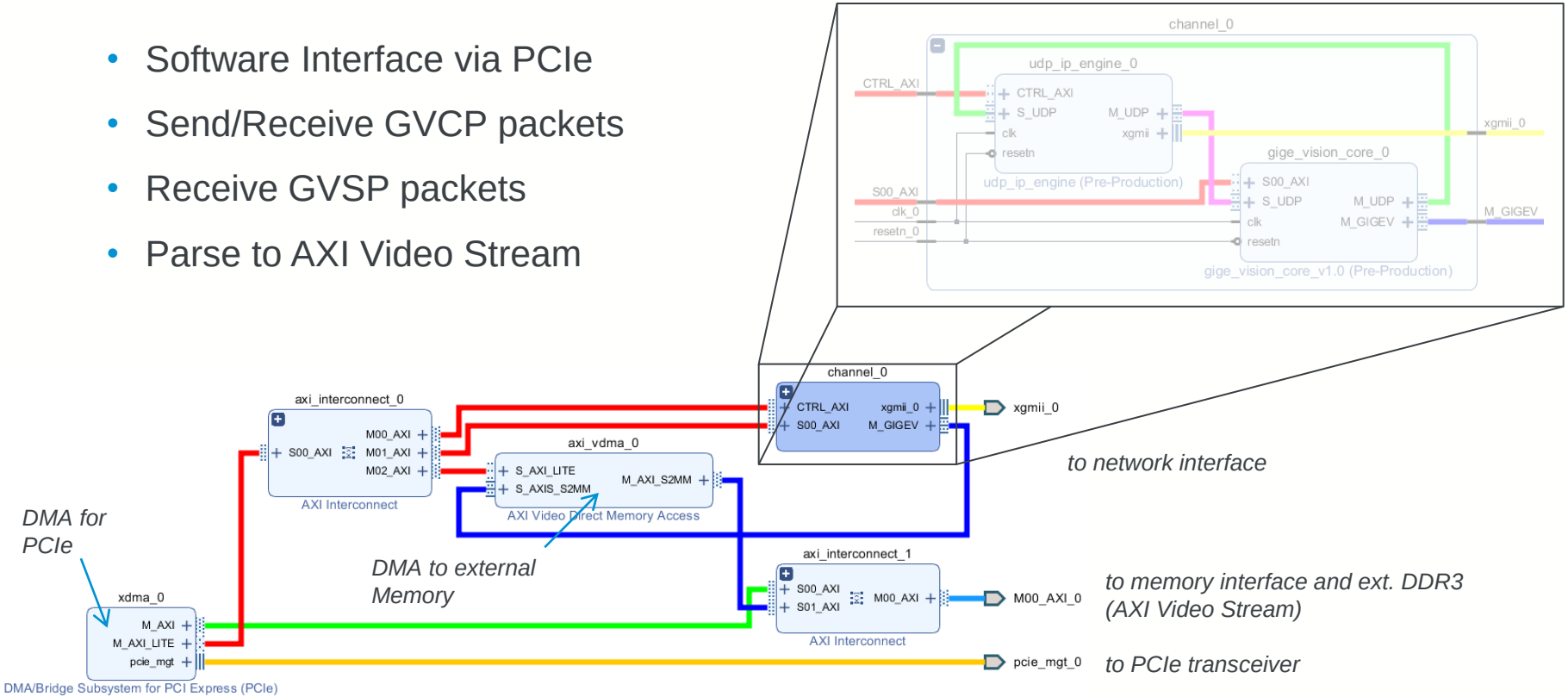
- System controller
- Python and C++



https://github.com/MicroTCA-Tech-Lab

# GigE Vision Firmware

- Software Interface via PCIe
- Send/Receive GVCP packets
- Receive GVSP packets
- Parse to AXI Video Stream



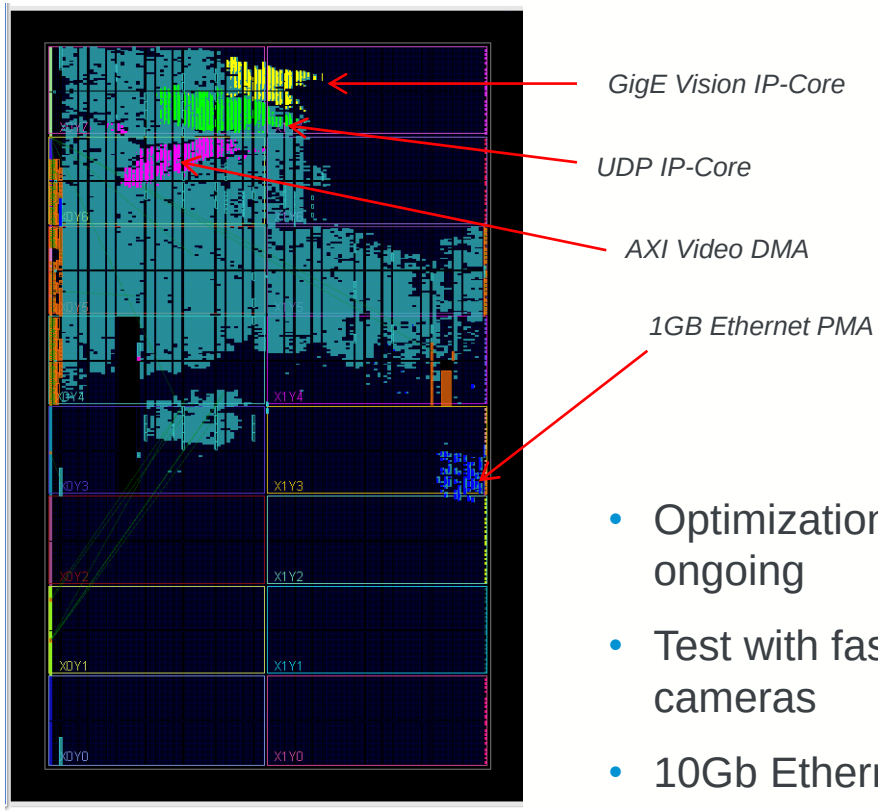
# GigE Vision Firmware

## Resource utilization GigE Vision IP-Core

| Primitive Type | Count |
|---|---|
| FLOP_LATCH | 1114 |
| LUT | 1543 |
| CARRY | 184 |
| BMEM | 10 |

## Performance GigE Vision Implementation

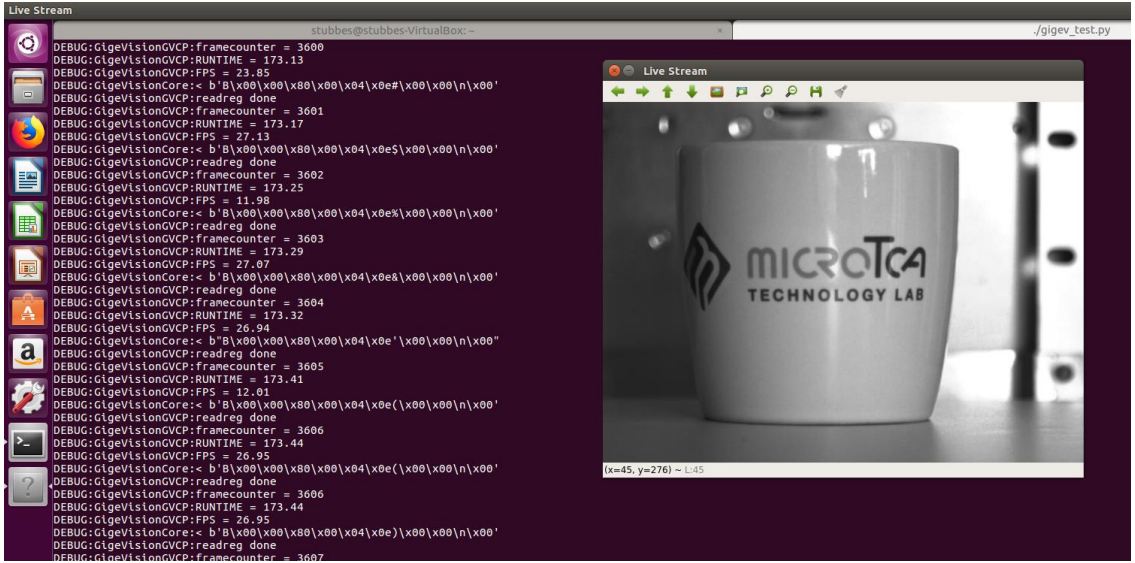
| Resolution | Frame Size | Framerate FPGA |
|---|---|---|
| 1920 x 1080 px | 16.59 Mbit | 50 fps |
| 1936 x 1216 px | 18.83 Mbit | 48 fps |



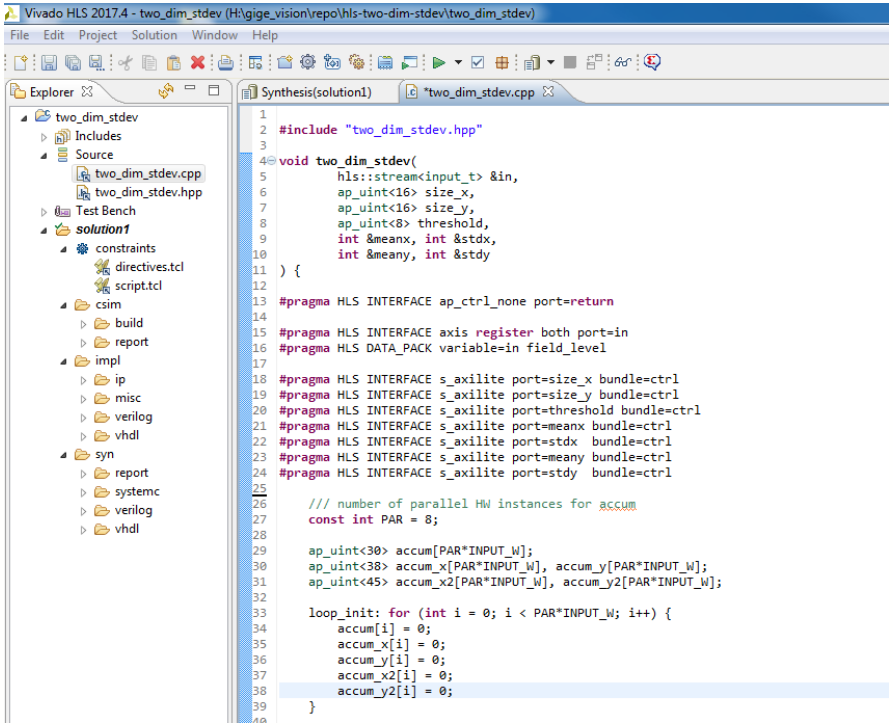

- Optimization is ongoing
- Test with faster cameras
- 10Gb Ethernet

# GigE Vision Software

- Modular controller concept
- PCIe driver provided by Xilinx with DMA IP-Core
- Usable with of OpenCV image processing library
- Support for Python and C/C++

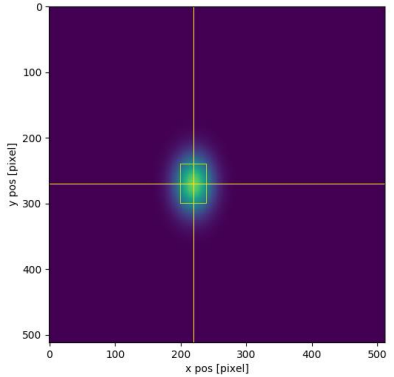


# Application Concepts



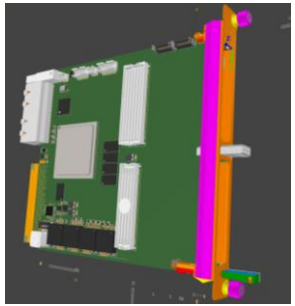

Synthesis

RTL export




- Application code is written in C++
- Low latency
  (dimension dependent)
- Convenient debugging and analyzation tools

# Application Concepts



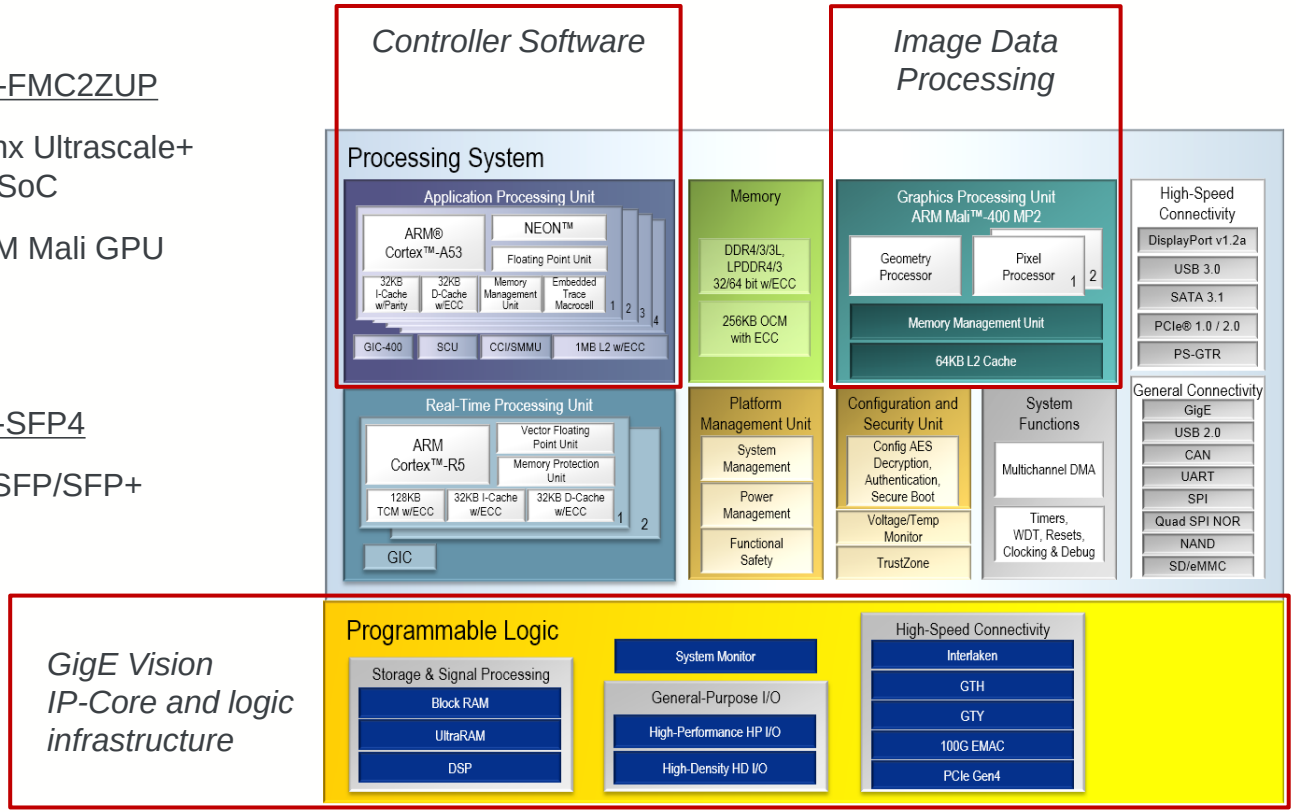
DAMC-FMC2ZUP

- Xilinx Ultrascale+ MPSoC
- ARM Mali GPU

DFMC-SFP4

- 4x SFP/SFP+

- Hardware and software on single chip
- Standalone solution

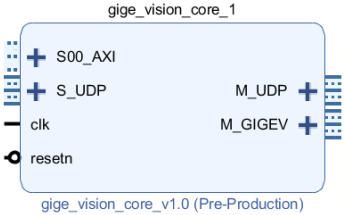


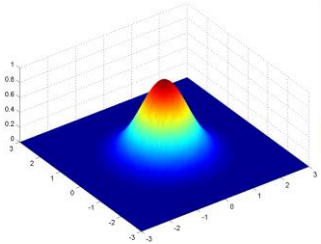

*from xilinx.com*

# Conclusion and Outlook

Products:

- GigE Vision IP-Core and infrastructure for DAMC-TCK7 (support for 8 cameras with single board)
- Standalone FPGA firmware solutions (UDP IP-Core, HLS processing application)



Ongoing projects:

- Image processing for PETRA-III Beamlines
- Porting for NAMC-ZYNQ-FMC with N.A.T.
- Firmware and software optimization