Implementation of GigE Vision Standard and Applications in MicroTCA

Sven Stubbe with support from Jan Marjanovic and Aaron Gornott Hamburg, 06.12.2018





AGENDA

- 1. GigE Vision Camera Support Why?
- 2. FPGA IP-Core Advantages
- 3. System Realization
- 4. GigE Vision Implementation
- 5. Application Concepts



Why GigE Vision Camera Support?

Sven Stubbe, 06.12.2018

p. 3

- Integrate into existing control system
- Outsource image processing to FPGA
- Algorithms can run in parallel
- Flexibility is same as in software





- Simple cabling (up to 100 m, PoE)
- Faster transfer rate than Firewire
- ROI definition is possible
- Device precision time protocol (IEEE1588)



Sven Stubbe, 06.12.2018

p. 4

Target product:

- Firmware that is modular, scalable and widely usable
- IP-Core for Vivado Design Suite integration
- AXI4 / AXI-Stream compliant





- Basically MTCA independent
- Xilinx 7Series, Ultrascale, Ultrascale+, SoC and MPSoC compliant
- Licensing as official GigE Vision product by AIA is ongoing



р. 5

DESY.





HELMHOLTZ

TECHNOLOG

ESEARCH FOR GRAND CHALLENGES

https://github.com/MicroTCA-Tech-Lab

p. 6



GigE Vision Firmware

Resource utilization GigE Vision IP-Core

Primitive Type	Count
FLOP_LATCH	1114
LUT	1543
CARRY	184
BMEM	10

Performance GigE Vision Implementation

Resolution	Frame Size	Framerate FPGA
1920 x 1080 px	16.59 Mbit	50 fps
1936 x 1216 px	18.83 Mbit	48 fps





- Modular controller concept
- PCIe driver provided by Xilinx with DMA IP-Core
- Usable with of OpenCV image processing library
- Support for Python and C/C++





p. 9

DESY.

🏊 Vivado HLS 2017.4 - two_dim_stdev (H:\gige_vision\repo\hls-two-dim-stdev\two_dim_stdev)
File Edit Project Solution Windo	w Help
) E; 🖆 🏟 🐚 🐐 🌐 🏳 🕨 🔻 🗹 🖶 👘 🕶 🔳 🚏 60 🍳
🔁 Explorer 🛛 🛛 🤣 🖓 🗖 🗖	Synthesis(solution1)
Explorer X Explorer X Explorer X Extractional states Includes Extractional states Ex	<pre> Synthesis(solution1)</pre>
	36 accum_y[1] = 0; 37 accum_x2[i] = 0; 28 accum_x2[i] = 0;
	39 }
11	10





RCH FOR GRAND CHALLENGES

- Application code is written in C++
- Low latency (dimension dependent)
- Convenient debugging and analyzation tools

Application Concepts

Sven Stubbe, 06.12.2018



DAMC-FMC2ZUP

- Xilinx Ultrascale+
 MPSoC
- ARM Mali GPU



DFMC-SFP4	

• 4x SFP/SFP+

Controller Software		lmage Proce	e Data essing	
Processing System				
Application Processing Unit ARM® Cortex™-A53 Floating Point Unit	Memory DDR4/3/3L, LPDDR4/3	Graphics Pro ARM Mali ^T Geometry Processor	Pixel	High-Speed Connectivity DisplayPort v1.2a USB 3.0
32KS 32KB Memory Embedded Hoadre D.Cache Management Tacca 1 2 3 4 GIC-400 SCU CCI/SMMU 1MB L2 wECC	32/64 bit w/ECC 256KB OCM with ECC	Memory Man 64KB L2	agement Unit	SATA 3.1 PCIe® 1.0 / 2.0 PS-GTR
Real-Time Processing Unit ARM Vector Floating Point Unit Cortex TM -R5 Memory Protection Unit 128KB 32KB I-Cache TCM wECC 32KB I-Cache WECC 1	Platform Management Unit System Management Power Management Functional Safety	Configuration and Security Unit Config AES Decryption, Authentication, Secure Boot Voltage/Temp Monitor TrustZone	System Functions Multichannel DMA Timers, WDT, Resets, Clocking & Debug	General Connectivity GigE USB 2.0 CAN UART SPI Quad SPI NOR NAND SD/eMMC
Programmable Logic Storage & Signal Processing	System Monitor	High-Speed Interla	Connectivity Iken	

- Hardware and software on single chip
- Standalone solution

GigE Vision IP-Core and logic infrastructure

nable Logic			High-Speed Connectivity	
J		System Monitor		Interlaken
Signal Processing		Constal Purpose I/O		GTH
ock RAM		General-Purpose I/O		GTY
ltraRAM		High-Performance HP I/O High-Density HD I/O		100G EMAC
DSP				PCle Gen4

TECHNOLOGY

HEI MHOL

RESEARCH FOR GRAND CHALLENGES

from xilinx.com

DESY.

Products:

- GigE Vision IP-Core and infrastructure for DAMC-TCK7 (support for 8 cameras with single board)
- Standalone FPGA firmware solutions (UDP IP-Core, HLS processing application)

Ongoing projects:

- Image processing for PETRA-III Beamlines
- Porting for NAMC-ZYNQ-FMC with N.A.T.
- Firmware and software optimization



