IRES Technologies

Multipurpose MTCA.4 data processing board based on FPGA device with built-in data converters

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Agenda

1. Fast Data Converters - Recent Problems
2. Xilinx RFSoC
3. AMC-RFSoC Specification
4. Data Processing
5. The General Cost Consideration
6. Project Status

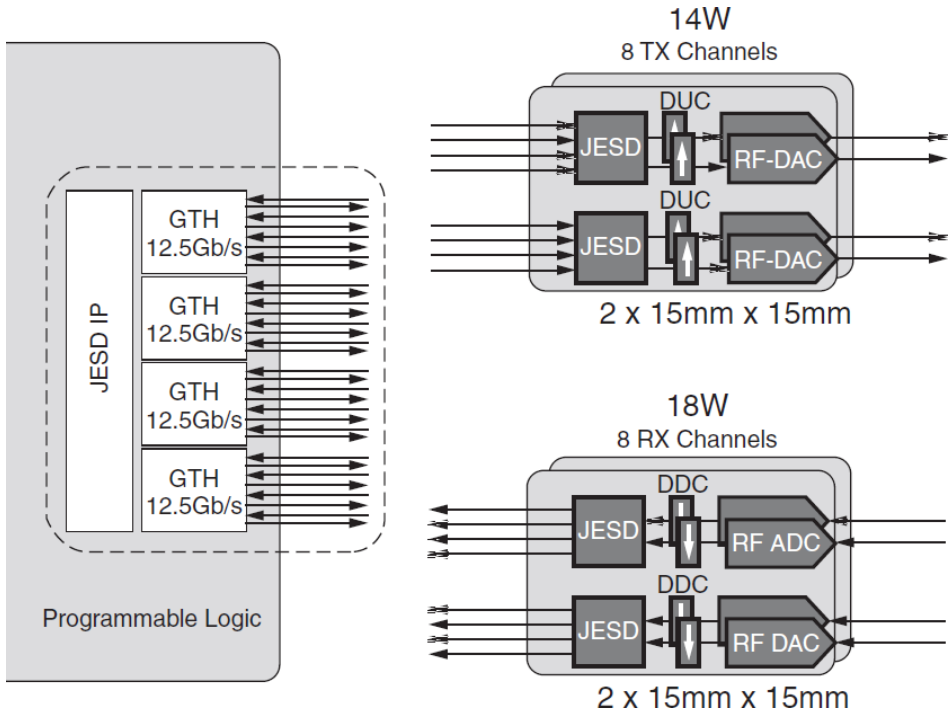
Fast Data Converters & Recent Problems

- FPGAs are more and more powerful, have more resources and can process a lot data in parallel
- The problem appears, when there is need to connect many fast data converters to one FPGA

Until now following interfaces are typically available for fast data converters:

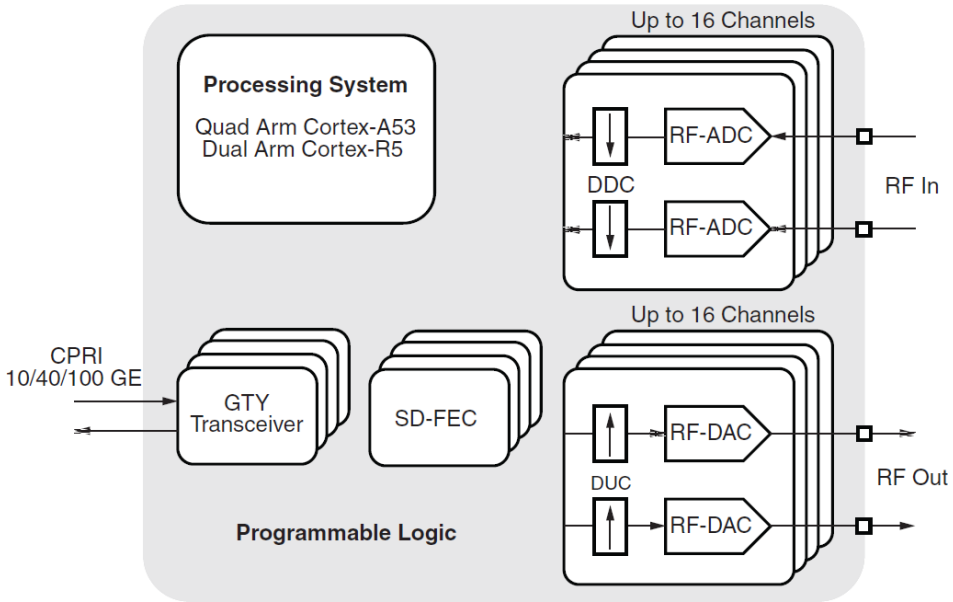
- **Parallel interface** - Legacy interface, DDR and LVDS helps, but does not solve the issue
- **JESD204** - complex, require clocking and synchronization, expensive

- Designed to make possible connecting multiple data converters to FPGA
- It uses GT Transceivers
- But it still needs:
  - PCB space
  - Power
  - Advanced clocking
- Extensive FPGA code is needed to support the communication (align data, etc.) - that is why Xilinx JESD204 core is cost **$6,790**...

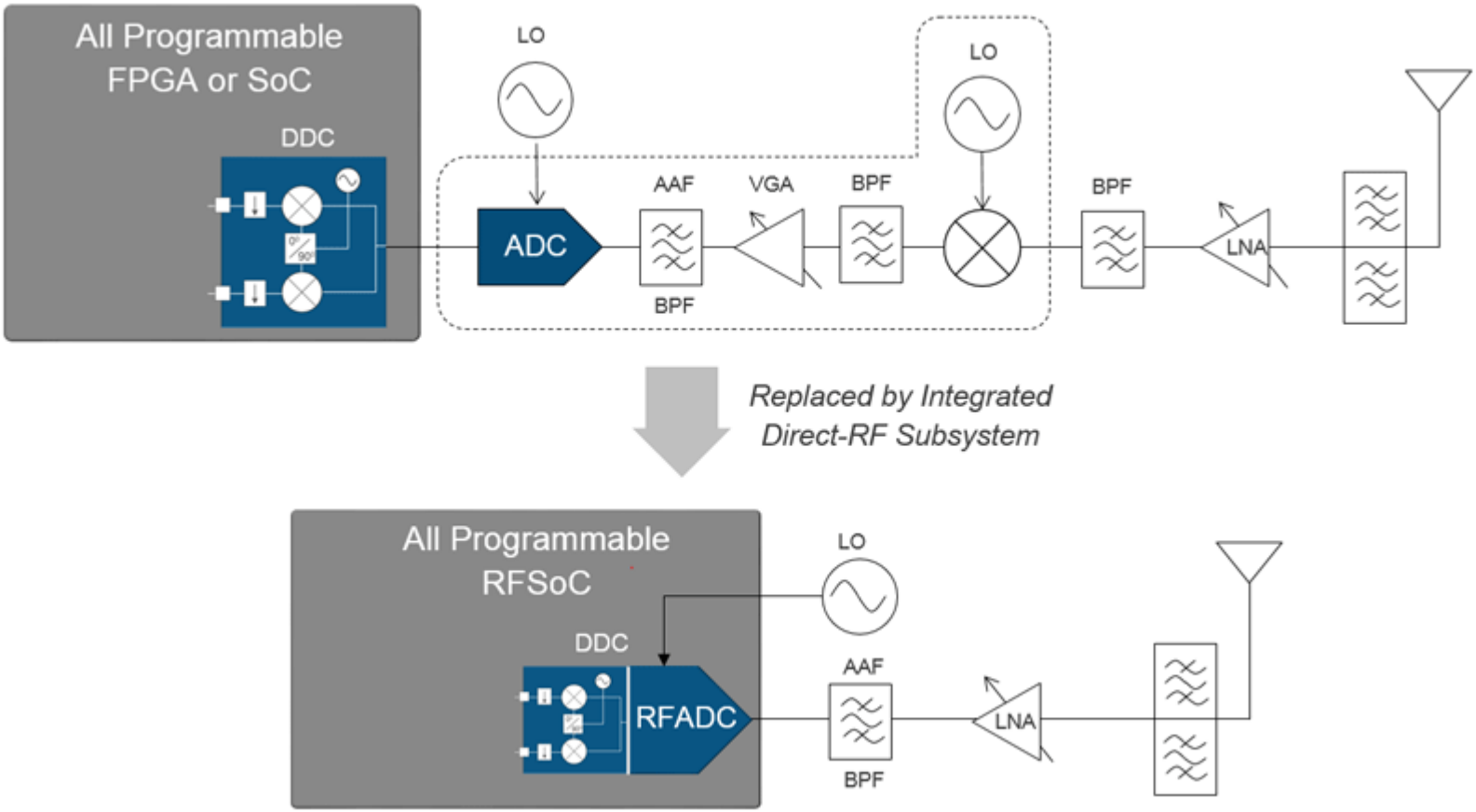


Xilinx has introduced RFSoC device family, FPGAs with integrated RF-class data converters:

- 8x 12-bit 4.096 GSPS RF-ADC
- 16x 12-bit 2.058 GSPS RF-ADC
- 8x or 16x 14-bit, 6.554GSPS RF-DAC



RF Sampling & Digital Up and Down Converters

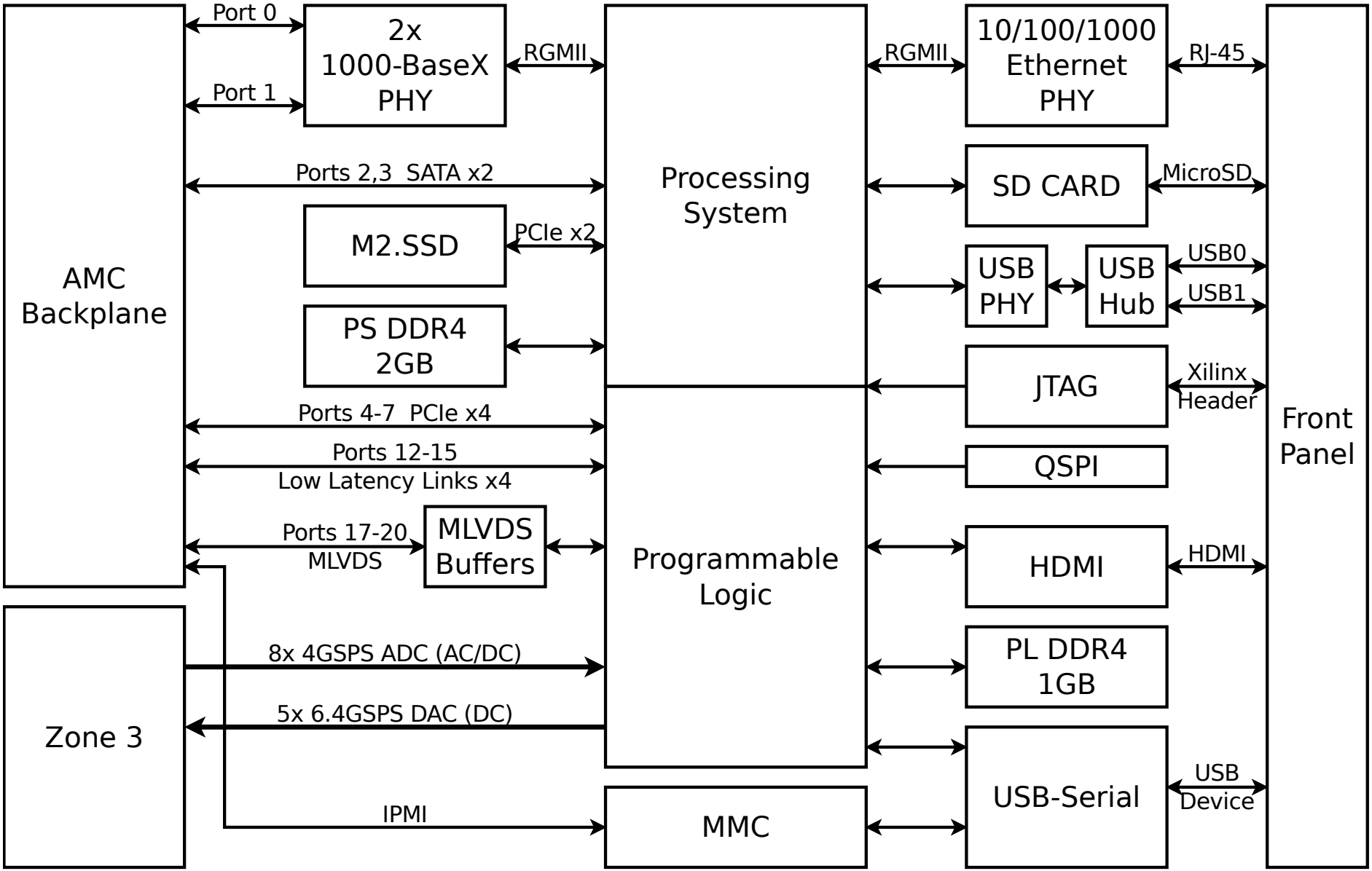


RFSoC devices significantly simplifies RF design

Xilinx RFSoC - Other resources

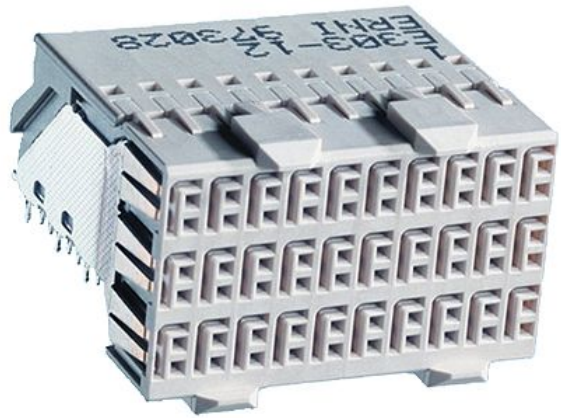
Processing System	Application Processing Unit	Quad-core Arm Cortex-A53	
	Real-Time Processing Unit	Dual-core Arm Cortex-R5	
	Supported Memories	DDR4; DDR3; DDR3L; LPDDR4; LPDDR3	
	General Connectivity	UART; CAN; USB 2.0; I2C; SPI; 32b GPIO	
	High-Speed Connectivity	4xPS-GTR; PCIe® Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII	
Programmable Logic	System Logic Cells	678k	930k
	CLB Flip-Flops	620k	850k
	CLB LUTs	310k	425k
	Distributed RAM (Mb)	9,6	13.0
	Block RAM (Mb)	27,8	38.0
	UltraRAM (Mb)	13,5	22,5
	DSP Slices	**3145**	**4272**
	GTY Transceivers	8	16
	PCIe Gen3 x16	1	2
	100G Ethernet w/ RS-FEC	1	2

AMC-RFSoC Block Diagram



AMC-RFSoC Specification

- Analog interface: ZONE.3, DESY A.X:
  - 8 x 4 GSPS ADC (AC or DC Coupled; solder resistors options)
  - 5 x 6.4 GSPS DC coupled DAC
- Bottleneck: ERNI Zone 3 connector
- **It is possible in future to redesign the PCB for user defined AMC-RTM connectors, coaxial for example.**



AMC-RFSoC Specification

AMC Interface:

- Ports 0,1: 2x GB Ethernet 1000-BaseX (PS RGMII)
- Ports 2,3: 2x SATA (PS GTR)
- Ports 4-7: PCIe x4 (PL GTY)
- Ports 12-15: Low Latency Links (PL GTY)
- Ports 17-20: MLVDS clocks & triggers

On-board Memories & Storage:

- M.2 SSD disk slot (PCIe x2, PS-GTR)
- 2 GB DDR4 (PS)
- 1 GB DDR4 (PL)
- 1x SD Card Slot
- 2x QSPI (2 Gb)

AMC-RFSoC Specification

Other interfaces:

- USB Serial (USB Device) (PL & MMC)
- USB 2.0 Host (PS)
- HDMI (PS)
- 10/100/1000 RJ-45 Ethernet on front Panel

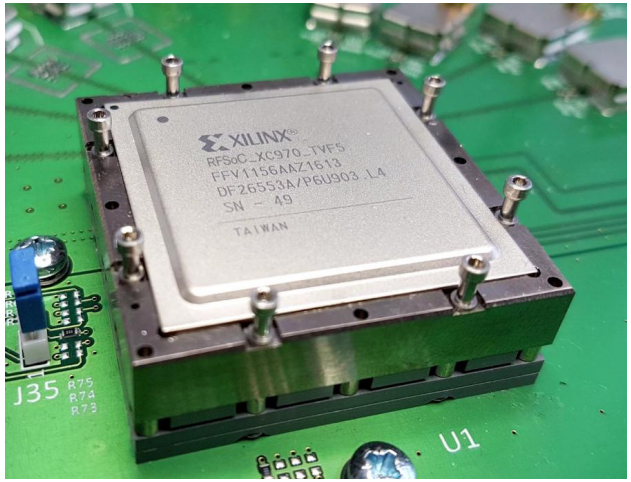
FPGA Configuration:

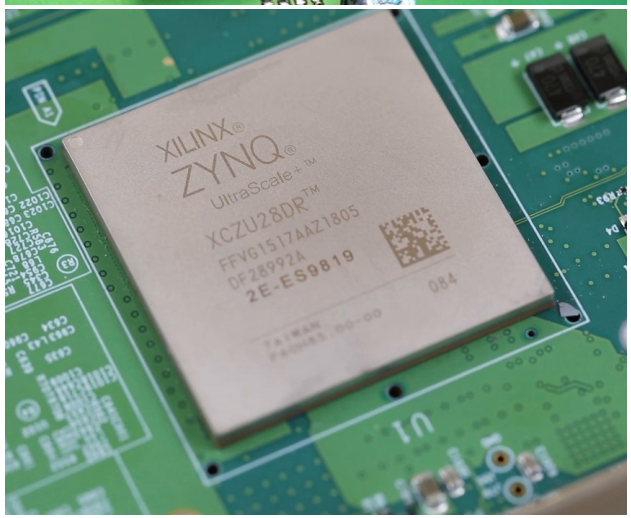
- SD Card
- QSPI Memories
- JTAG

AMC-RFSoC Specification

AMC-RFSoC will have optional BGA socket for FPGA device

- Board Can be tested or repaired without affecting RFSoC device
- Expensive RFSoC device may be reused if needed
- Ordering options:
  - AMC-RFSoC with soldered FPGA device
  - AMC-RFSoC with FPGA in the socket
  - AMC-RFSoC with with empty socket
- Following devices are compatible:
  - XCZU25DR-E1156
  - XCZU27DR-E1156
  - XCZU28DR-E1156





Data Processing

- FPGA PL will support realtime data processing (HDL programming)
- Quad ARM can handle:
  - High-level (C++, python, etc.) based data procesing implementations
  - Communication and control system tasks
- No data transfers to or from CPU!:
  - PS ARM can access FPGA resources immediately
  - PL FPGA can access ARM RAM memory directly !

The General Cost Consideration

Board will have following functionality:

- 8x 4 GSPS 12-bit Integrated ADCs - instead discrete ones
- 8x 6.4 GSPS 14-bit Integrated DAC - instead discrete ones
- Large FPGA
- Quad Core ARM, works as CPU in crate
- DDC & DUC will simplyfiy or replace RTM (like DWC or VM)
- M.2 SSD disk will provide storage instead SATA AMC

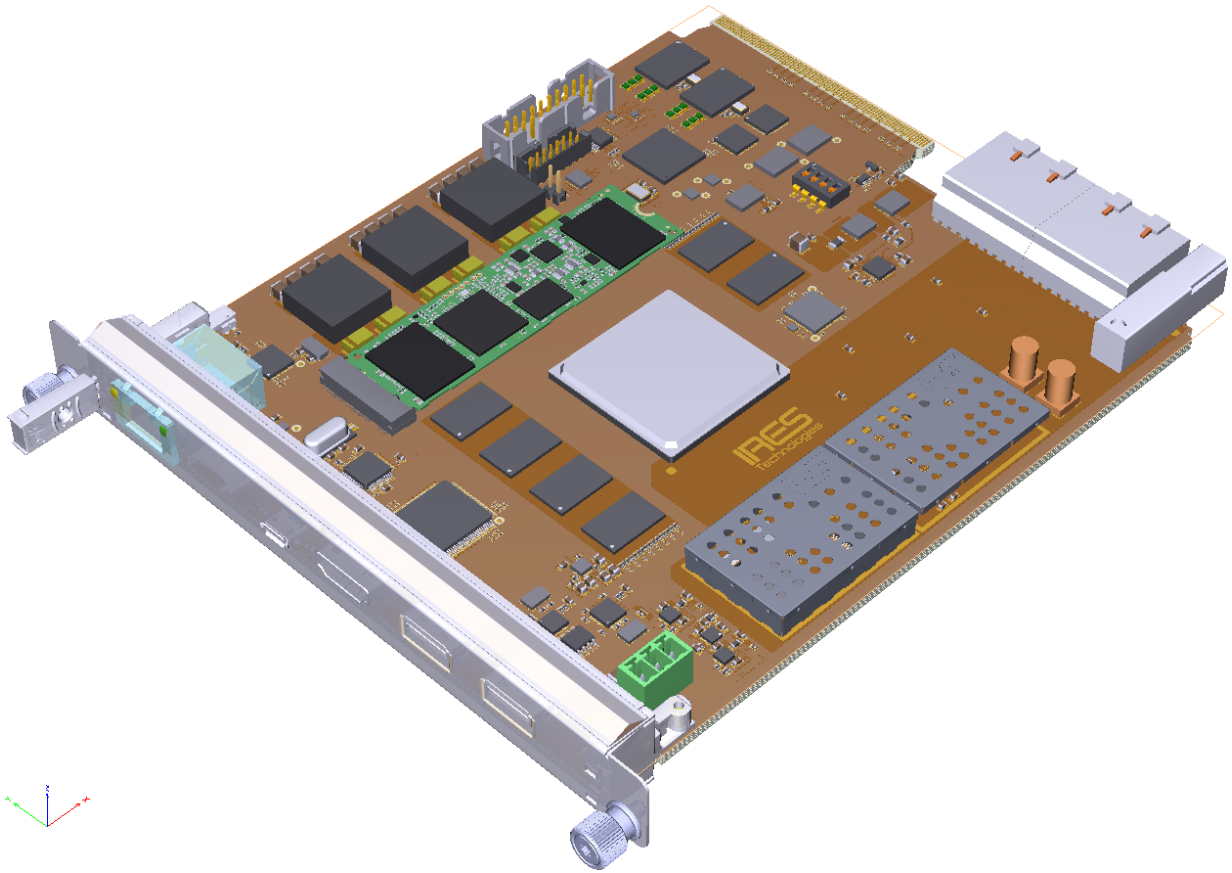
Savings:

- No overhead of interfacing FPGA & Data Converters (PCB, HDL)
- No need for JESD204 IP Core

Overall performance/cost ratio looks very promising

Actual Status

- PCB design is ready in 80-90%
- Q1/2019 production & testing is planned
- Q2/2019 First boards available for market



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Thank You for Your Attention!

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