MicroTCA Future Developments

7th MicroTCA Workshop for Industry and Research, December 2018

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Current Situation – Data Transfer Rates and Power

- Current released AMC dot-specifications define PCIe Gen2 (5 Gbit/s per diffpair) and 10G Ethernet (3.125 Gbit/s per diffpair)
- 40G on MTCA working group has nearly finished it‘s work, 40G Ethernet and PCIe Gen3 spcification to be released in 2019
- However, even if many crates in the field have not been built in accordance to the pending 40G specification, they successfully run PCIe Gen3 and 40G Ethernet applications
- Attention: Even if 40G Ethernet or PCIe Gen3 works in dedicated setups, a change of one component might lead to performance issues
- 100G Ethernet is already in use in ATCA for several years. MTCA should adapt it soon
- The 80W power limitation of MTCA is already an issue since several years
- **MTCA requires an update to allow higher data transfers and higher power per AMC**

Signal Integrity:
Basics, Simulations, Verifications

Open Standards / Bus Specifications

System specifications / **Open Standards** are defined by

- **PICMG** (PCI Industrial Computer Manufacturers Group)
- **VITA** (VMEbus International Trade Association)
- **PXI-SA** (PCI eXtensions for Instrumentation System Alliance)

These specifications define the dimensions of chassis, dimensions of the backplane, slot pitch, connectors, connector pinouts, bus types to use …

Bus parameters for data transmission are defined in **Bus-specifications**:

- **Ethernet: IEEE** (Institute of Electrical and Electronics Engineers)
  40 Gbps, 100 Gbps Ethernet
- **PCI-Express: PCI-SIG** (Peripheral Component Interconnect Special Interest Group)
  PCI, PCIexpress Gen 1/2/3/**4/5*** (2.5 / 5 / 8 / **16 / 32*** Gbps per diff pair)

* PCI-express Gen 5 expected in Q2 2019

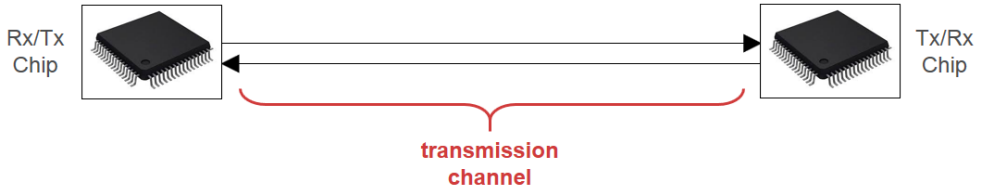
Bus Specifications / Open Standards

Bus-specifications define (besides other parameters):

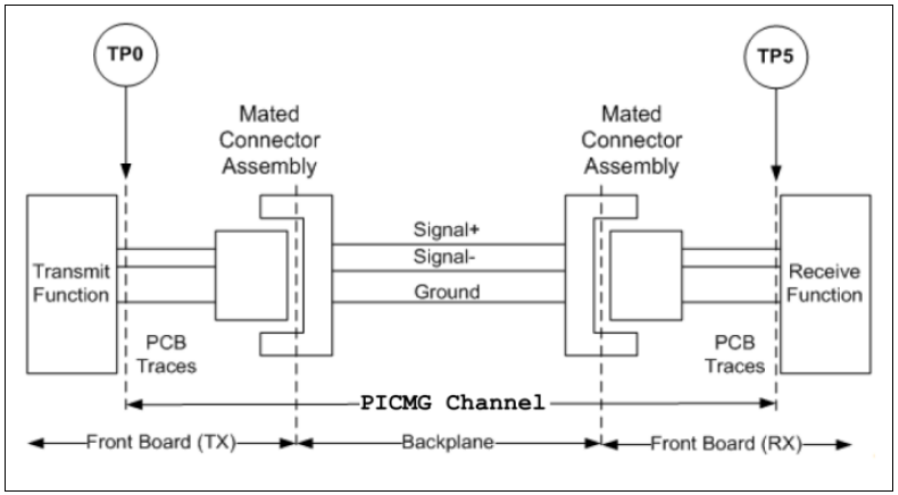
- **Transmitter chip parameters:**
  Data rates, voltage levels, output impedance, max Jitter …
- **Receiver chip parameters:**
  Data rates, voltage levels, input impedance, max Jitter …

Chip manufacturer responsibility

- **Channel parameter:**
  Impedance, Losses, x-talk …

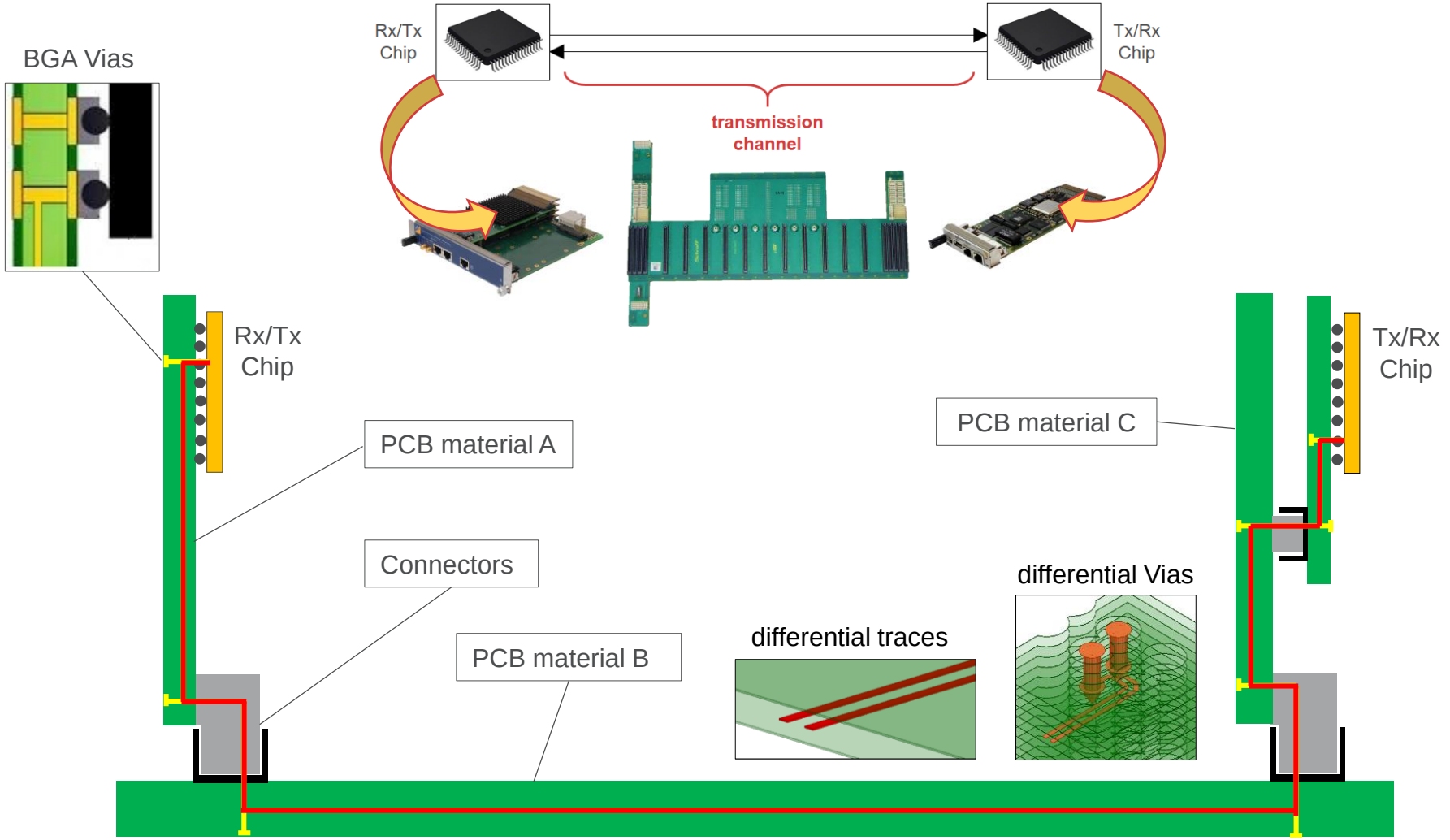


Open Standard organizations split the channel into the separate parts in their System



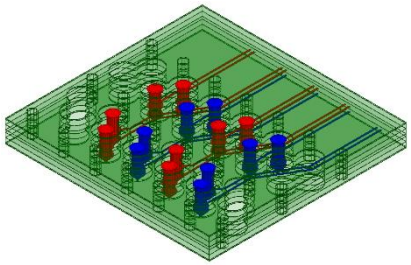
Data Transmission Channel – Create the Channel Model

Pre- and post layout simulations



Signal Integrity Simulation

Simulation tools
(Pre- and Post-layout simulation)**:**

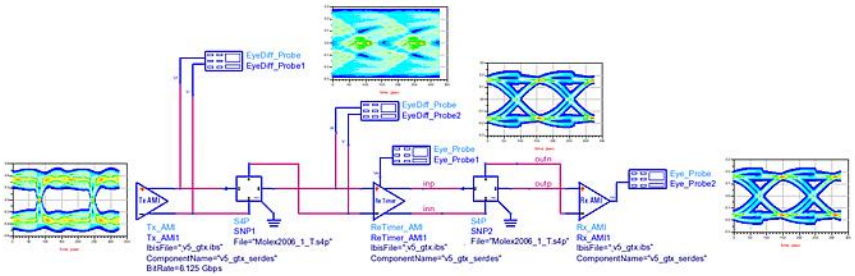


- **HFSS,** 3D electromagnetic field solver from ANSYS

ANSYS

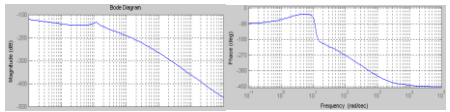
- **ADS** (Advanced Design System) from Keysight with Momentum 3D Planar EM Simulator

KEYSIGHT TECHNOLOGIES Agilent Technologies



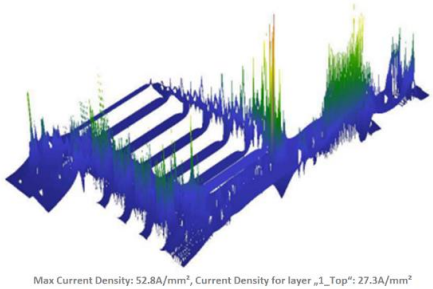
- **MATLAB**

MATLAB



- **HyperLynx PI** from MENTOR (Power integrity simulation)

Mentor Graphics



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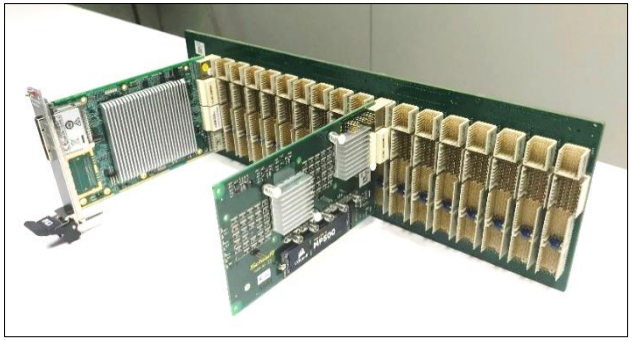
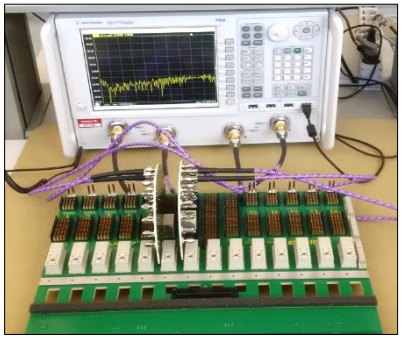
Signal Integrity - verify the simulation results

Signal integrity verification (DVT, Design Verification Test)



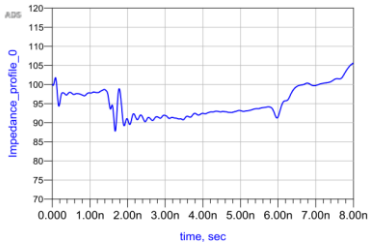
➢ Functional test:

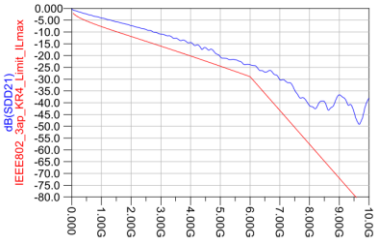
- Advantage:
  - perfect for first tests
  - fast
  - relatively low investment costs
- Disadvantage:
  - set-up with other cards could led to other results
  - safety margin unknown
  - fault tracing not possible

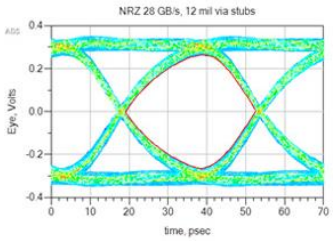


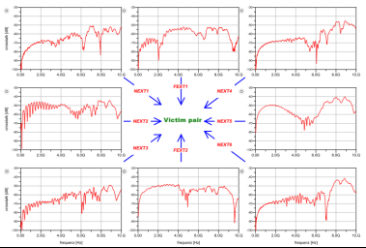
➢ Measurements:

- Advantage:
  - shows channel parameter
  - allows fault tracing
- Disadvantage:
  - high investment cost (measurement equipment)
  - test time



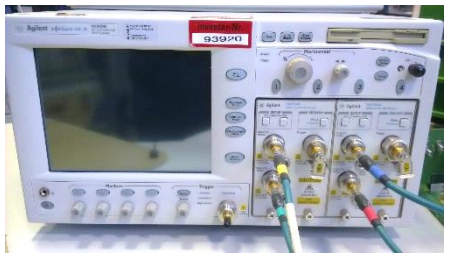




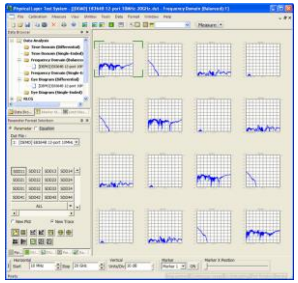


Signal Integrity Verification

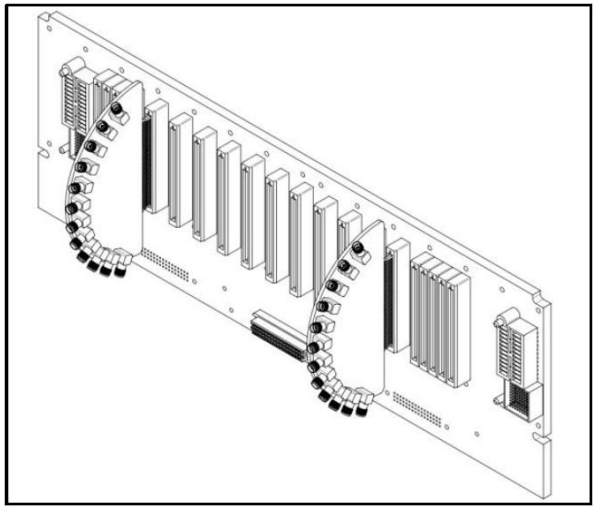
Signal integrity measurement equipment
(Time and Frequency domain measurements)



- **N5227A 67GHz Network Analyzer from Keysight**
- **TDR. 86100B mainframe + 54753A sampling modules from Keysight**
- **PLTS Software from Keysight**

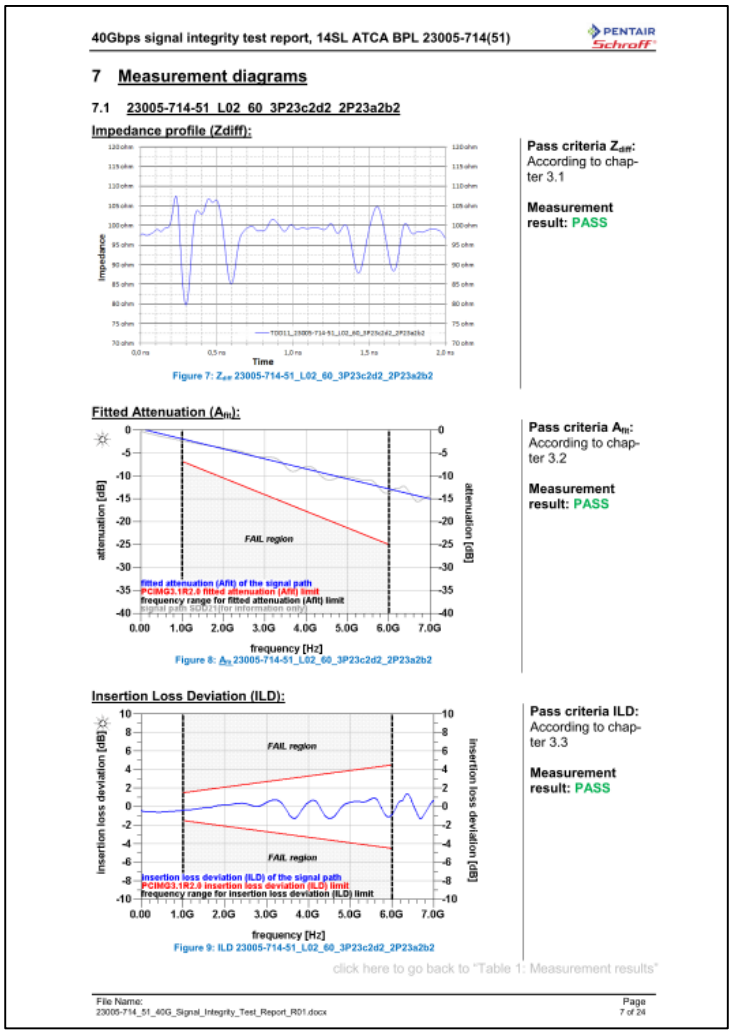


- **Measurement adapter (paddle cards) for different connector/backplane types**
  - The paddle cards simulate the worst case board parameters defined in the corresponding open standard specification
  - The measurement results will contain the backplane plus paddle card results (complete channel)



Signal Integrity Verification

Signal integrity measurement report



40Gbps signal integrity test report, 14SL ATCA BPL 23005-714(51)

PENTAIR Schroff

7 Measurement diagrams

7.1 23005-714-51_L02_60_3P23c2d2_2P23a2b2

Impedance profile (Zdiff):

Figure 7: Z_{diff} 23005-714-51_L02_60_3P23c2d2_2P23a2b2

Pass criteria Z_{diff}: According to chapter 3.1

Measurement result: PASS

Fitted Attenuation (A_{fit}):

Figure 8: A_{fit} 23005-714-51_L02_60_3P23c2d2_2P23a2b2

Pass criteria A_{fit}: According to chapter 3.2

Measurement result: PASS

Insertion Loss Deviation (ILD):

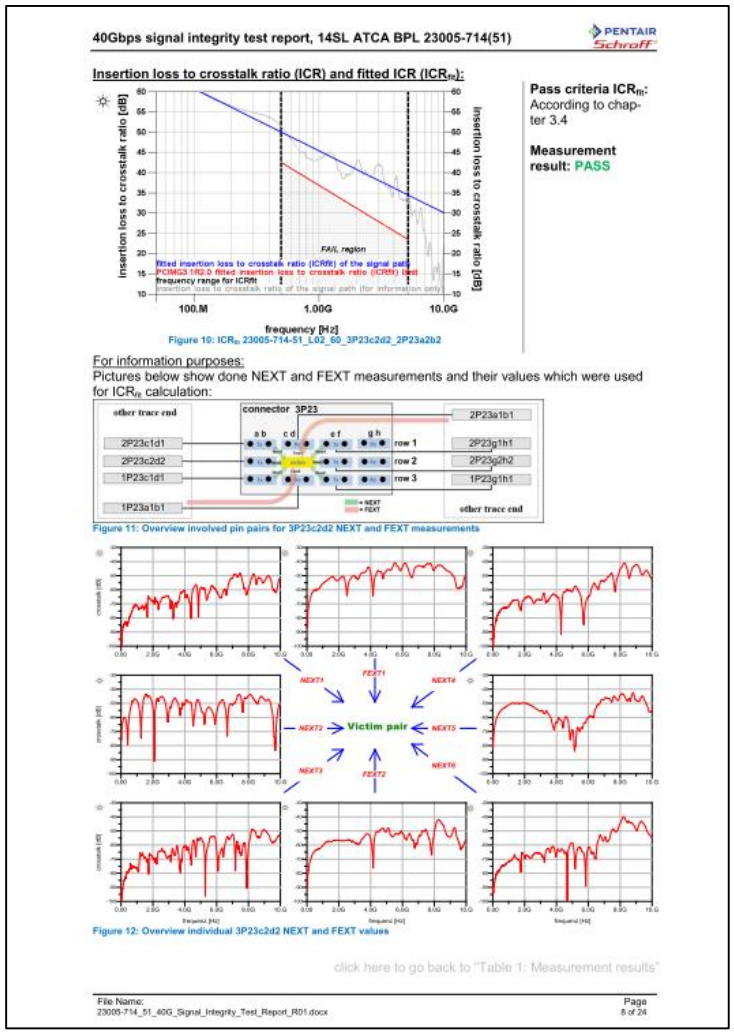
Figure 9: ILD 23005-714-51_L02_60_3P23c2d2_2P23a2b2

Pass criteria ILD: According to chapter 3.3

Measurement result: PASS

click here to go back to "Table 1: Measurement results"

File Name: 23005-714_51_40G_Signal_Integrity_Test_Report_R01.docx Page 7 of 24



40Gbps signal integrity test report, 14SL ATCA BPL 23005-714(51)

PENTAIR Schroff

Insertion loss to crosstalk ratio (ICR) and fitted ICR (ICR_{fit}):

Figure 10: ICR_{fit} 23005-714-51_L02_60_3P23c2d2_2P23a2b2

Pass criteria ICR_{fit}: According to chapter 3.4

Measurement result: PASS

For information purposes:

Pictures below show done NEXT and FEXT measurements and their values which were used for ICR_{fit} calculation:

Figure 11: Overview involved pin pairs for 3P23c2d2 NEXT and FEXT measurements

Figure 12: Overview individual 3P23c2d2 NEXT and FEXT values

click here to go back to "Table 1: Measurement results"

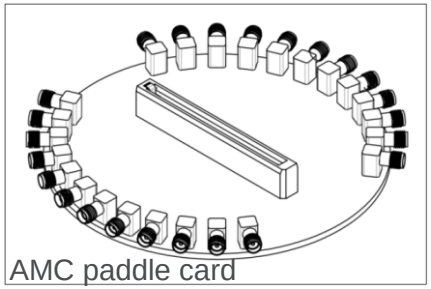
File Name: 23005-714_51_40G_Signal_Integrity_Test_Report_R01.docx Page 8 of 24

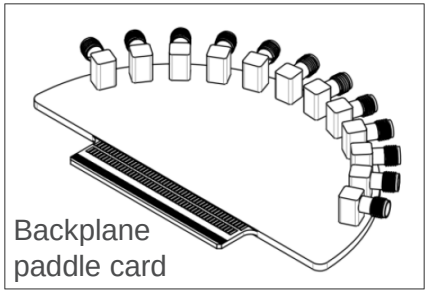
40G, 100G Ethernet and PCIe Gen4 & 5 @ MTCA

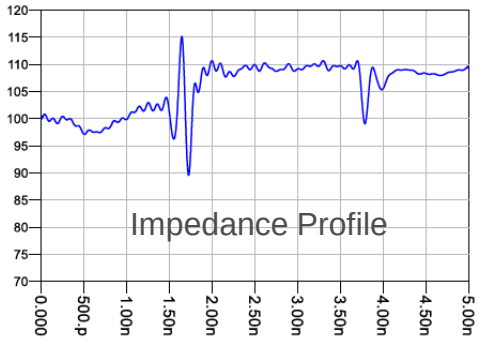
40G @ MTCA

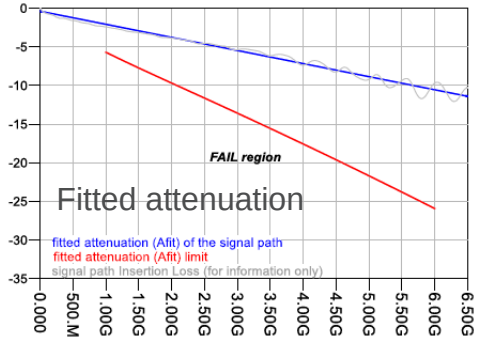
40G specification to be released soon

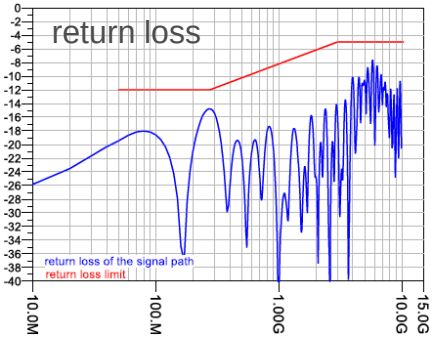
- Will support all connectors / plugs that are available today
- Defines the signal requirements for short, middle and long signal traces
- Defines the parameters for the test paddle cards
- Channel Characteristics for the backplane:
  - Fitted attenuation
  - Insertion loss deviation
  - Fitted Insertion loss to crosstalk ratio
  - …

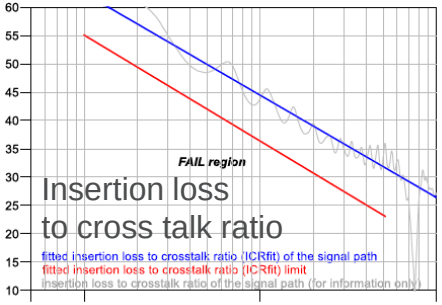


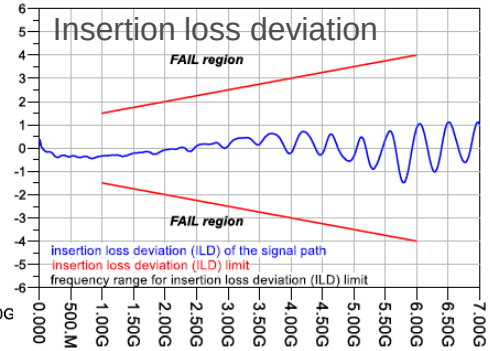


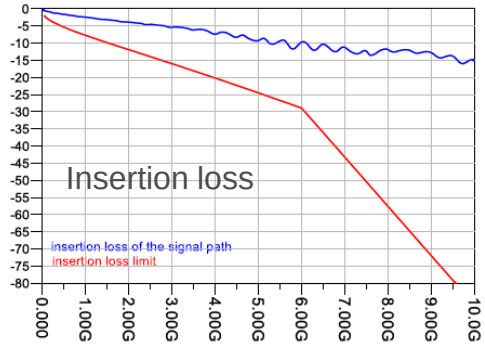






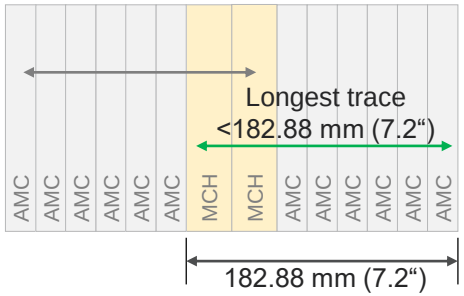




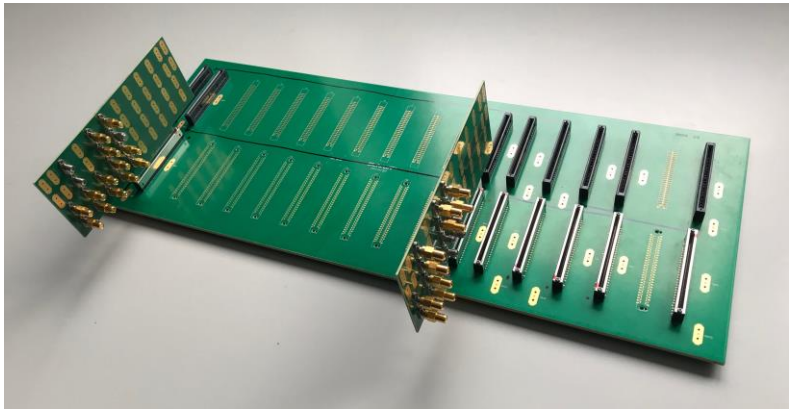


100G @ MTCA

100G: Simulations and measurements started



- **Measurements proofed that 100G Ethernet is possible with „middle loss“ PCB materials for backplane traces up to 6“ (152.4 mm)**
  - 2 AMC‘s with PCB tongue connector (no plug)
- **Simulations show that with „low loss“ PCB materials 100G Ethernet is possible for 12 Slot mTCA backplanes**
  - Measurements for verification need to be performed
  - Might work even with MCH tongue 3 & 4 plug and AMC without plug (not every MCH plug type is suitable)
  - IEEE provides MatLab script for COM (Channel Operation Margin) calculation -> doesn‘t look that spectacular anymore
- **A new 100G MTCA with downward compatibility to existing AMC modules will be possible**



Differential impedance:

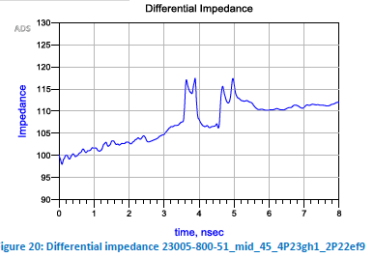


Figure 20: Differential impedance 23005-800-51_mid_45_4P23gh1_2P22ef9

Pass criteria for differential impedance according to chapter 3.1

Result: PASS

Backplane signal path differential skew:

Routed trace length (backplane PCB):
Net 2_Tx3_4+: 44,51087mm
Net 2_Tx3_4-: 44,50995mm

Length difference: about 0, 001mm
Resulting skew: <<1ps

Pass criteria for differential skew according to chapter 3.2

Result: PASS

COM (Channel Operation Margin):

IEEE COM values [dB]:
Case 1: 7,16dB
Case 2: 6,64dB

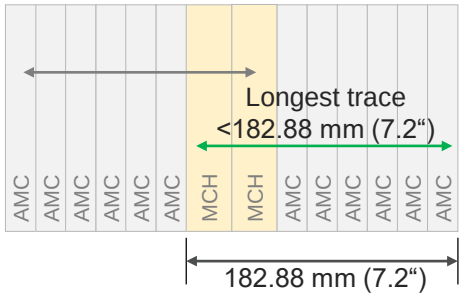
Pass criteria for COM according to chapter 3.3

Result: PASS

PCIe Gen4 & Gen5 @ MTCA

PCIe Gen5

- Will run with 32 Gbaud per differential pair
- To be released Q2 / 2019
- PCIe Gen4 might be skipped due to next years specification release of PCIe Gen5
- Right now, no AMC connector parameters available for this speed
- Might require more changes to the signal path within the MTCA Crate



Possible implementations for PCIe Gen5 in MTCA:

- Separate MCH into a Carrier Manager and a Switch
- Carrier Manager would contain MCH tongue 1 & 2, hardware management functionality and common options part (GbE and CLK‘s)
- Carrier Manager could be a Single or Double Mid-size module or reside somewhere else in the chassis like in ATCA
- The switch would get a new high speed connector with high pin density to allow Singe or Double Mid-size Switches

Even PCIe Gen5 in MTCA should be possible to realize

Increased power @ MTCA

Current Power Limitations @ MTCA

- **Currently the MTCA and AMC specification limit the power / AMC to 80W**
- **Limiting factor 1 -> AMC Power Pins**
  - 8 Pins, each 1.5 A @ 10 .. 14V = **120 W** (@10 V)
- **Ideas for increasing power:**

1. Increase voltage to 13V and limit the voltage tolerance to 12 .. 14 V

   Power per AMC = 144 W (@ 12 V)

2. Define „high power AMC pinout“
   - Some current GND pins are not required (~ 4)
   - 2 pins are „reserved, not used“
   - 6 additional power pins = **108 W** (@ 12 V) / **90 W** (@ 10 V)

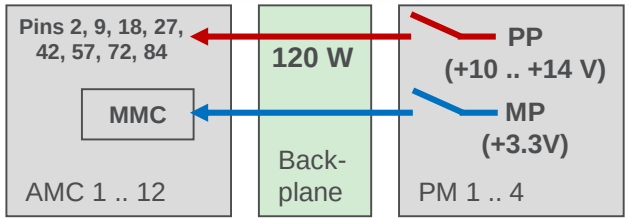
   Power per AMC = 210 W (@ 10 V)

- **ATTENTION: If new power pins are defined there must be a differentiation between legacy and high power AMC‘s**

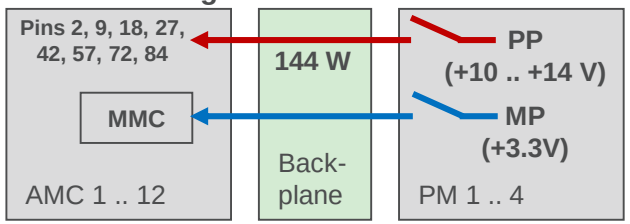
Table 7-5 Current-carrying capability

	Current rating (With Derating of IEC 60512)	Connector Capability	Temperature rise
General purpose conductor	0.40 A/Pin	0.50 A/Pin	30°C Maximum
Ground conductor	0.30 A/Pin	0.375 A/Pin	30°C Maximum
Power conductor	1.52 A/Pin	1.9 A//Pin	30°C Maximum
Differential pairs conductor	0.1 A/Pin	0.125 A//Pin	30°C Maximum

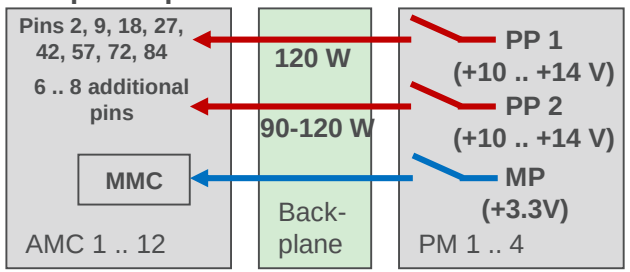
Current version



Increase voltage to 12 .. 14 V



Add power pins and second channel



Current Power Limitations @ MTCA

- **Currently the MTCA and AMC specification limit the power / AMC to 80W**

- **Limiting factor 2 -> Power Module Connector**
  - Power Module connector (Spec): 9.3 A per channel = **93 W**
  - Power Module connector (data sheet): 12 A per channel = **120 W**

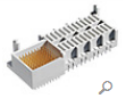
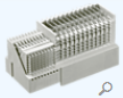
- **Ideas for increasing power:**
  - Increase voltage to 13V and limit the voltage tolerance to 12 .. 14 V

    -> Power per Channel (Spec) = **111.6 W** (@ 12 V) -> not sufficient

    -> Power per Channel (data sheet) = **144 W** (@ 12 V) -> OK

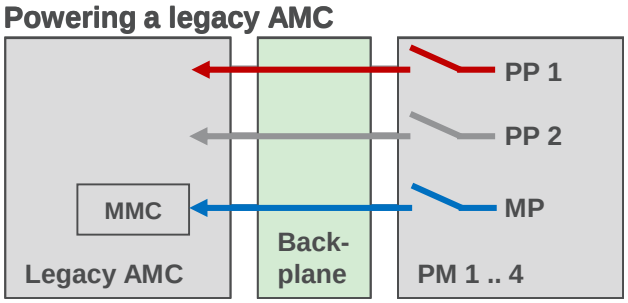
  - Define „high power AMC pinout“
    - 2 Power channels per AMC required
    - Power Module with 2 power connectors, either side by side with Single / Double **Full-Full** size PM or one on top of the other with Double Full-size PM
    - „High Power“ AMC need entry in the FRU data, that PM can activate second channel on MCH request

	Current rating (With Derating of IEC 60512)	Connector Capability	Temperature Rise
Signal and Signal GND Conductor	0.5 A/pin	0.625 A/pin	30°C Maximum
Power branch and GND Conductor	9.3 A/pin	11.625 A/pin	30°C Maximum

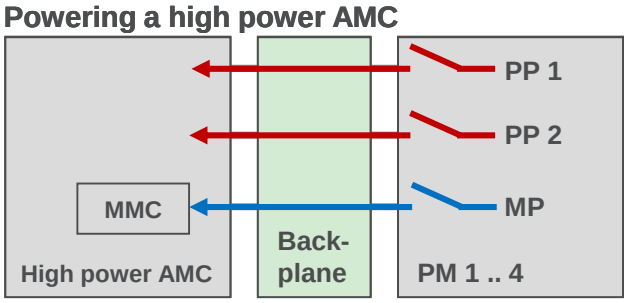
Type		No. of contacts Signal/Power	High Speed or Power	Mating connectors
	MTCA Power Backplane	72 / 24	Power 12 A	MTCA Power Module Output
	MTCA Power Module Output	72 / 24	Power 12 A	MTCA Power Backplane

Activating Legacy and High Power AMC

- When inserted, Management power get switched on
- MMC doesn‘t report „high power“ requirements
- Only Payload Power 1 gets switched on



- When inserted, Management power get switched on
- MMC reports „high power“ requirements
- Payload Power 1 and 2 get switched on



MTCA Future Developments - Conclusion

Conclusion

- To achieve compatibility with the next generation of data transfer rates and power requirements, MTCA needs an update
- It‘s possible to implement a new revision of MTCA that is 100G and PCIe Gen5 capable and supports significant higher power for each AMC
- Such new revision will limit the number of connectors / plugs that can be used and will require changes in the Power Module and Power Management
- The MCH switch section might require another „high speed“ connector, maybe switch and management part as separate modules
- All details have not been reviewed completely yet. There might be some unforeseen traps
- To implement that, there MUST be a new specification by PICMG to guarantee interoperability of AMC‘s, MCH‘s, PM‘s and Crates
- Other requirements for a new revision of MTCA?

Thank you