ESS: Status and Developments

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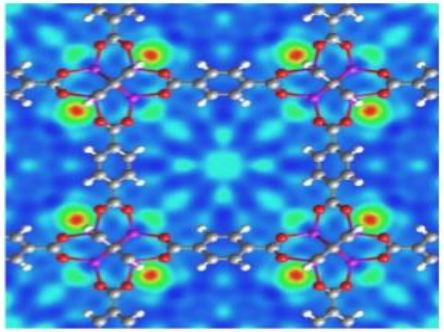
Outline

- Brief recap of the European Spallation Source
- Application areas for MTCA.4 in ESS
- Portfolio of MTCA.4 equipment
- Developments and points of possible interest
- Initiatives for future
- Conclusions

The European Spallation Source

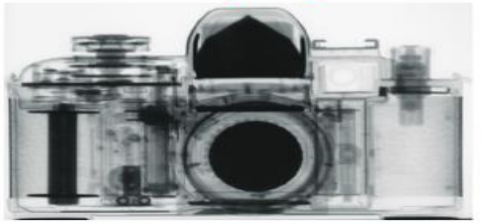
- ESS is a neutron spallation source for neutron scattering measurements.
- Neutron scattering can reveal the molecular and magnetic structure and behavior of materials:
  - Structural biology and biotechnology, magnetism and superconductivity, chemical and engineering materials, nanotechnology, complex fluids, etc.
- Neutrons are complementary to X-Rays (synchrotrons, X-FEL)
- High beam power will open up new possibilities for neutron scattering experiments
  - Traditionally, low flux and “slow” experiments



Neutron scattering of hydrogen in a metal organic framework

Neutron radiograph of a flower corsage

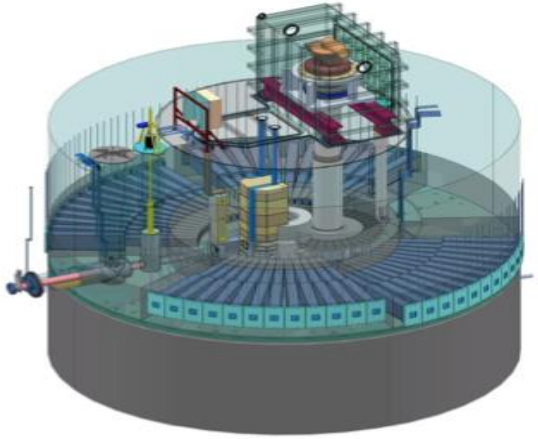
X-Ray Image

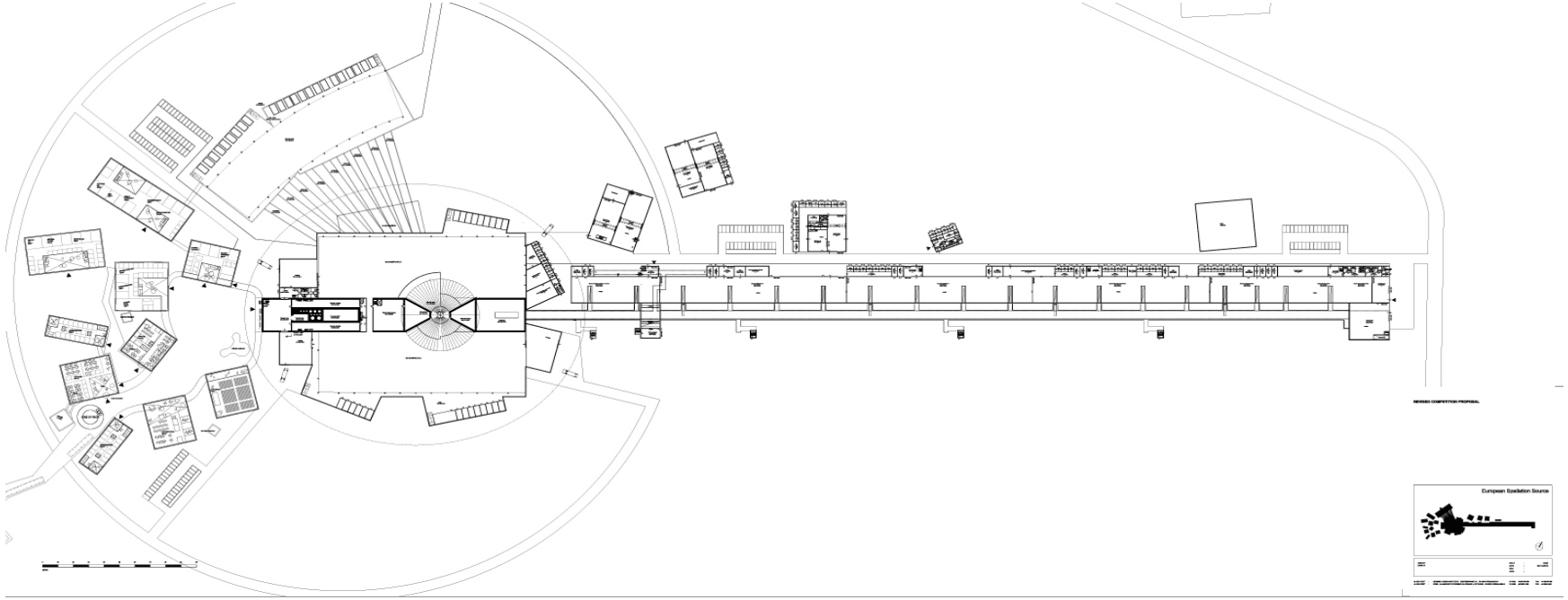


Neutron radiograph

The European Spallation Source

- The European Spallation Source (ESS) consists of :
  - a pulsed accelerator that shoots protons into…
  - a rotating metal (tungsten) target to produce neutrons
  - (up to) 22 neutron instruments for various experiments





The European Spallation Source

- The European Spallation Source (ESS) will house the most powerful proton linac ever built.
  - The average beam power will be 5 MW.
  - The peak beam power will be 125 MW
- At 5 MegaWatts, one beam pulse
  - has the same energy as a 7.2kg shot traveling at 1100 km/hour (Mach 0.93)
  - Has the same energy as a 1000 kg car traveling at 96 km/hour
  - Happens 14 x per second
- This puts some severe conditions on
  - Machine Protection
  - Reliability of instrumentation
    - Used as input for MPS
  - Usability of the control system
    - Balance between protection, availability and ease of use

Construction site overview

ESS Construction Site, OCT-2018

- Accelerator tunnel, equipment galleries ready.
  - Installation work ongoing
- First cryoplants operating
- Target building taking shape
- Instrument halls, neutron lines under construction
- Temporary offices for the whole ESS staff now on site
- Construction of final offices has started (this week.)
- Status updates, nice photos on https://europeanspallationsource.se/

ESS is starting to form…

The King of Sweden and the President of Italy in the inauguration ceremony, 15. November 2018

The first few meters of the ESS Accelerator – Ion Source and Low Energy Beam Transport - have been delivered and gone through initial commissioning.
Commissioning is still continuing
More accelerator components will come in and be installed next year (Normal Conducting LINAC, including RFQ, MEBT and Drift Tube Linac.)

Still some work ahead until neutron production, but nevertheless we are an accelerator laboratory now!

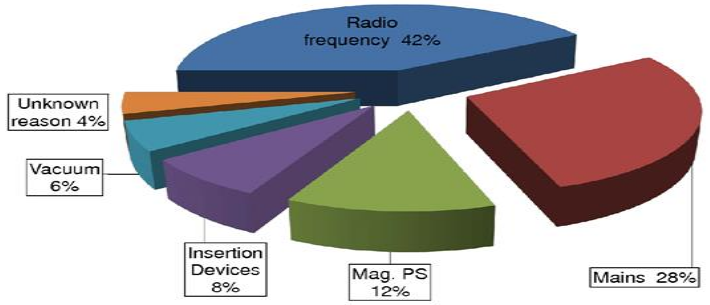
The European Spallation Source – one more aspect

EUROPEAN SPALLATION SOURCE

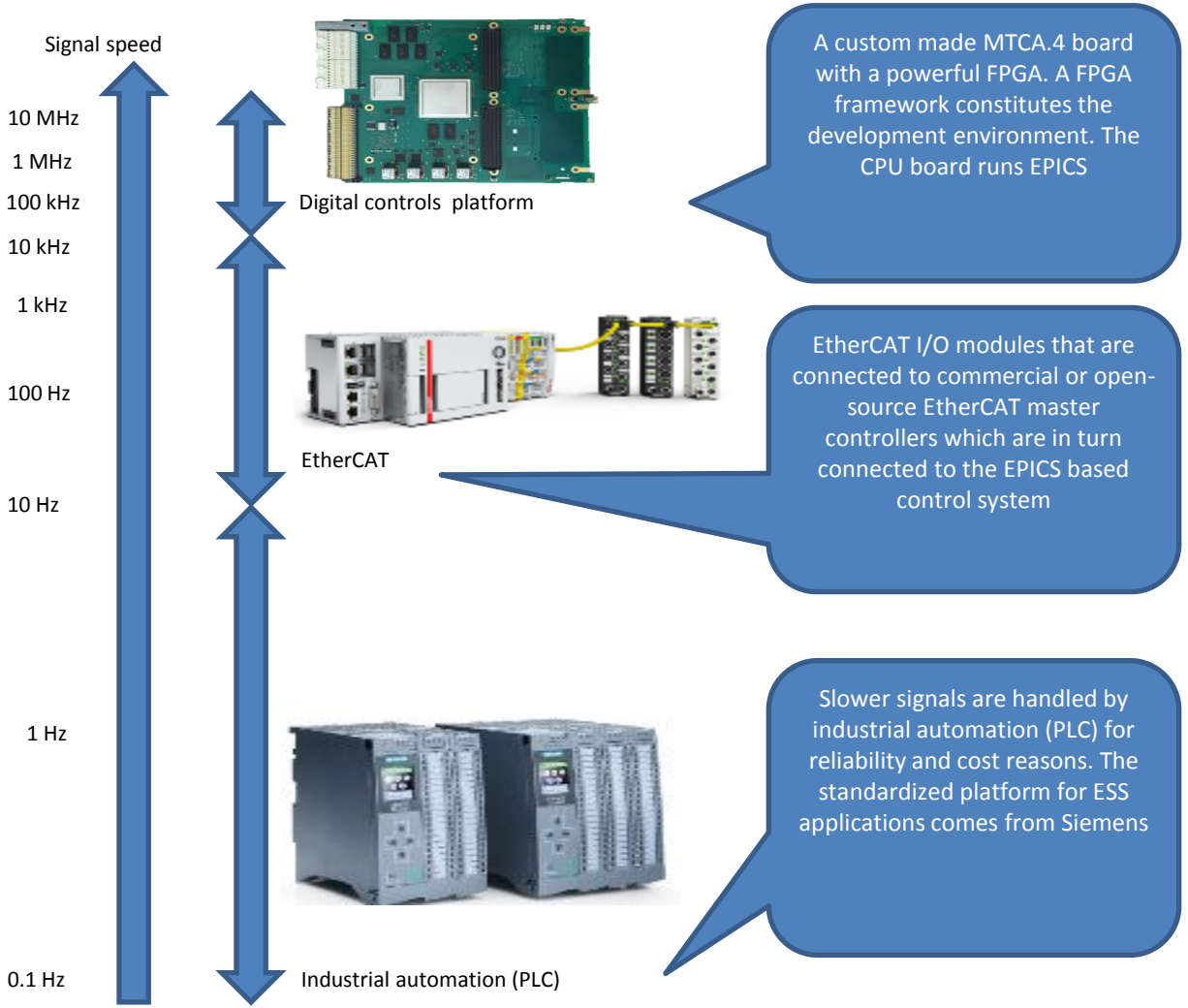
- The European Spallation Source is a joint project of 15 member countries
  - Many components will be delivered in-kind
  - Components either are control, or instrumentation systems, or require controls to operate
  - This creates a wide outreach of the ESS project in member countries
  - Challenging but crucial to our success
- We have to drive standards also with the in-kind partners
  - Support for getting started
  - Repeated discussions and meetings during development
  - Standards will be familiarized in our partner labs
- If we are successful, this will ripple further
  - Good experience with our standards encourages partners to continue using them
  - Could also be the other way…
- We hope to help in growing the MTCA.4 ecosystem
  - On top of the work that DESY has pioneered.

The ESS Integrated Control System

- Shall enable operation of ESS from a single control room
- Provides controls for the Accelerator, Target, Site infrastructure, Neutron Instruments (excl. data handling)
- High reliability: 95% for the whole ESS, 99.99 for ICS (exact numbers for ICS to be defined, high in any case)
  - 24 hours, 7 days a week operation
- Long lifetime (planned lifetime 40 years)
  - Upgrades will happen in between, though
  - High maintainability
- Supports (up to) 14 Hz operation of ESS
  - May not sound that fast but long pulses make this challenging!
- Is based on EPICS (7)



Three layer strategy for control systems at ESS



- **ICS has adopted a three layer strategy for implementing the control system based on signal processing needs**
  - MTCA.4 for applications with data acquisition exceeding few kHz
  - These applications require a FPGA and custom, high-speed signal processing in system.
  - For slower signals, EtherCAT will be used as a real-time fieldbus with good price/performance ratio
  - Synchronization and event information are key for applications where a full custom platform solution would be too costly
  - Low speed signals are handled with commercially available PLC systems
  - This is a cost-effective solution that addresses ESS reliability and maintainability requirements
  - The PLCs are connected to EPICS for further integration into the control system

MTCA.4 Application areas

- RF Systems: LLRF, fast RF protection (RF-LPS)
- Machine Protection System: fast beam interlock system (FBIS)
- Timing System (MRF)
- Beam Instrumentation

- All of these use heavily FPGAs
  - Pay attention to flexible and standardized interfaces
- Much ICS effort goes into
  - Supporting FPGA development
  - Low-level drivers and operating system support
  - Long-term maintainability

Applications #1: RF Systems

- 150+ RF systems using MTCA
  - LLRF
    - One of the earliest MTCA-developments at ESS
    - Collaboration between ESS and many European labs and countries
  - RF-Local Protection (RF-LPS)
    - Also a collaboration, but MTCA part developed for/by ESS
    - Fast protection and monitoring implemented on a MTCA FMC carrier
  - LLRF and RF-LPS integrated into same MTCA crates
    - Equipped with timing and other infrastructure

RF-Local Protection System

- Combination of a MTCA AMC…
  - IFC_1410 FMC Carrier (details in later slides)
  - ADC_3117 20-channel, 5 MSPS differential 16-bit ADC
  - DIO_3118 digital I/O FMC
  - Interface to Beam Interlock System
- and a PLC, integrated in one system
  - To protect klystrons
  - High requirements on reliability
- Simple and not-that-simple functions
  - Level comparator & interlock
  - Power monitor, calculation from several inputs
  - Full buffering of analogue and digital inputs and status outputs (“first fault detection”)

MTCA Applications #2: Machine Protection System

- Beam Interlock System, fast part, aka FBIS, implemented using MTCA
  - High damage potential, stringent requirements on Machine Protection
  - Lots of diverse systems to be connected
    - Some slow ones (limit switches, temperatures, power converters)
    - Some fast and complicated
      - Beam Loss Monitors
      - Beam Current Monitors
      - (at least a part of) Beam Position Monitors
  - Fast reaction time required
    - ~10 us in low energy part, somewhat more (~20 us) in high energy part of linac
      - Low energy beam causes damage faster – Bragg peak energy deposition
- In-kind collaboration with ZHAW, Switzerland

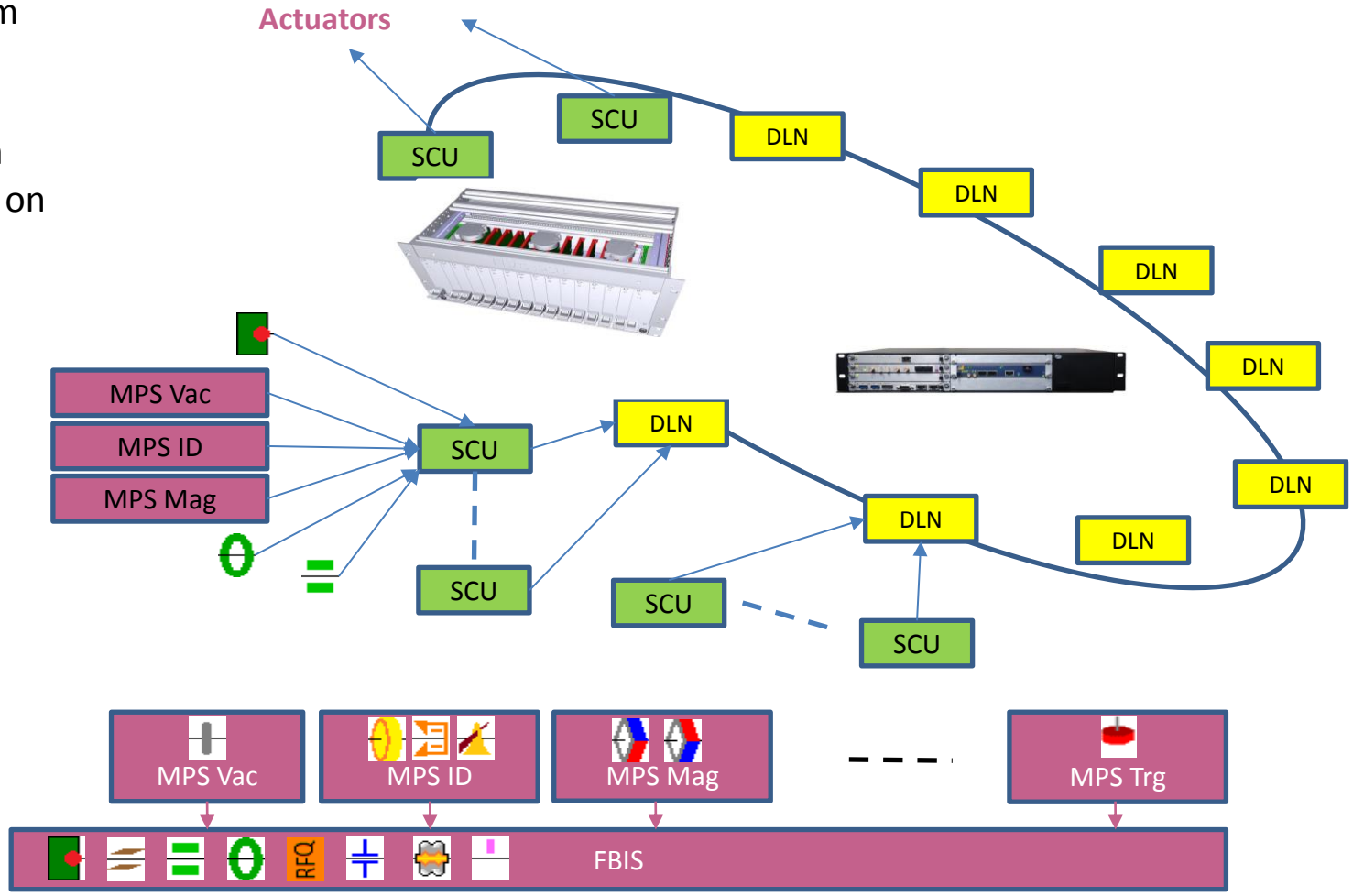
The Fast Beam Interlock System

- **SCU** (Signal Converter Unit) concentrating signals from **Sensor Systems** and **MPS PLC based systems**

- **DLN** (Decision Logic Node) concentrating signals from several SCUs, deriving global beam permit and acting on **Actuators** to stop Beam

FPGA based systems, Fast ! Reaction time ~ 5us
- SCU HW design based on standard mechanical components (cPCI)
- DLN based on MTCA
  - IFC_1410
  - SFP links to connect to SCUs.

DLNs connect to Optical Protection Line
- Light is intercepted by a DLN when an interlock situation is detected
- No hierarchical tree or other structure, no “master” node



Applications #3: Beam Diagnostics Systems on MTCA

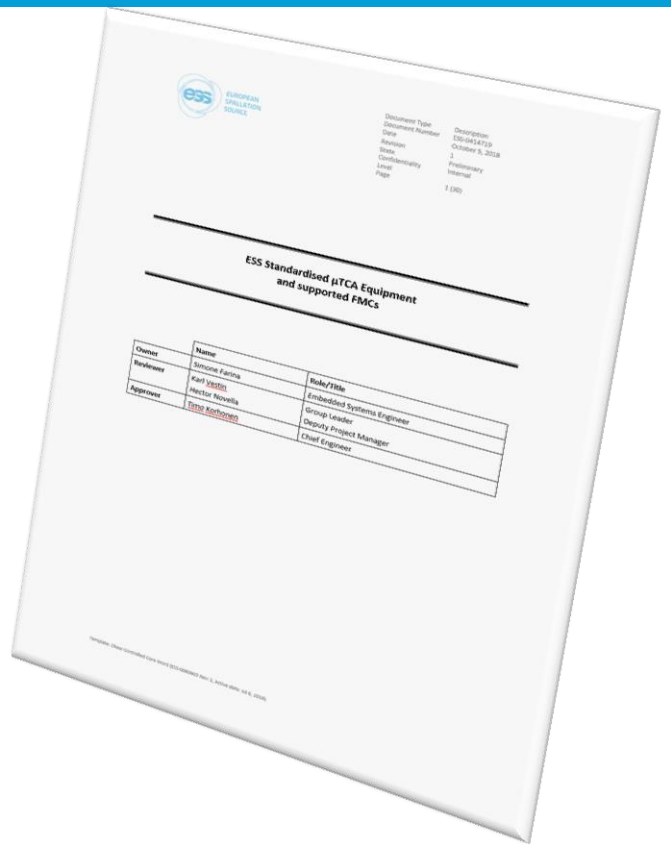
EUROPEAN SPALLATION SOURCE

- Beam Current Monitors
- Beam Loss Monitors
  - Crucial for Machine Protection
- Beam Position Monitors
- Some Target Monitoring systems
  - Camera-based, processing (partially) in FPGA
- Faraday Cup signal acquisition
- Emittance Meter Units
- Wirescanners
- All of these need data acquisition and processing in (several) MHz speed range
  - No time to go into details in this talk.

Standardization Process for MTCA

Comprehensive list of equipment including:

- Infrastructure components:
  - Chassis
  - Power modules
  - MicroTCA Carrier Hubs
  - Chassis replacement parts
- Specialized AMC cards:
  - High performance CPU
  - Data Acquisition
  - Timing synchronization
- Versatile AMC cards:
  - FMC carrier
  - RTM support card
- RTM cards
- FMC modules



MicroTCA Chassis (1)

Two different chassis types for production deployment:

- 12 slots 9U for systems requiring more than 6 AMCs and/or more than 4 RTMs or redundant low noise power modules;
- 6 slots 3U to reduce system space in racks.

Front to rear cooling scheme

Tradeoffs:

Supported Components	9U	3U
MCH(s)	2	1
Power Module(s)	4 (3+1)	2 (single width)
Cooling Unit(s)	2 (push-pull)	2 (pull)
AMC(s)	12	6
RTM(s)	12	4

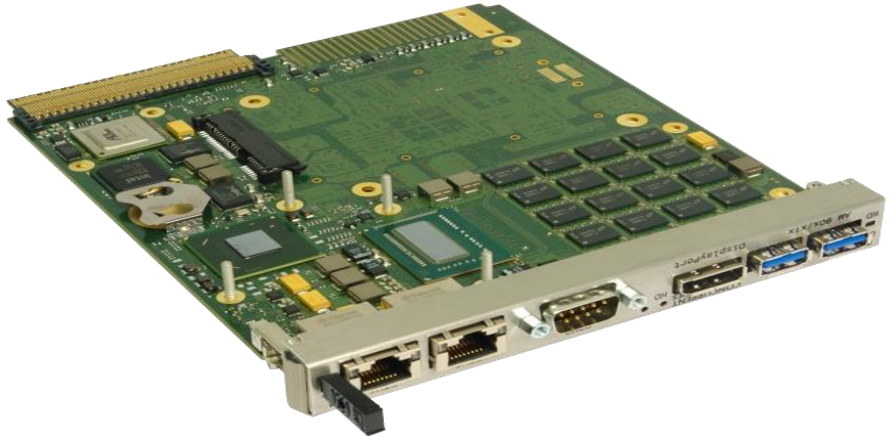
MicroTCA PM & CPU

Power Modules:

- Wiener (1KW)
- N.A.T. (600W)

Both will be used. Choice according to:

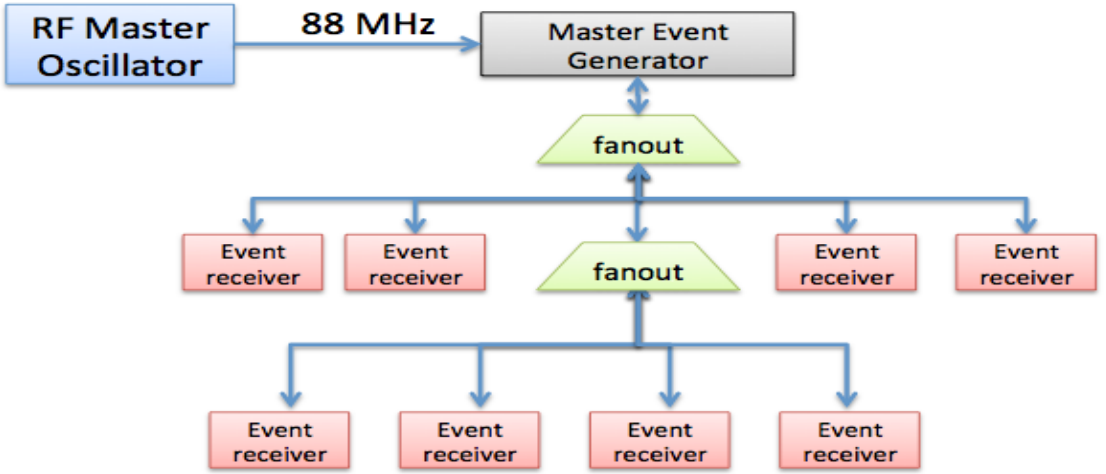
- Noise requirements;
- Redundancy;



Concurrent Technologies AM900:

- Intel i7 x86-64 architecture
- Up to 16GB DDR3 memory
- PCIe upstream

MicroTCA-based Timing System (Micro-Research Finland)



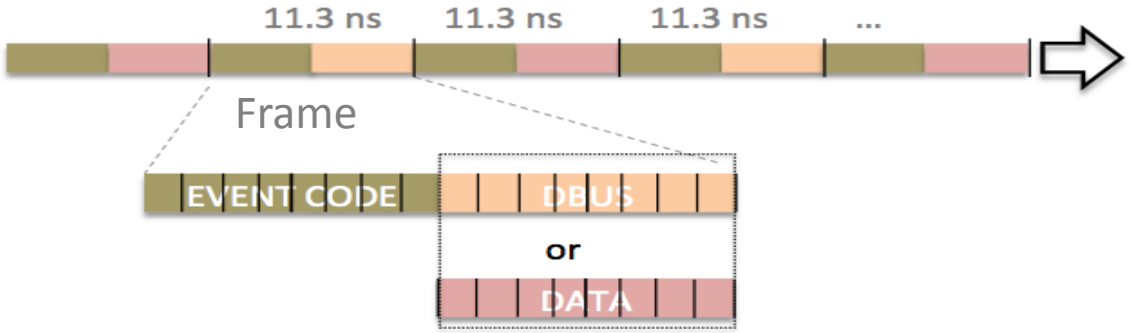
Provides the base frequency of ~14 Hz
(derived from 88.0525 MHz)

Provide timestamping

Provide trigger and clock signals
(using ports 17 to 20 and TCLKA/TCLKB)

Frames sent by Master Event Generator :

- contains an 8-bit event code and alternating distributed bus/data byte (8 bits).
- Distributed bus (DBus) broadcasts eight binary signals which can be output from each Event Receiver.
  Clocks, status bits, etc.
- Event Generator can broadcast arbitrary data
  (up to 2kB blocks)
- Event propagation also upstream
  - Also data propagation, but not foreseen for use right now



MicroTCA AMC Timing, Event Receiver and Generator/Master

Timing system EVR:

- clocks from/to TCLKA/TCLKB
- driving/receiving differential triggers AMC RX/TX ports 17 to 20 (MLVDS)
- front panel 4 x TTL outputs, 2 x TTL inputs
- front panel 2 Universal I/O modules
- Delay compensation with feedback

Timing system EVM (Event Master: Generator and Fanout)

:
- Compatible with other 300-series form factors (VME, cPCI)
- Dual functionality: Event Generator or Fanout module
  - 1-to-7 fanout
- Integrates also two Event Receivers
- EPICS integration tests ongoing

MicroTCA AMC FMC carrier

IFC1410, by IOxOS SA

in-kind contribution from PSI, Switzerland

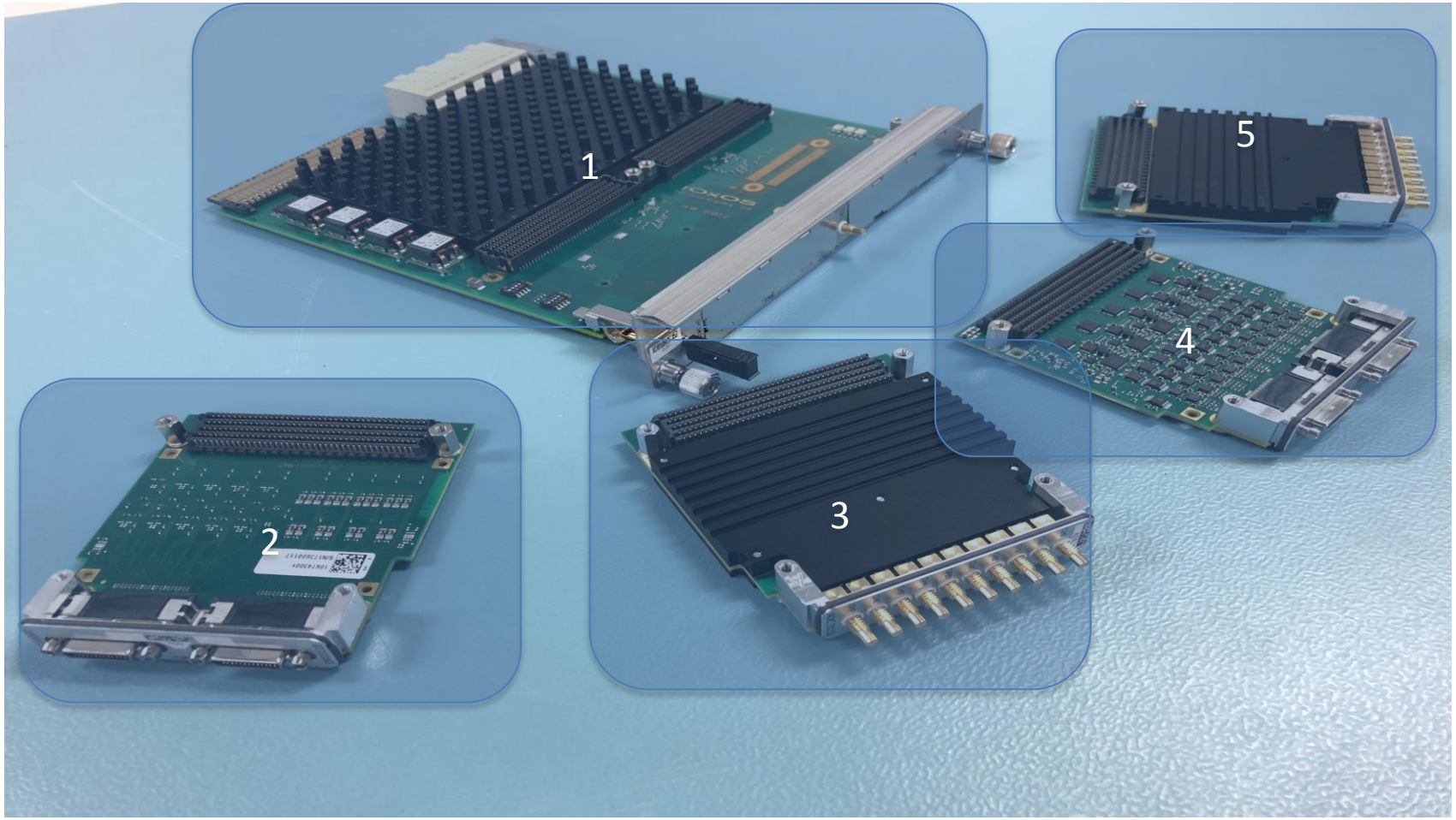
Processing System:

- NXP T2081 PPC running at 1.8GHz
- 2GB DDR3L (upgrade path to 4GB with ECC)
- 64 MB SPI Flash memory
- 512MB NAND Flash
- PCIe x4 gen.3 connection to Programmable Logic (no direct connection to backplane)

Programmable Logic:

- Xilinx Kintex Ultrascale KU040 (vertical migration KU060)
- 2x 512MB DDR3L
- 3 PCIe End Points (x4 gen.3 to backplane)
- 2 HPC FMC support
- Support for non-standard form factor mezzanine card (ie FBIS connection) on AMC side 1 or 2
- Zone3 connector (RTM support) compliant to class D1.4

I/O cards, readily available (selection)



A selection of MTCA cards:

1. IFC_1410 AMC
   - Carrier board
2. DIO_3118
   - Digital in/out
3. ADC_3110
   - 250 MSPS ADC, 8 Ch
4. ADC_3117
   - 5 MSPS ADC, 20 Ch
5. ADC_3111
   - Like #3 but DC-coupled

Cards not in photo but available:

- ECATS
  - EtherCAT slave interface
- FMC-Cameralink
  - Integration of cameras

Two ways of modularization

- FMCs have been proven to be a very flexible solution for many applications
  - Reuse of the digital platform and infrastructure around it
  - Supports different types of I/O
  - Excellent performance is achievable even with the small footprint
- MTCA.4 enables compact systems
  - All electronics in one chassis – no, or at least fewer external “pizza boxes”.
  - Signal routing from the backplane
    - Less cable clutter on the front side (advantageous, even if this moves the clutter on the rear side…)
  - However: I/O standardization is an issue
    - DESY recommendations for standard I/O pin allocation tries to address this
    - Ideally, enables creation of interoperable “ecosystem” of board-level solutions
    - Wider adoption of these recommendations in practice has been challenging
- Can these advantages be promoted?
  - We have at least tried...

MicroTCA AMC DAQ IFC1420

piggyback slot for Beam Interlock System interface

IFC1411 + DAQ1430:

in-kind contribution PSI

Processing System:

Same characteristics as IFC1410

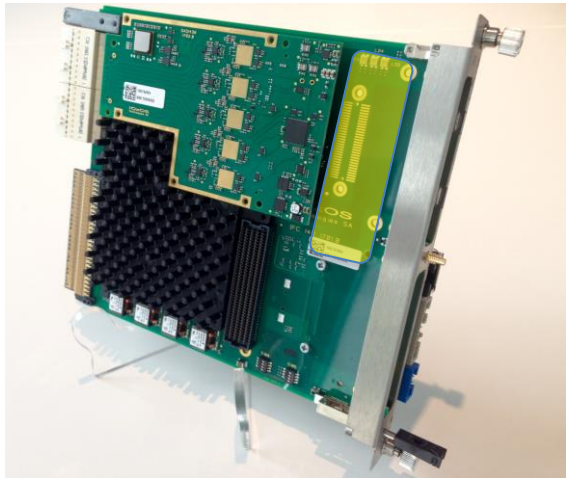
Programmable Logic:

- Xilinx Kintex Ultrascale KU040
  - (vertical migration KU060)
- 2x 512MB DDR3L
- 2 PCIe End Points (x4 gen.3 to backplane)
- 10 ch ADC 250MSPS 16-bit (DAQ1430)
- 4 ch DAC 2.5GSPS 16-bit (DAQ1430)

Intended for use with RTMs that conform to the Class A1.1 recommendation:
Downconverters, signal conditioning

- Internal, Front Panel and Backplane Clock Sources
- 1 HPC FMC support
- Support for non-standard form factor mezzanine card (ie FBIS connection) on AMC side 1 or 2
- Zone3 connector (RTM support) compliant to class A1.1CO

Speciality of IFC_1420



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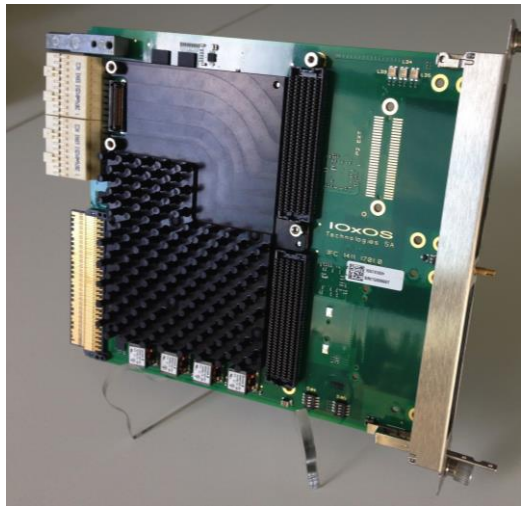

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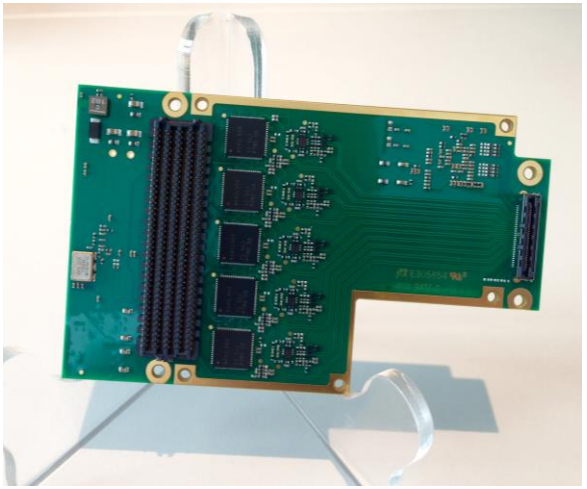
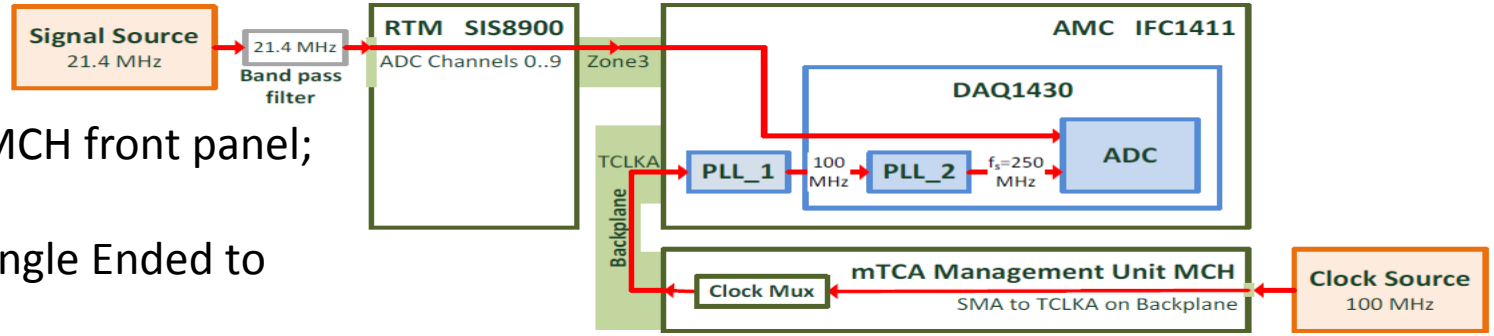


IFC_1420 implements the DESY (and PICMG) recommendation for analog signals A1.1

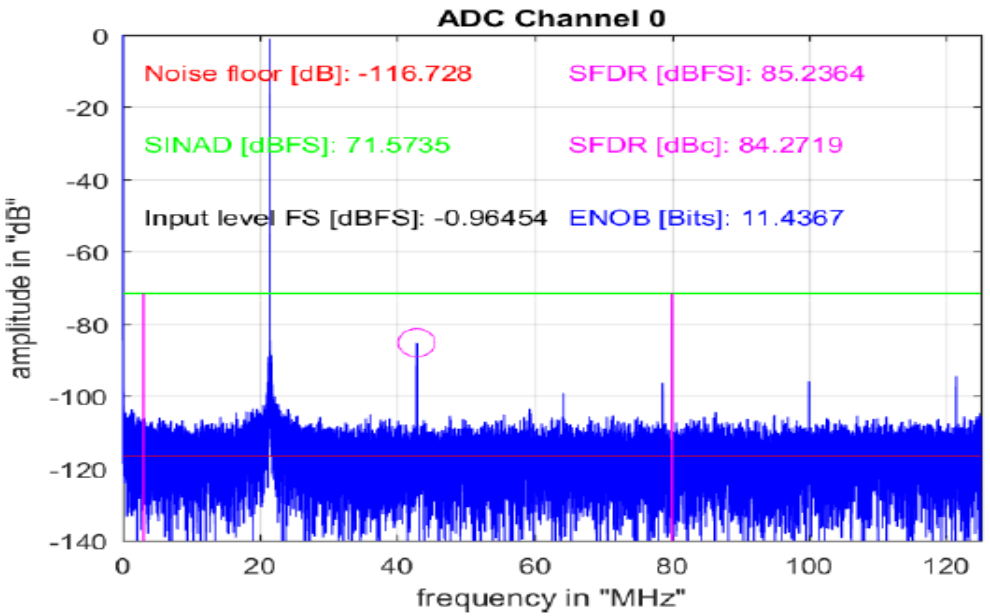
- Compatible with available RTMs, e.g., Downconverters designed at DESY (available from STRUCK)
- Usually ADC boards have a fixed design; change of ADC requires change of AMC board (and FPGA, and..)
- With IFC_1411, mezzanine (DAQ1320) can be replaced for different applications
- Digital interface of the ADC mezzanine is **conform with FMC standard** (mechanical interface obviously not)
  - Push for standardization of this idea, maybe…

MicroTCA AMC DAQ IFC1420 characterization



Test setup:

- ADC clock source by TCLKA (backplane) from MCH front panel;
- Filtered sinusoidal input source at 21.4 MHz;
- SIS8900 RTM signal conditioning board with Single Ended to Differential circuitry;
- **Besides the nice results, verified I/O interoperability** 👆



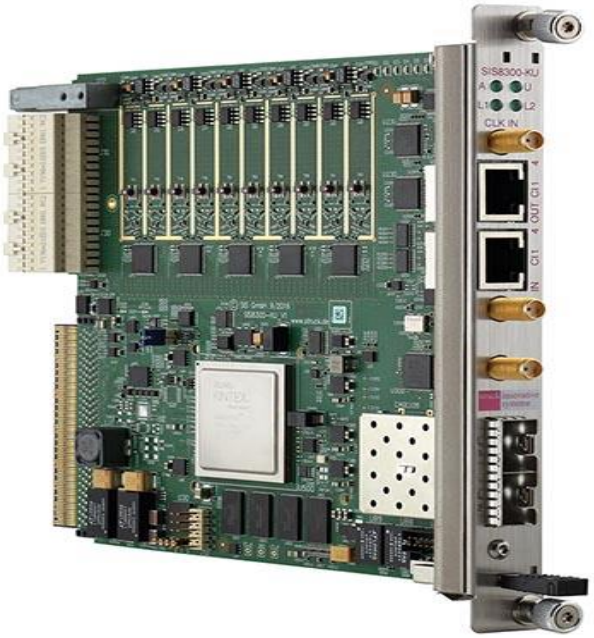
Average Analog Performance of the 10ch:

ENOB	11.56 Bits
SFDR	84.17 dBFS
SNR	70.33 dBc

Comparison with Analog Performance of ADC3110 (8ch 250MSPS 16-bit ADC FMC card) :

ENOB	11.84 Bits
SFDR	87.54 dBFS
SNR	72.04 dBc

MicroTCA AMC ADC - well known to everybody here ☺



SIS8300-KU:

COTS AMC card

Programmable Logic:

- Xilinx Kintex Ultrascale KU040
- 2 GB DDR4
- x4 gen.3 PCIe End Point to backplane
- 10 ch ADC 125MSPS 16-bit
- 2 ch DAC 16-bit
- Internal, Front Panel, RTM and Backplane Clock Sources
- Support for up to 2 SFP+ modules for high speed system interconnect
- 2 front panel RJ45 for external I/Os (eg BIS connection)
- Zone3 connector compliant to class A1.1CO

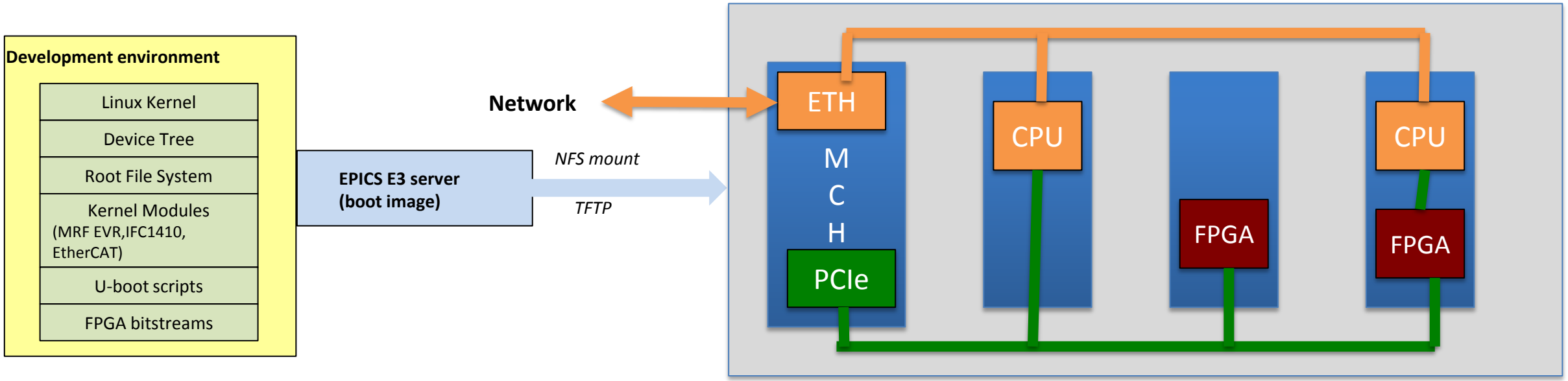
Similar in function to IFC_1420

- Used in e.g., LLRF and BCM

Firmware development for ESS applications

- Our in-kind contribution includes a development stack (IOxOS, Ivan Garcia talk)
  - Firmware framework TOSCA, source code level
  - based on PCI Express interfaces and a Network-On-Chip architecture
  - (linux) kernel and initial EPICS drivers for the framework
  - This is used for all IFC-based applications
- In-house developed framework for the Struck platform (Christian Amstutz talk)
  - Due to need of extensions and modifications to the vendor FW, this framework has been developed in-house
  - Covers applications for Struck and another, in-kind developed board
  - Based on Xilinx IP and AXI framework
- Software stacks are required for both of these
  - Kernel drivers, EPICS drivers

MicroTCA software&firmware architecture



- Multiprocessing architecture: central + local CPUs
  - Eventually, not all established yet…
- Operating System(s): Linux (Yocto, or CentOS) with Realtime (RT) Patch
  - EPICS on either a central CPU, on the IFC local CPU, or both (scalability, application-specific processing)
- All software/firmware modules are in an on-line BitBucket/GitLab repository
  - All updates of e.g., kernel modules or new FPGA firmware versions

“Procurement for Innovation” initiative

- ESS Procurement came up with an idea to utilize large procurements to drive innovations in industry
  - This can also be applied to MTCA.4 infrastructure
  - Development of new features, applications
  - Drive for future standards and extensions of standards
- Two workshops to this effect have been held
  - Participants from industry and (scientific) users
  - New features to be implemented in the (near) future have been discussed
    - Increased bandwith, power per slot and so on.
  - Setting up a project organisation
- Our (ESS) problem:
  - We are too busy with ESS!
  - Too little manpower to promote the innovation project, even if it is nice and interesting.
  - If you are interested to join us and help, please let me know (**hint** ☺)
    - Catch me at a coffee or lunch break, or anytime.

Summary

- MTCA used in several high-speed applications
- Standard selection of components available
  - Only standards are guaranteed to have support
  - Not all showed or mentioned in these slides
- Mostly commercial and in-kind contributed components
  - Little internal staff – yet – to drive developments
  - Still, quite many areas can be covered
    - In some cases, system development is just starting
- MTCA has evolved
  - Much less interoperability issues today than in the past
  - Integration of monitoring and management is a nice feature
  - Performance is good (high signal-to-noise ratios)
- Discussion