



MicroTCA Technology Lab at DESY Summary of 1st Year Operations

Jan Marjanovic on behalf of Thomas Walter
2018-12-05

MTCAWS 2018, Hamburg

microTCA
TECHNOLOGY LAB

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES





TRANSFER MTCA TO RESEARCH AND INDUSTRY

- ▶ Custom developments
- ▶ High-end test & measurement services
- ▶ System configuration & integration
- ▶ LLRF design

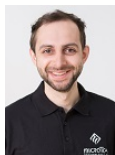
Marketing.
Services & Support.
Tech-Shop.

- ▶ Helmholtz funded project, Funding: 5 mio EUR/5 years
- ▶ Goal: foster the MTCA standard in Industry
- ▶ "Enabling space" for innovative ideas and new business models
- ▶ Cooperation of DESY and several partners from industry
- ▶ Start of renovation, hiring in Oct 2016, Official opening in April 2018
- ▶ Size of the lab: ~ 10 FTE in January 2019

Status



Dr. Thomas
Walter



Aaron
Gornott



Çağıl
Gümüř



Christoph
Kampmeyer



Jan
Marjanovič



Johannes
Zink



Dr. Patrick
Nonn



Stanislav
Chystiakov















Susanne
Schuster



Sven
Stubbe



https://techlab.desy.de/partners/index_eng.html

	Bevatech GmbH		CAEN ELS s.r.l.
	el-spec GmbH		EMCOMO Solutions AG
	N.A.T. GmbH		nVent Schroff
	powerBridge GmbH		Rohde & Schwarz
	Teledyne SP Devices		Struck Innovative Systeme GmbH
	VadaTech		WIENER Power Electronics GmbH

We (together with our industrial partners) participated at:

- ▶ Embedded World (at PICMG booth)
- ▶ IPAC 2018 (with Rohde & Schwarz)
- ▶ IEEE RT conf 2018 (with NAT)
- ▶ IBIC 2018 (with Struck)
- ▶ LINAC 2018 (with WIENER)
- ▶ Electronica (with CAEN ELS)
- ▶ ...

In 2018 we have also organized several MicroTCA micro-conferences:

- ▶ Real Time conference pre-workshop
- ▶ at Diamond Light Source
- ▶ IBIC 2018 pre-workshop
- ▶ Workshop on beamline instrumentation for scientists and engineers
- ▶ Photon Science Day

slides available here: https://techlab.desy.de/events/archive/index_eng.html

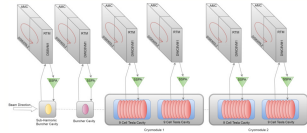
Projects

- ▶ LLRF developments
 - ▶ TARLA, NICA, ...
- ▶ System integration
 - ▶ Trioptics WaveScan - quality inspection system
 - ▶ configurator
- ▶ Custom developments
 - ▶ GigE Vision
 - ▶ FMC+ carrier with Zynq MPSoC
 - ▶ DFMC-DS800 board with new Zone 3 analog class
 - ▶ Board Support Package for TCK7
 - ▶ MMC System on a Module
- ▶ Measurement services
- ▶ Supporting activities

Turn-key solutions for LLRF, based on experience from FLASH and European XFEL.



Turkish Accelerator and Radiation Laboratory Ankara

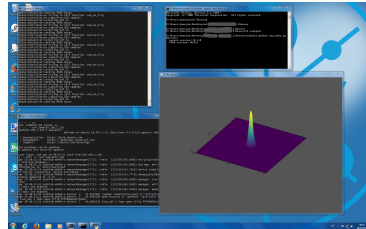
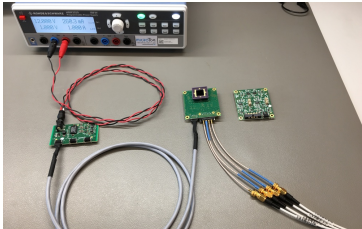
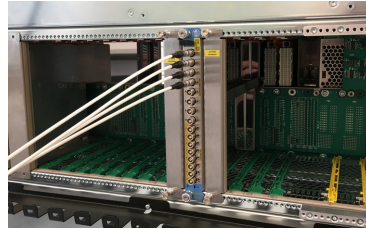


System integration test at DESY & preparation for final rack assembly

Talk on Thursday at 10:15 by P. Nonn:

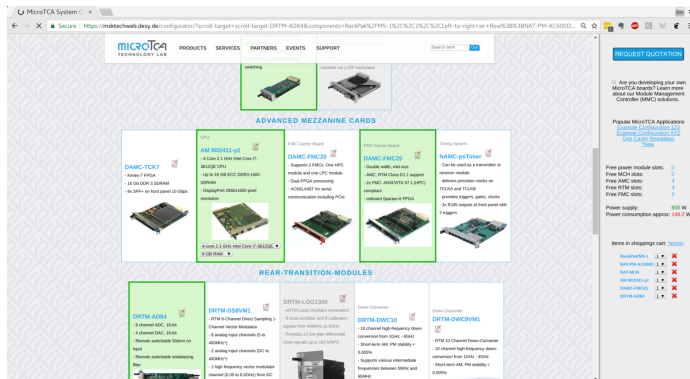
”Overview and status of LLRF system developments at the MicroTCA Technology Lab”

example: Trioptics WaveScan - high-end quality inspection system



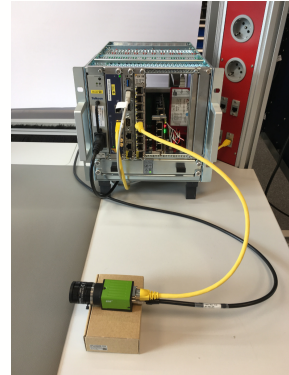
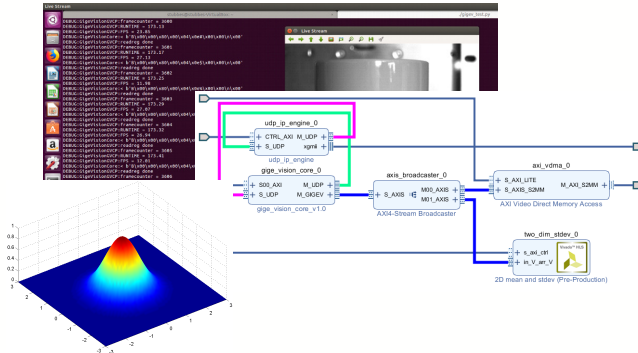
Web-based tool to assemble custom MicroTCA system.

Accessible at: <https://msktechweb.desy.de/configurator/>



Talk on Wednesday at 12:00 by H. Betancourt (powerBridge):
"The MTCA Configurator tool"

Implementation of GigE Vision protocol (with 1/10 GbE UDP/IPv4 engine) in FPGA.

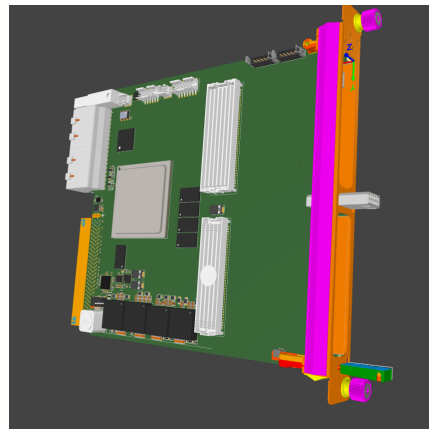


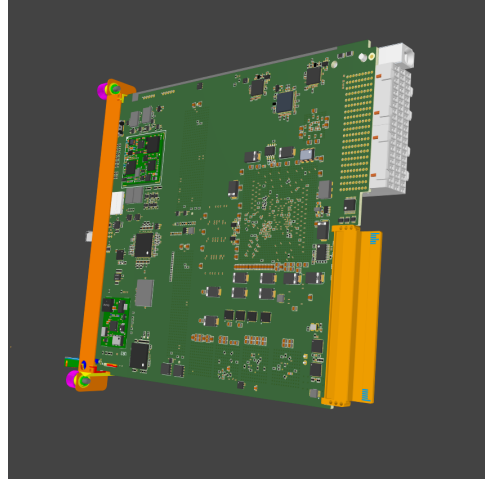
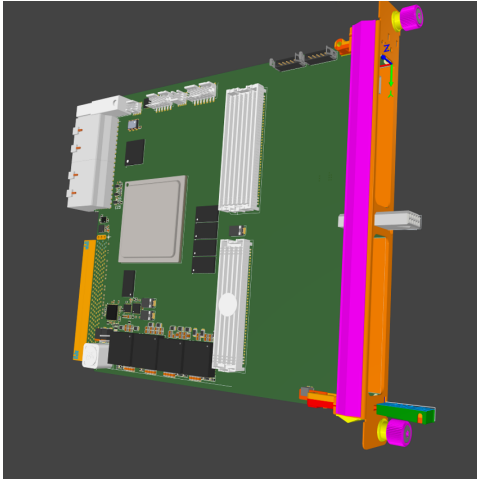
Talk on Thursday at 9:45 by S. Stubbe:

"Implementation of GigE Vision standard and applications in MicroTCA"

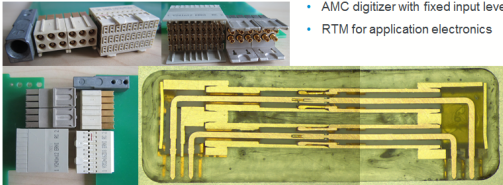

DAMC-FMC2ZUP FMC+ carrier

- ▶ high-end FMC+ carrier in MTCA.4 form factor
- ▶ based on Xilinx Zynq MPSoC
 - ▶ quad-core 64-bit (ARM® Cortex®-A53)
 - ▶ real-time co-processor (ARM® Cortex®-R5)
 - ▶ large FPGA (650k logic cells, 2920 DSP)
 - ▶ transceivers: 32 GTH (16 Gbps), 16 GTY (28 Gbps)
 - ▶ hard IP blocks (PCIe Gen3, 100G Eth, Interlaken)
 - ▶ ARM® Mali™-400MP multicore GPU
- ▶ 16x GTY transceivers (28 Gbps) on FMC+
- ▶ flexible clocking scheme, White Rabbit endpoint
- ▶ front-panel trigger and clock input over Harlink
- ▶ Zone 3 according to class D1.1
- ▶ backwards-compatible with DAMC-FMC25
- ▶ available Q2/2019, first licensee CAEN ELS





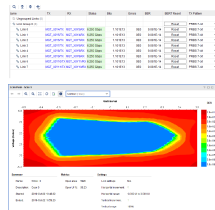
New Analog Zone 3 class for high-frequency signals (up to 6 GHz), new AMC digitizer

DAMC-DS800		Fast FMC/AMC Digitizer Development at MSK
		J.Zink, 2018-11-21, Hamburg
		10
<ul style="list-style-type: none">• new analog Zone3 Class will be introduced• new single-ended Zone3 connectors developed• signals up to 6 GHz can be transmitted from RTM side	<ul style="list-style-type: none">• improved isolation between conductors in one insert• isolation of -70 dB up to 3 GHz• THT mounting or cable feed trough possible• AMC digitizer with fixed input levels• RTM for application electronics	
		
DESY Photon Science Day, Hamburg 2018		
		

Talk on Thursday at 12:00 by J. Zink:

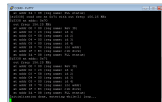
”Direct Sampling of RF Signals up to 3 GHz in MTCA.4”

Vivado project including support for PCIe, DDR3, clock configuration, IBERT on SFP+ and UDP/IPv4 beacon on AMC port 0; available under permissive license (3-clause BSD)

[illegible]

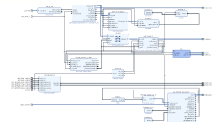
It is necessary to reset the CPLDs by writing 1 and then 0 to PORT.CPLDRESET in both CPLDs. Another alternative solution is to configure the FPGAs for the second time; the oscillators are already stable at this point and the CPLDs will work.

On-board clock configuration



Recreating project

This project requires Maple version 1817.4



10. *Journal of the American Statistical Association*, 92, 1997, 1039-1047.

- ```
1. cd into project dir
2. source ../scripts/setupenv.sh
3. source ../scripts/setIP.sh
4. source ../scripts/unpack.sh
```
- To compile the project:
- ```
1. launch run_ipi.sh to stop write histogram jobs
2. Grab a coffee, this is going to take some time
```

Setting up so

Setting up software development environment

1. Create IntelliJ diagram and it's wrapper (see "Recreating project")
2. From Visuals open SDK (File -> Launch SDK)
3. For **Exported location** select `<workspace>sw` for **Workspace** select `<workspace>`
4. Xilinx SDK will open
5. Import project. File -> Import -> Existing Projects into Workspace
6. **Select root directory** is `<workspace>`
7. Make sure that both tool based controller and tool based controller base are selected

Committing changes

Block diagram

From product line

```
writeb hd tail :include lcnash :form ..../xasids/hd.tl
```

Update MicroBlaze init script

1. Copy generated `all` into `ofibc/sdk/all`
2. Add `all` to Vivado project
3. Set parameters `SCREEN_TO_CELL` to `accr@accellera.org` and `SCREEN_TO_HDL` to `system`

Project settings

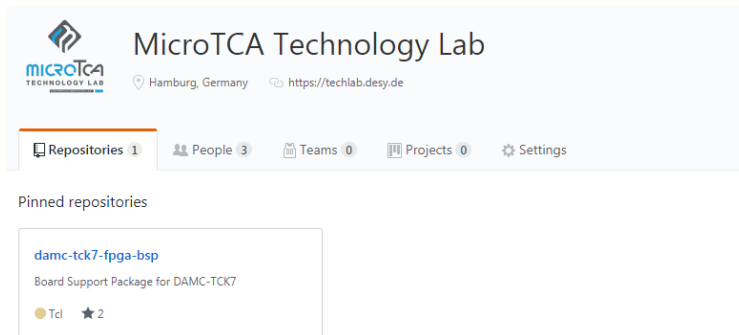
If you need to update version 3.1, run

```
write -p 'ask: tel: ' >> tel; if [ $? -eq 0 ]; then
```

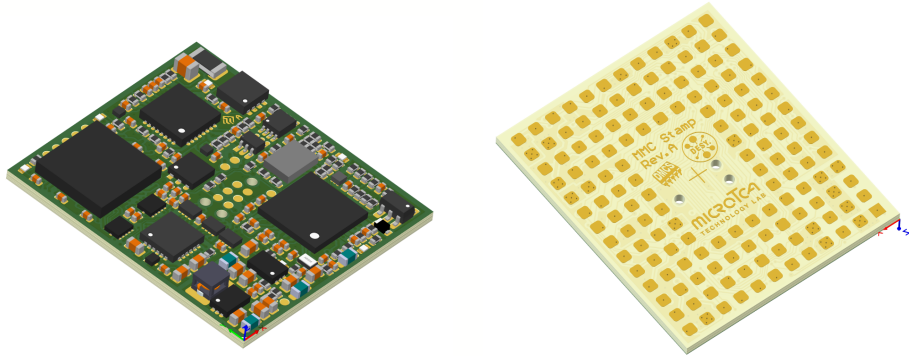
Please be careful as there are some hand-crafted modification in recreates to

We understand the needs of the community and are committed to provide open-source solution when commercially viable

Our GitHub page: <https://github.com/MicroTCA-Tech-Lab>

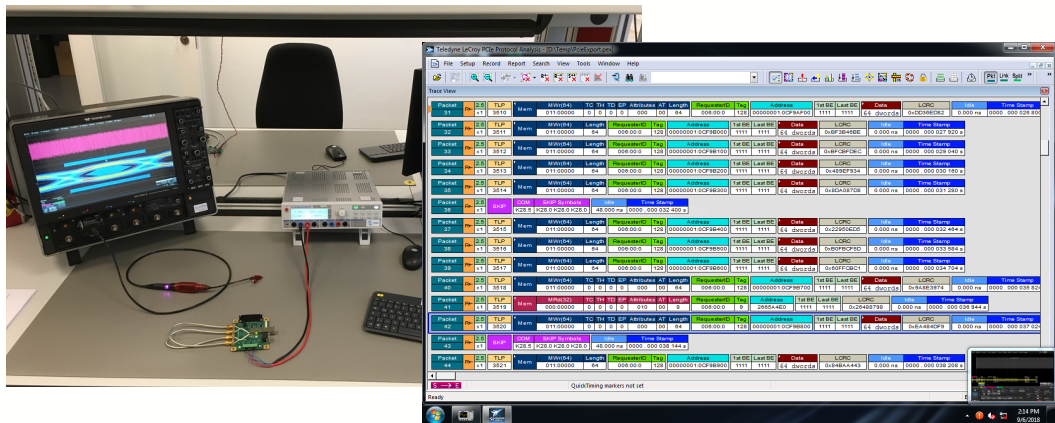


Full implementation of everything needed on management side on a single module



Talk on Wednesday at 17:45 by M. Fenner:
"DESY MMC System on a Module and its Applications"

High-end digital measurement equipment (80 GSPS LeCroy)



High-end measurement equipment from



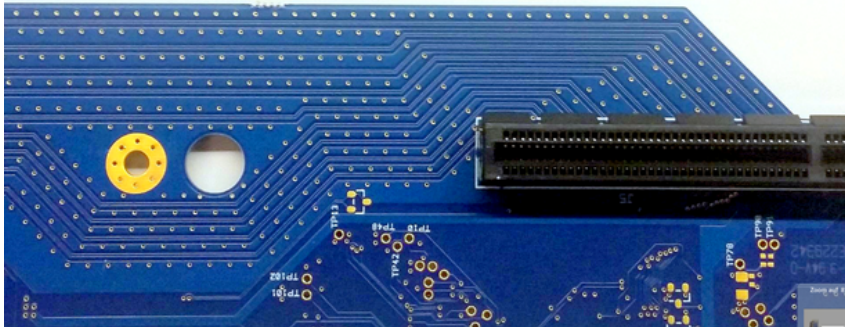
- ZNB20 → 20 GHz VNA with TDA Option
- FSWP → Phase Noise Analyzer
- RTO2064 → 6 GHz / 20 GS/s



- SMA100B → 20 GHz / 30 dBm
Ultra Low Phase Noise
Generator

We are able to solve signal integrity issues and provide consulting on high-speed PCB design, FPGA design and other areas of electronics.

Example of a board after our suggestions were implemented:



Together with N.A.T. we provide training in MicroTCA, both basic and advanced.

More info at:

https://techlab.desy.de/services/training/index_eng.html

Next dates:

- ▶ basic training: 23 - 24 January 2019
- ▶ advanced training: 2 - 13 March 2019



Website in Chinese at https://techlab.desy.de/index_cn.html

The screenshot shows the homepage of the MicroTCA Technology Lab website in Chinese. The header features the MicroTCA logo, navigation links (PRODUCTS, CONFIGURATOR (BETA), SERVICES, PARTNERS, EVENTS, SUPPORT), and a search bar. The main content area is divided into several sections:

- 我们的产品 (Our Products):** Describes the development of products and specialized equipment for industrial and scientific research, mentioning products like AMC, RTM, and FMC cards.
- 我们的服务 (Our Services):** Lists services provided by the MicroTCA Technology Lab, including hardware and software development, testing, design, and equipment rental.
- 我们的合作伙伴 (Our Partners):** Mentions that the lab provides high-end testing and development services in cooperation with partners.
- 关于MICROTCA技术实验室 (About MicroTCA Technology Lab):** States that the lab is one of the seven innovation labs supported by the Helmholtz Association.
- TECHLAB ON GITHUB:** A link to the lab's GitHub repository.
- 联系我们! (Contact Us!):** A section with the MicroTCA logo and contact information: Notkestr. 85, 22607 Hamburg, +49 (0)40 8998 1818.
- 关于 MICROTCA... (About MicroTCA...):** Describes MicroTCA as a modular and reliable electronic board architecture, highlighting its main advantages: high modularity and reliability, support for PCIe, 10G Ethernet, and other high-speed connections.

The footer includes the MicroTCA Technology Lab logo and the Helmholtz Research for Grand Challenges logo.

Near future

- ▶ New Zone 3 analog class, new AMC digitizer
- ▶ Second-sources and product variety
- ▶ BSPs for new boards (White Rabbit implementation)
- ▶ 40GbE implementation
 - ▶ up-coming AMC.2 standard
- ▶ RFSoc evaluation
 - ▶ 8x 12-bit, 4.096GSPS RF-ADC w/ DDC
 - ▶ 8x 14-bit, 6.554GSPS RF-DAC w/ DUC
 - ▶ large FPGA
 - ▶ quad-core 64-bit ARM
 - ▶ "LLRF-System-on-a-Chip"

Thank you

<https://techlab.desy.de>

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A Research Centre of the Helmholtz Association
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