EUROPEAN SPALLATION SOURCE

Generic AXI4-based FPGA Framework

Enhancements and Experience

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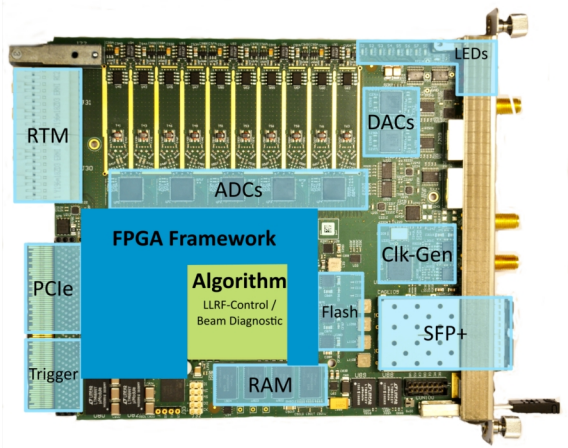
NCBJ: Jaroslaw Szewinski, Marcin Gosk, Dominik Rybka

www.europeanspallationsource.se

Concepts of the AXI4-based Framework



Flexibility

Different Boards / Different Applications

Re-use of provided IP

Xilinx tools have a lot to offer

XILINX
VIVADO

Follow Standards

e.g.: AXI4 for interconnects

Defined, scripted workflow

Repeatable code generation, easy integration of modules

→ FPGA Framework is a set of design concepts

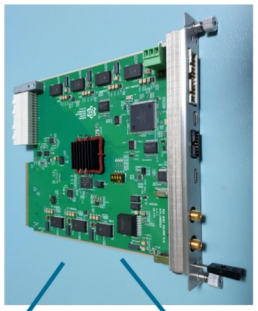
Current Applications

AMC

RTM

Struck SIS8300-KU
(Xilinx Kintex UltraScale)

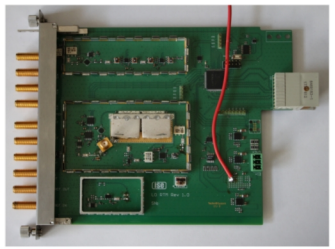
PEG RTM Carrier
(Xilinx Artix-7)



Struck DWC8VM1
Struck DWC8300

Struck SIS8900

DMCS Piezo Driver RTM
(HDP-200)



PEG Local Oscillator

Low-Level RF

Beam Current Monitor

Local Oscilator Controller

Beam Position Monitor

Piezo Driver Controller

Current Applications

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- Poster by Jaroslaw Szewinski

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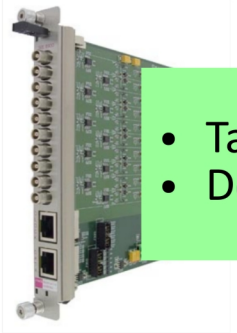
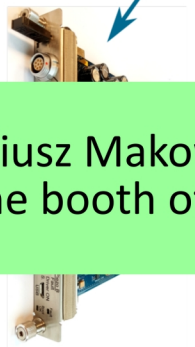


Struck SIS8900



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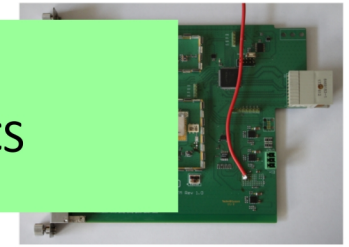


PEG Local Oscillator

- Talk by Dariusz Makowski
- Demo at the booth of DMCS

Low-Level RF

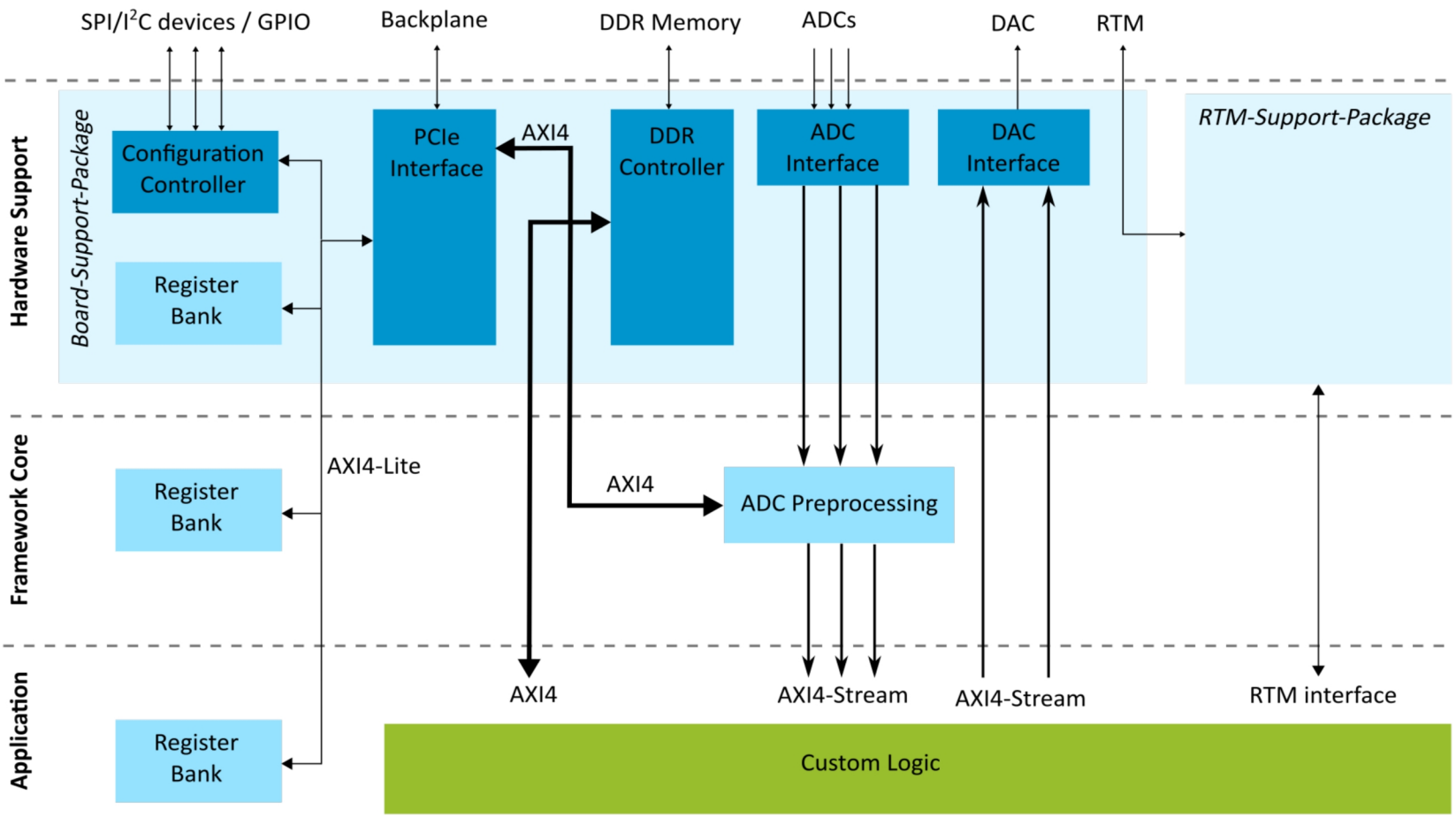
Beam Position Monitor

Beam Current Monitor

Piezo Driver Controller

Local Oscilator Controller

Functionality



FPGA Resources

Framework only

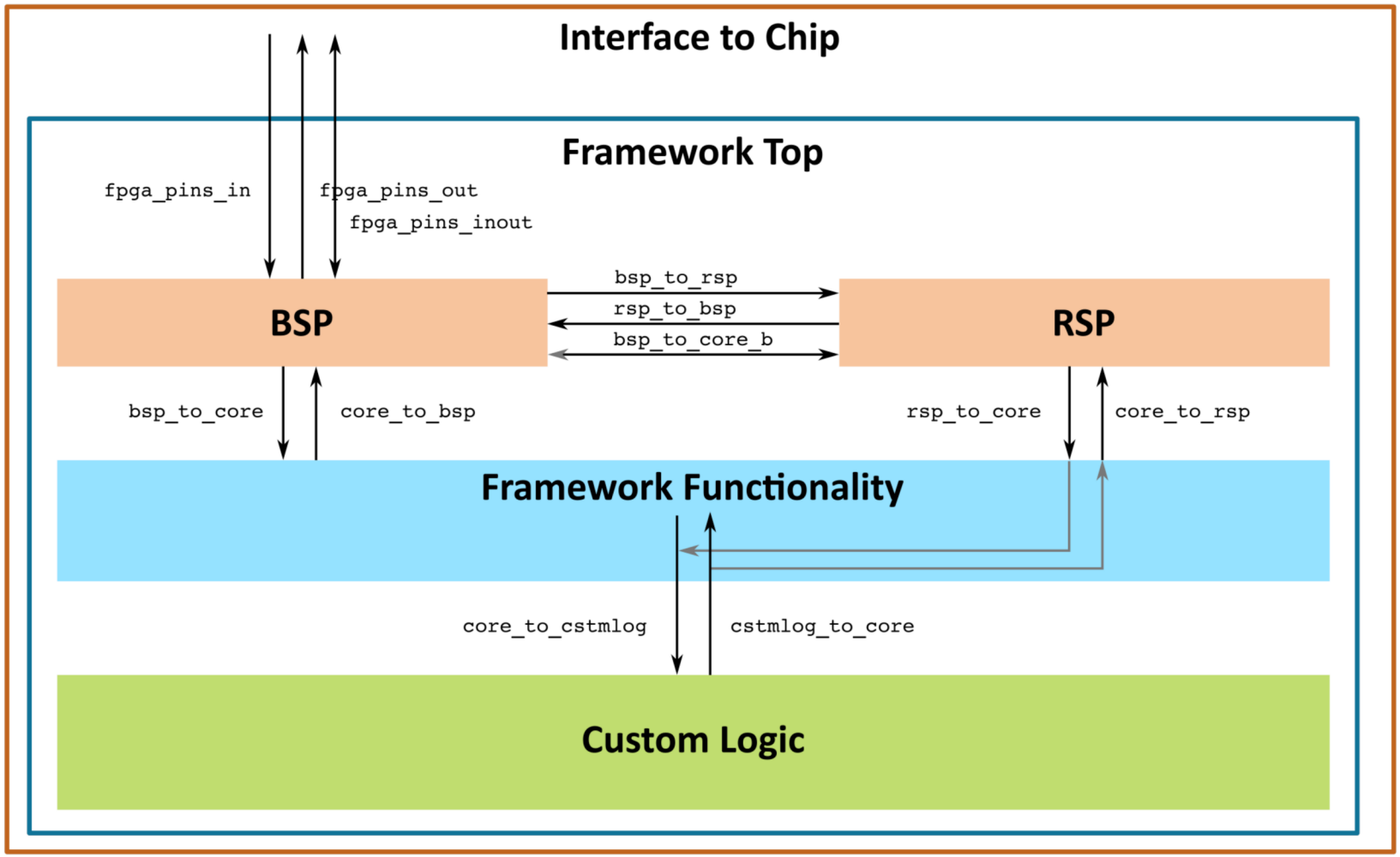
Resource	Utilization	Available	Utilization %
LUT	65457	242400	27.0
Flip-Flop	81833	484800	16.9
BRAM	289	600	48.2
DSP	150	1920	7.8
MMCM	1	10	10.0
PLL	4	20	20.0

only framework on Struck SIS8300-KU

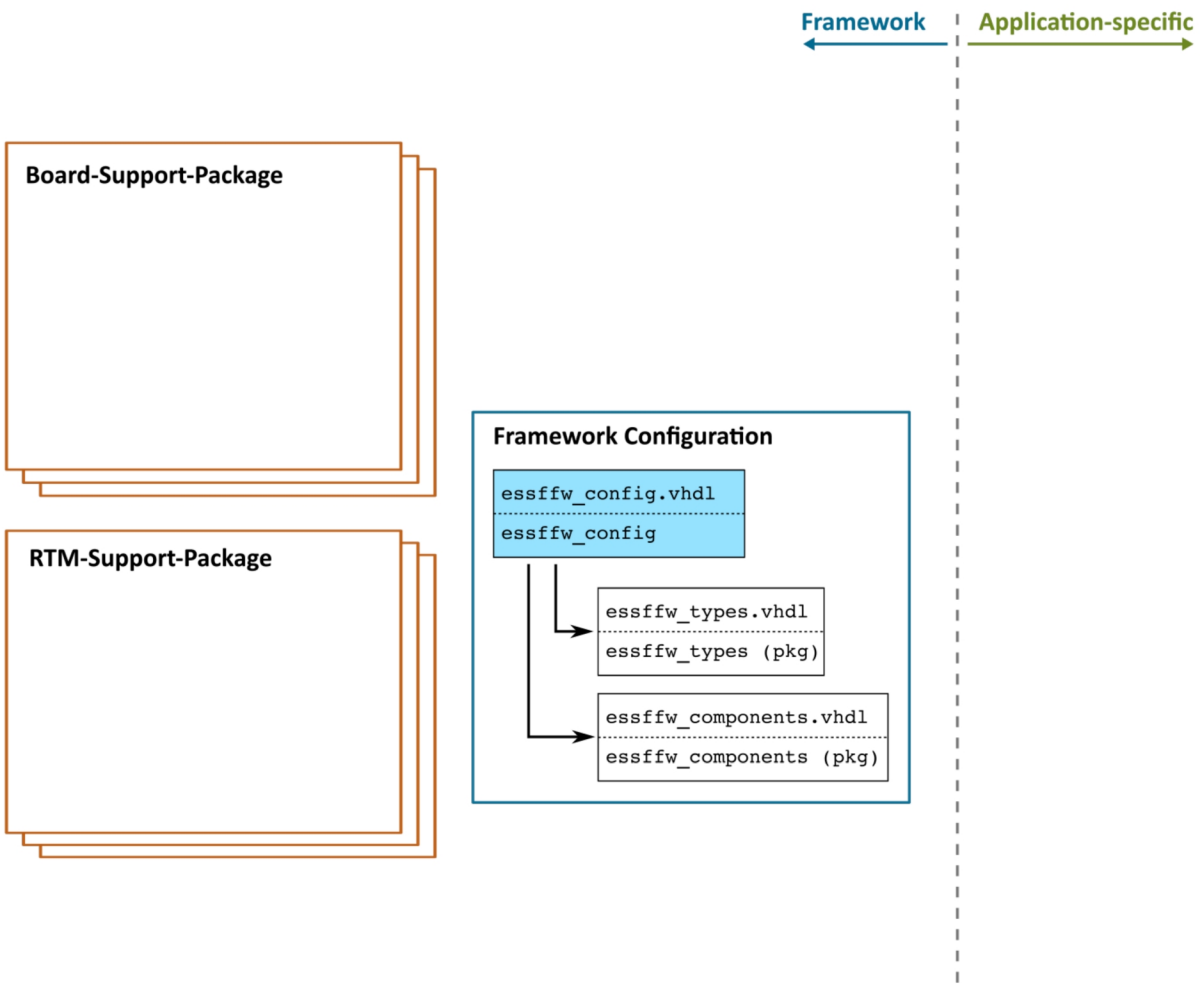
→ FPGA resources occupied by framework: below 30 %

(Device: Xilinx Kintex Ultrascale xcku040-ffa156-1-c, AXI4 bus: 512 bit @ 200 MHz, Tools: Xilinx Vivado 2017.4)

Organization in the Code



Configuration



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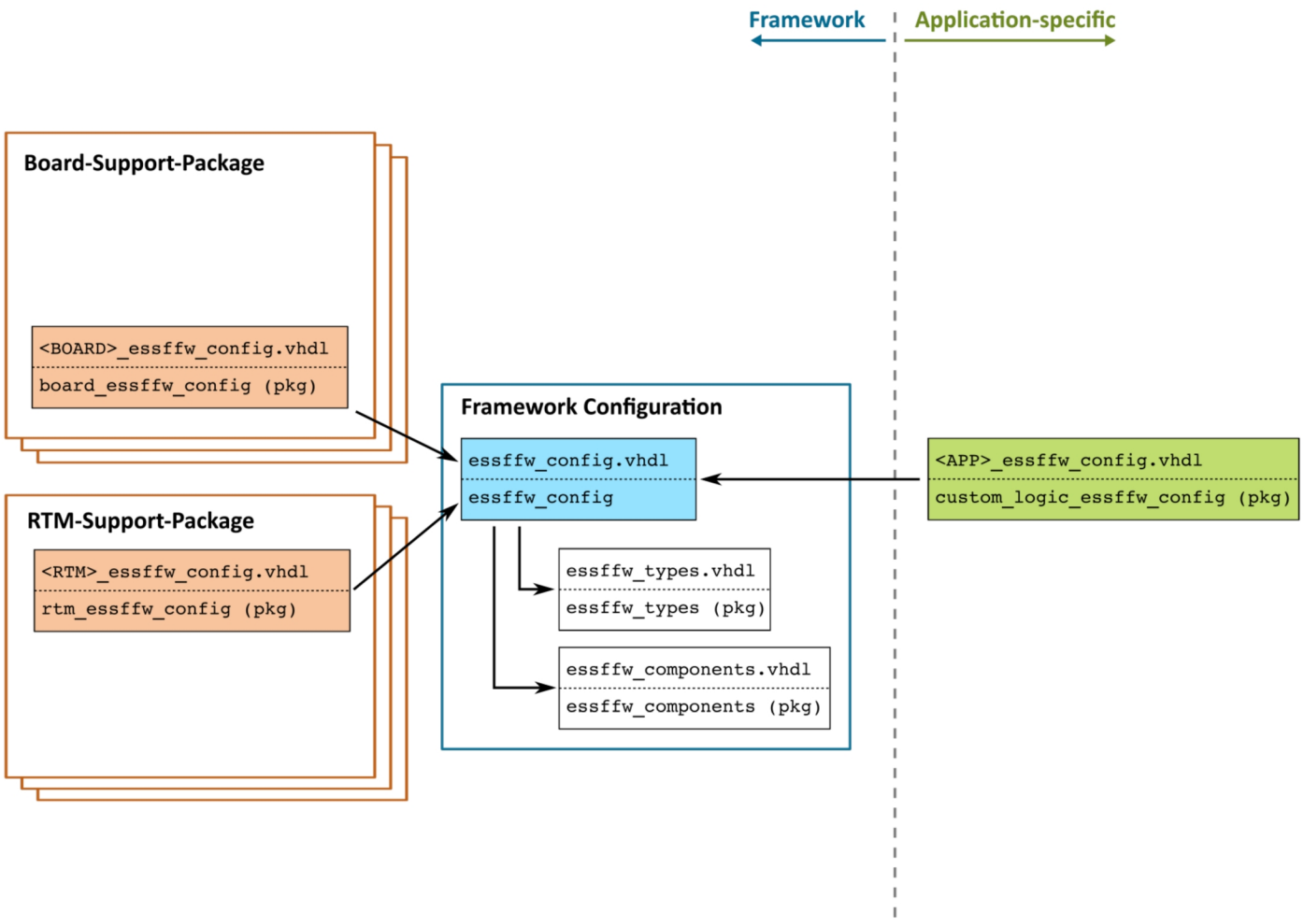

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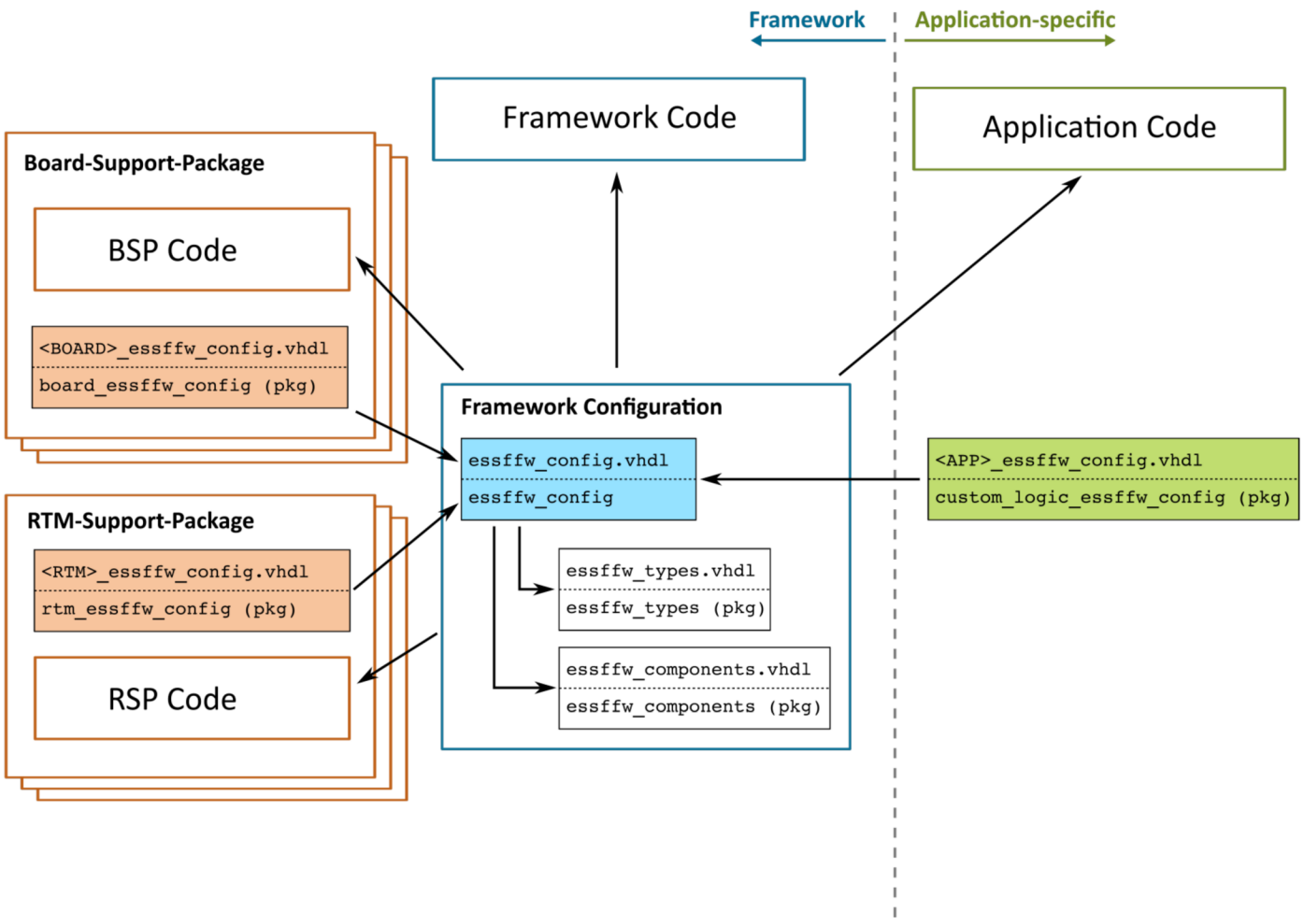
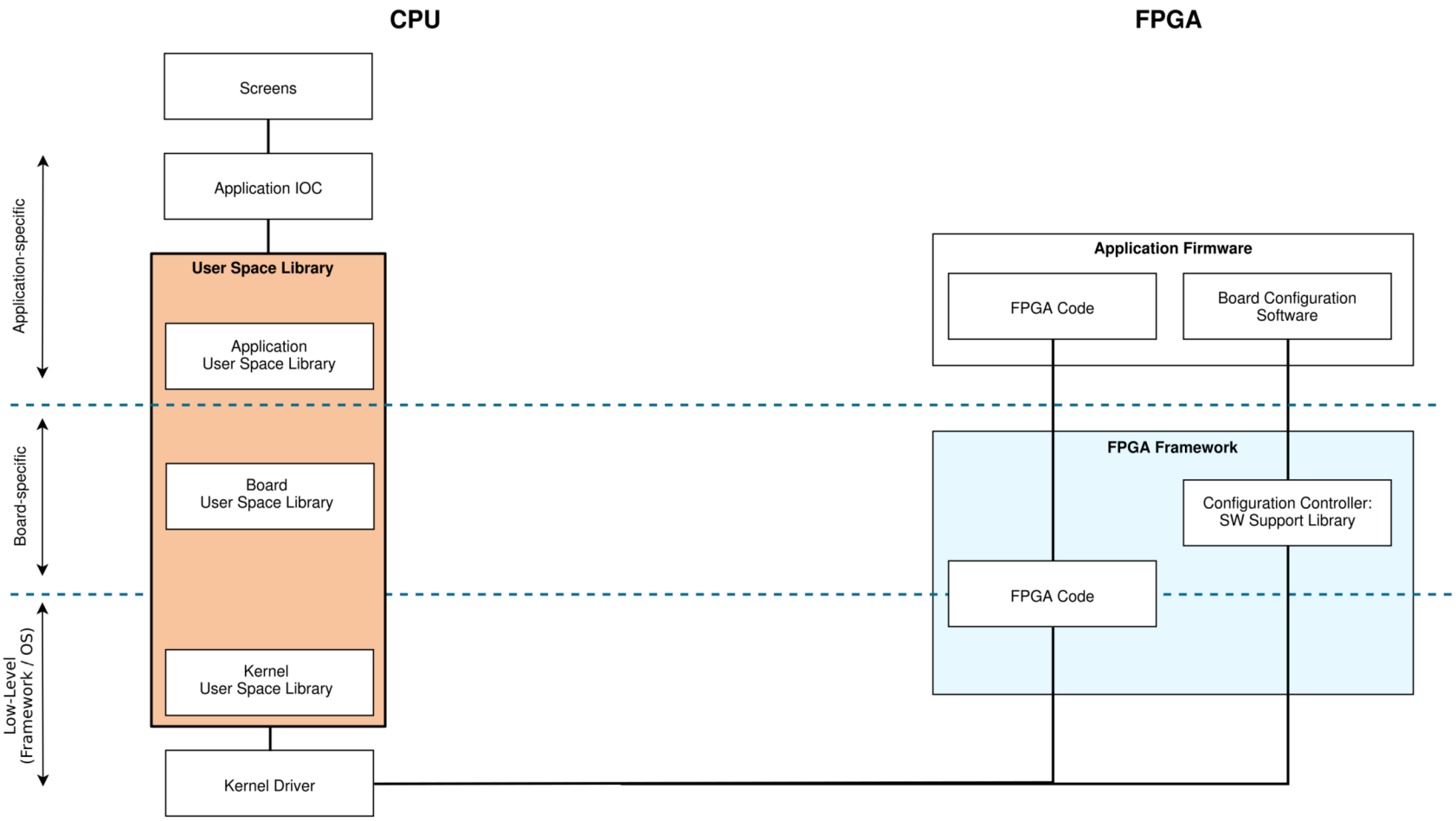
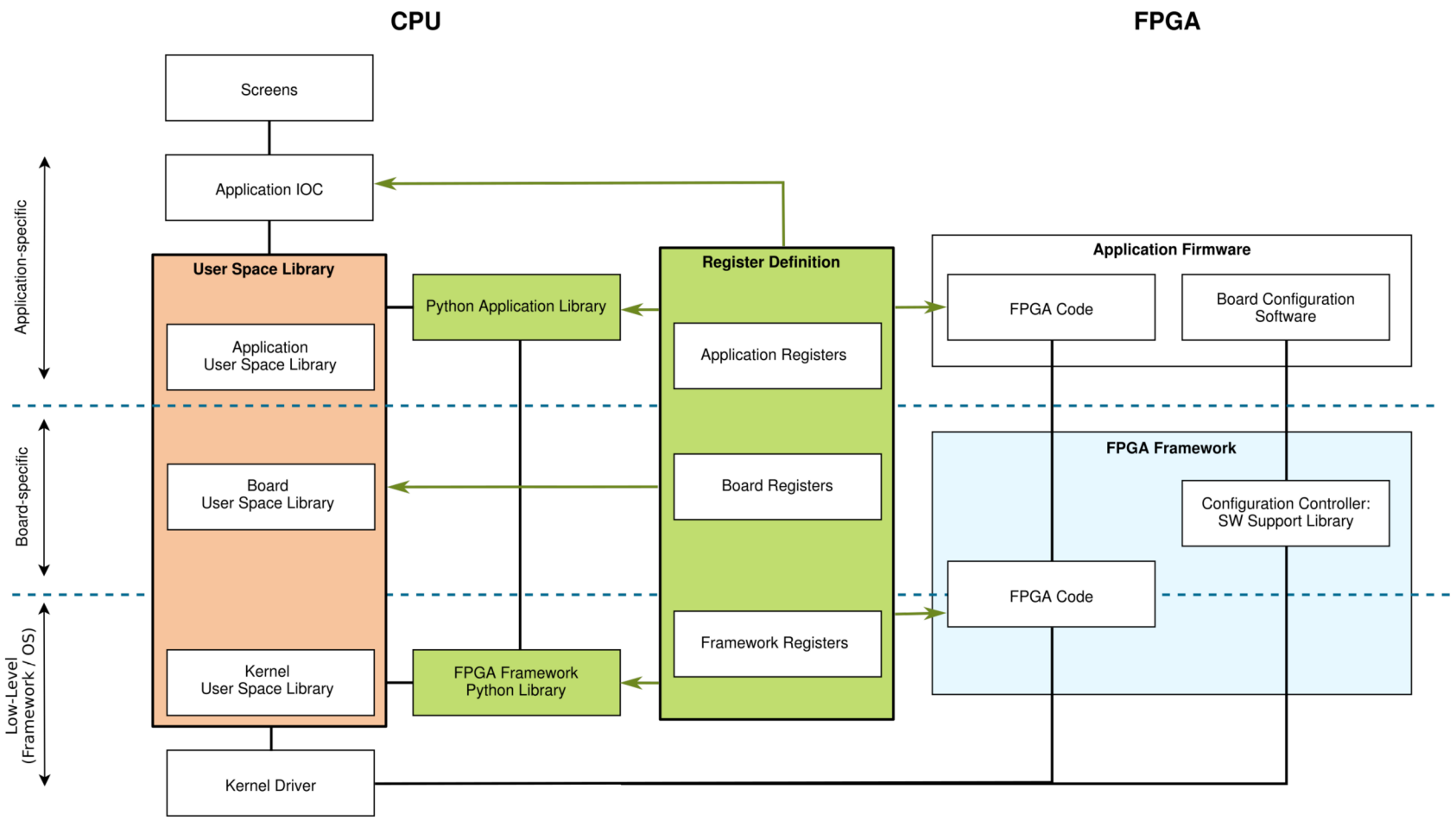


Integration into Control System



Integration into Control System



Python Support

Automated register bank generation

- AXI4-L interface
- Integration in automated workflow

Control System (EPICS)

- C header file generation
- Generation of certain process variables (PVs)

Quick Documentation

Automated on-board testing

- Register access
- Memory testing, DMA speed

Helper scripts

- System setups
- System status checks

Testing of Control System Functions

Prototyping control system scripts

Python Support: Example (1)

address	name	mode	16	0
0x000	firmware version	read-only	MAJOR	MINOR
0x001	GPIO register	read/write		

```
my_registers = essffw.RegisterBank("example_bank", 8, 16)
my_registers.add_register("FW_VERSION", 0x000, "R")
my_registers["FW_VERSION"].add_field("MAJOR", 8, 8)
my_registers["FW_VERSION"].add_field("MINOR", 0, 8)
my_registers.add_register("GPIO", 0x001, "RW")

print(my_registers)

my_registers.generate_code("rtl_code/folder")
```

```
example_bank @ 0x0
  0x000 - FW_VERSION  : 1111111100000000 (0x0000)
    (0) - MINOR       :  8 bit(s) @  0     (0x00) - R
    (1) - MAJOR       :  8 bit(s) @  8     (0x00) - R
  0x001 - GPIO        : 0000000000000000 (0x0000) - RW
```

VHDL
Register Bank

Python Support: Example (2)

- Read registers / fields
- Set/clear bits
- Read memory

```
test_board = essffw.Device()
test_board.add_register_bank(my_registers)
ku_boards = essffw.find_essffw_devices()
test_board.connect(ku_boards[0])

minor = test_board["FW_VERSION"]["MINOR"].read()
major = test_board["FW_VERSION"]["MAJOR"].read()

test_board["GPIO"].clear()
test_board["GPIO"].set_bit(5)

test_board[(0, 100)].read()
```

Conclusions

- Concepts of generic framework held up in practice
- Multiple FPGA applications att ESS are based on the framework
- Python helper classes are very useful for testing

Contact: christian.amstutz@esss.se

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Thank you

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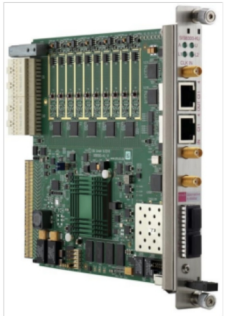
Backup

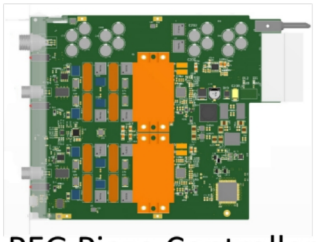
Example LLRF System at the ESS Linear Accelerator

Concurrent Technologies
AM 90x AMC CPU

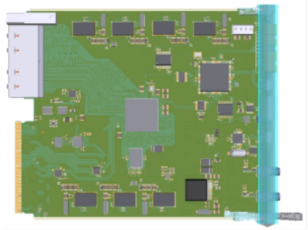
Struck DWC8VM1



Struck SIS8300-KU
(Xilinx Kintex UltraScale)



PEG Piezo Controller

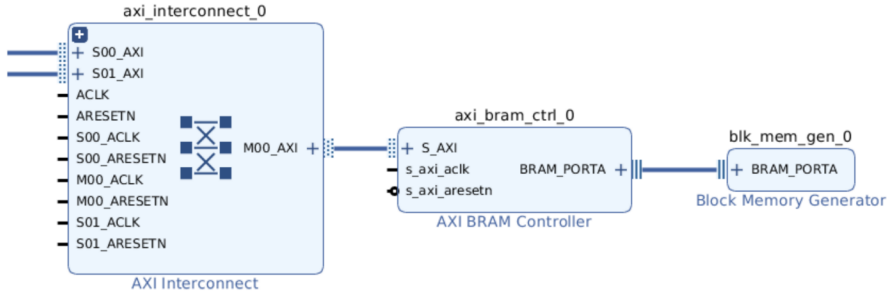


PEG RTM Carrier
(Xilinx Artix-7)

Schroff 12 slot MTCA crate

AXI4 Bus

- Part of the open-standard AMBA bus family from ARM
- On-chip interconnect: High bandwidth / low latency
- Highly configurable:
  - Read-only / read-write
  - Width of data lane
- 3 types:
  - AXI4
  - AXI4-Lite
  - AXI4-Stream
- Official bus in Vivado IP Integrator



One repository contains everything

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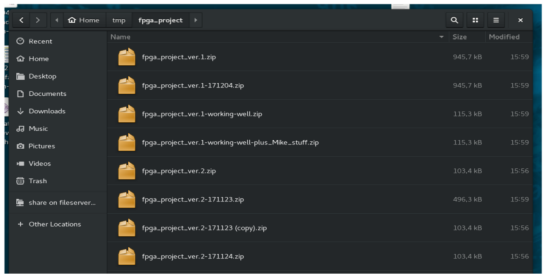
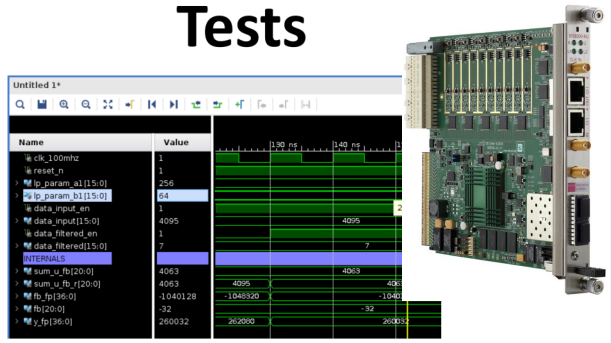
Code



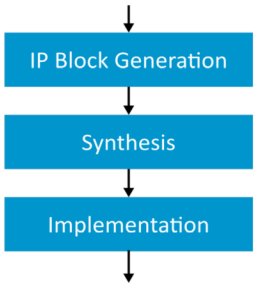
Tests



Atlassian Bitbucket

git

Build Process



Build Environment

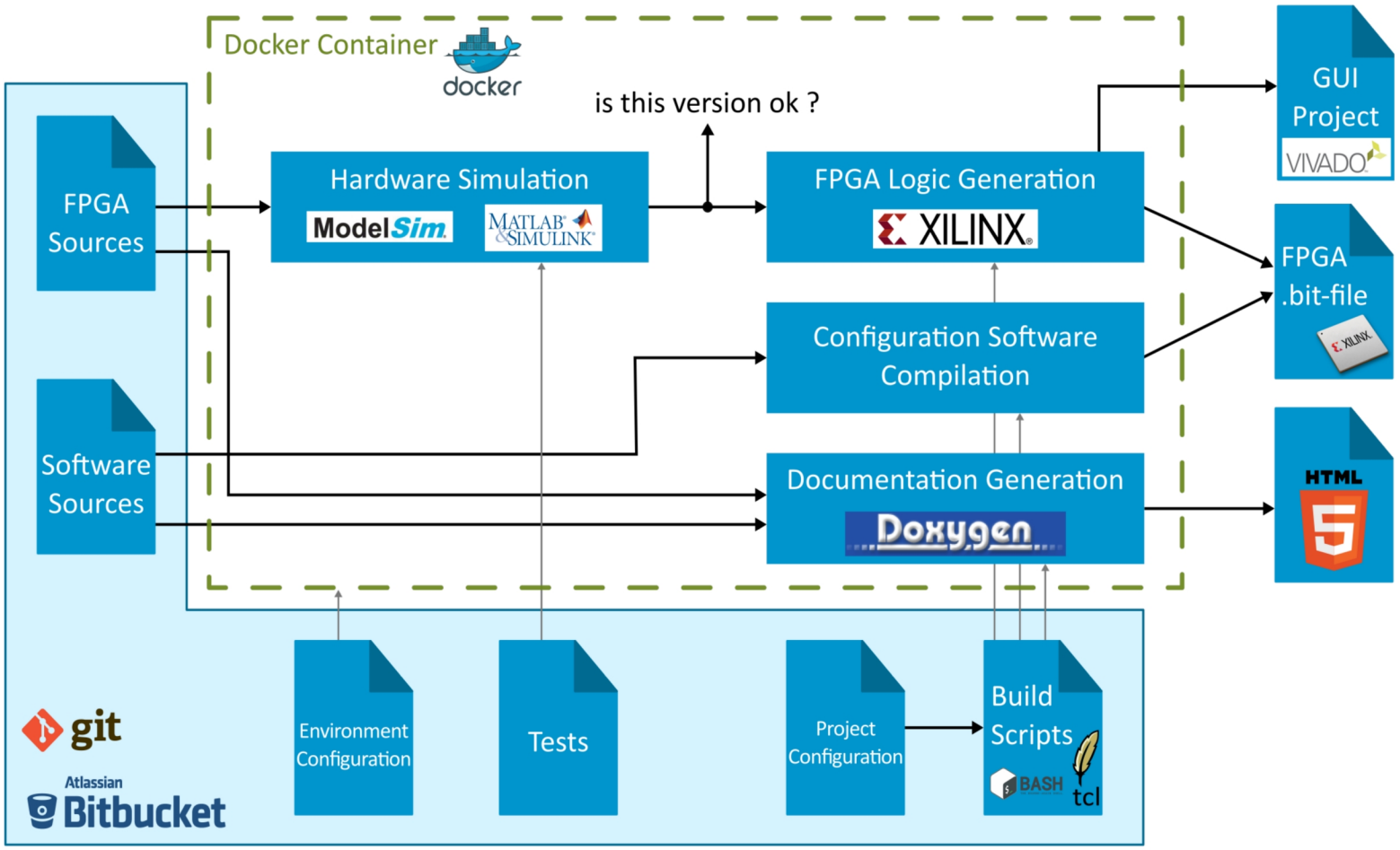
CentOS

ubuntu

VIVADO 2016.4 2017.2

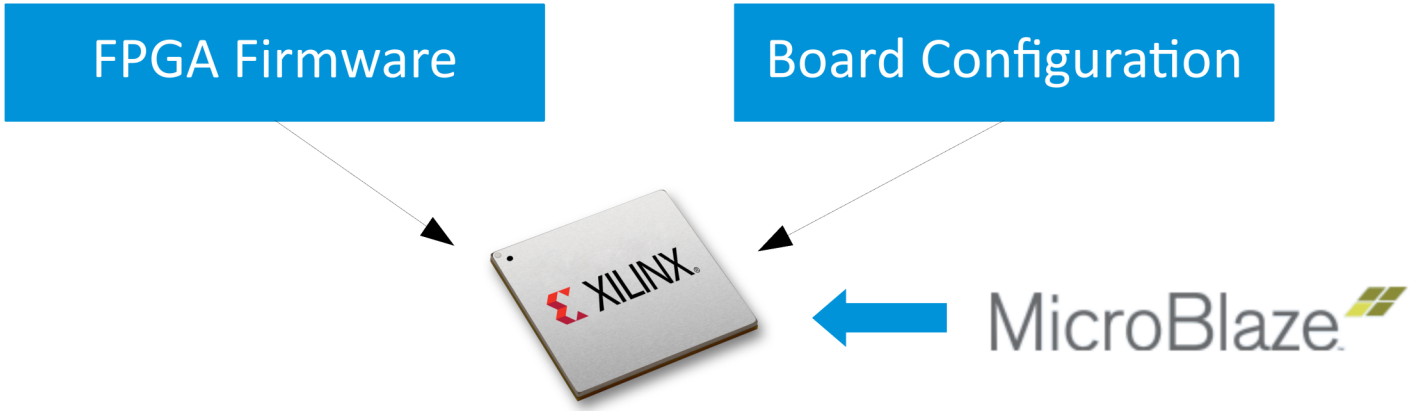
Goal: Usage of the continuous integration system Jenkins.

Automated Design Process



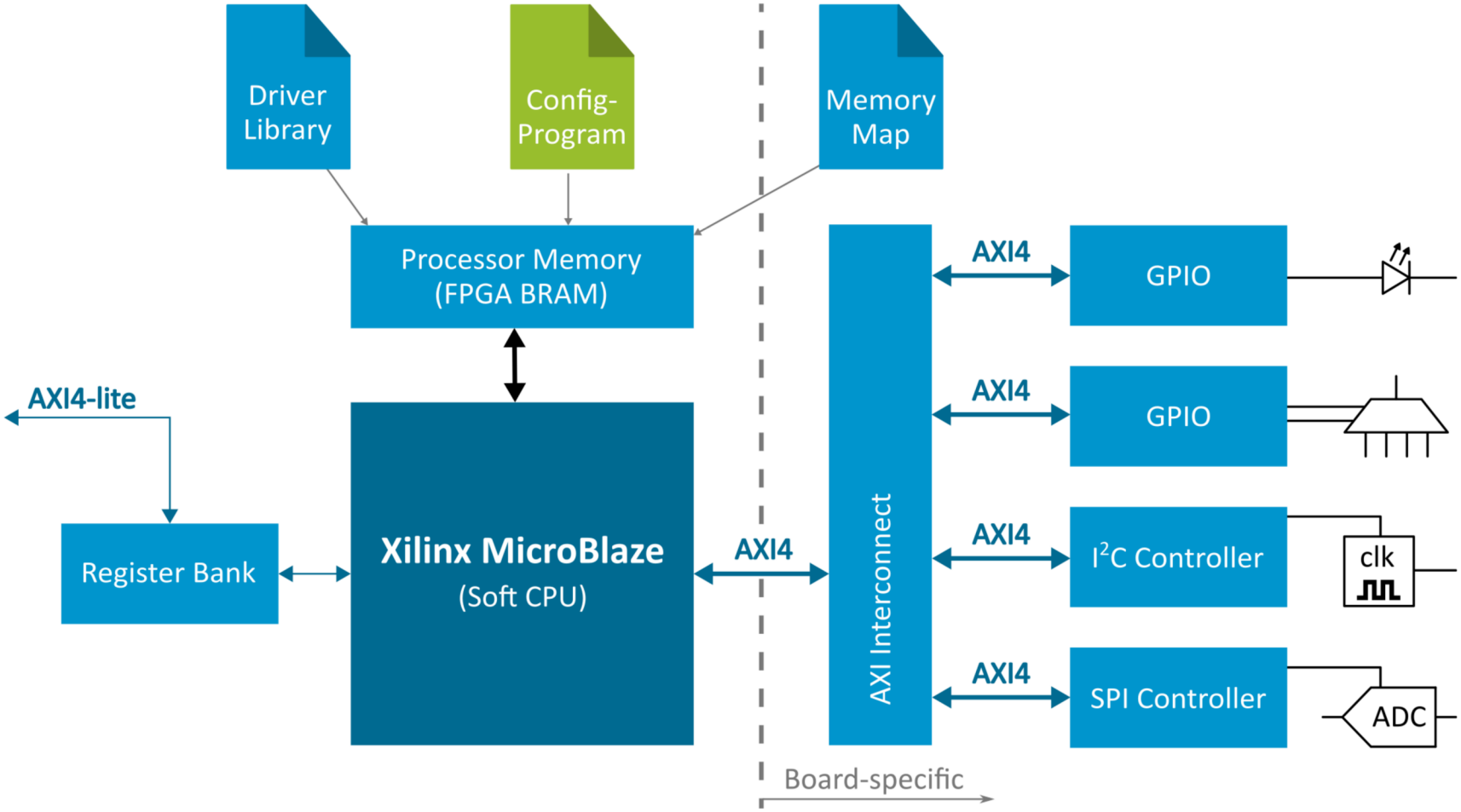
Configuration Controller – Concepts

→ Board Configuration is rather static for one application



- Usage of Xilinx IP blocks for SPI, I2C, GPIO
- Adaptations to the serial protocols (SPI, I2C) made in software
- Separate board configuration from driver

Configuration Controller – Overview



Test Application