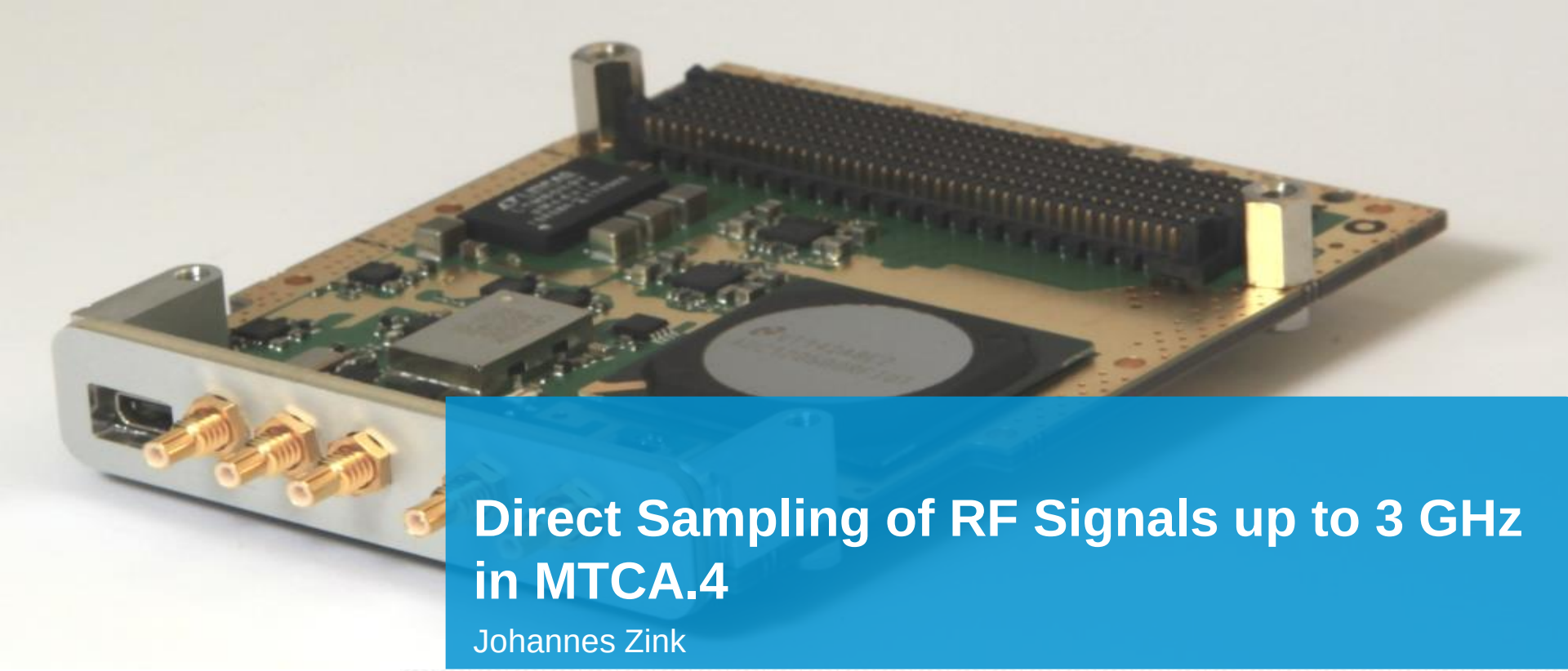


Direct Sampling of RF Signals up to 3 GHz in MTCA.4

Johannes Zink

MicroTCA TECHNOLOGY LAB

DESY.

OUTLINE

1. State of the art - Zone3 Connection in MTCA.4
2. High-frequency diagnostic applications
3. Direct-sampling digitizer boards (FMC/AMC)
4. New Zone3 classification for MTCA.4

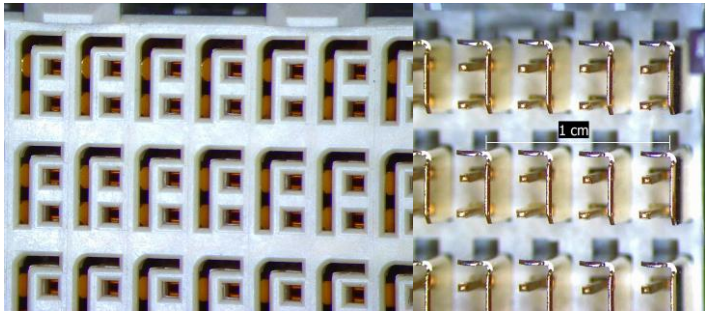
Digitizing of RF Signals in MTCA.4

- high-resolution digitizer (AMC)
- analog front-end (AFE) on RTM side
- down conversion of high frequency signals → Zone3 differential
- Zone3 → sampling on the AMC-board
- IF sampling at 50 MHz

struck innovative systeme

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

Zone3 Differential Connector



- differential pair connections between AMC and RTM board
- digital and analog Zone3 classes
- J30 contains power, management, clock and digital data signals
- J31 contains analog differential inputs and outputs (AMC view)

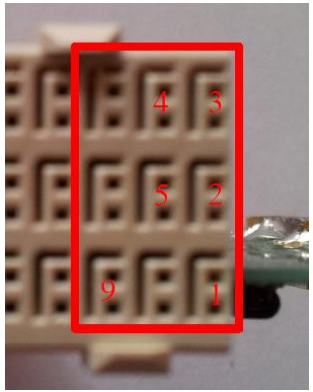
DISADVANTAGE:

- cross talk between differential pairs

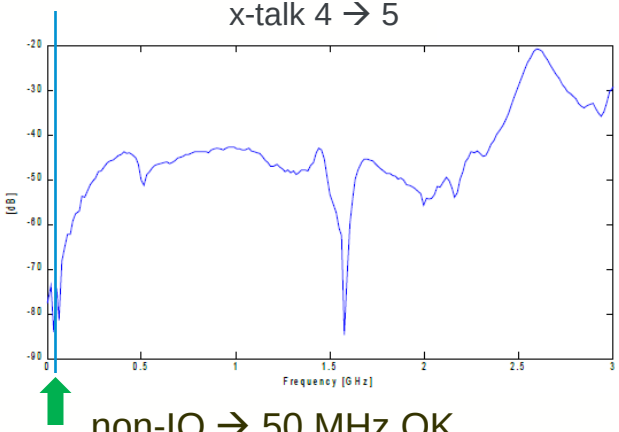
AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A1 / Zone			a	b	c	d	e	f
MTCA 4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	D0+ / SFP-CLK+	D0- / SFP-CLK-	D1+ / SFP-RX+	D1-/SFP-RX-	D2+ / SFP-TX+	D2- / SFP-TX-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		6	D9+ / AMC_TCLK+	D9-/ AMC_TCLK-	D10+ / OUT0+	D10- / OUT0-	D11+ / OUT1+	D11- / OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
		9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
		2	CH8_TF+	CH8_TF-	gnd	gnd	CH8_PA+	CH8_PA-
		3	CH7_PA+	CH7_PA-	DAC1+	DAC1-	CH7_TF+	CH7_TF-
		4	CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
		5	CH5_PA+	CH5_PA-	DAC2+	DAC2-	CH5_TF+	CH5_TF-
		6	CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
		7	CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
		8	CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
		9	CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
		10	CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

Table 1 : Pin assignment of Class A1, AMC side view



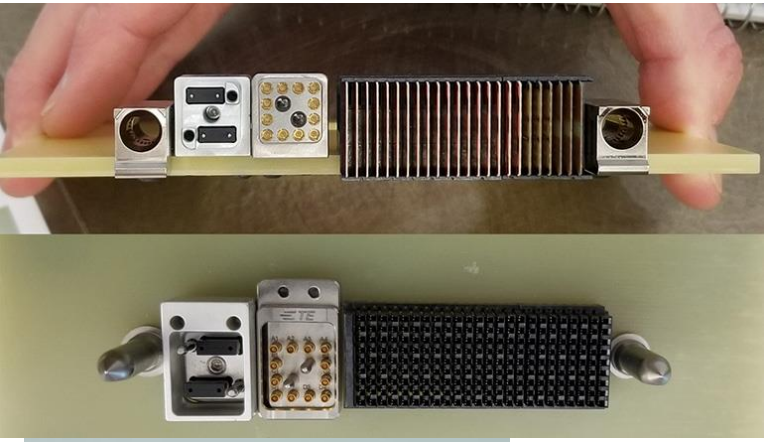
x-talk 4 → 5

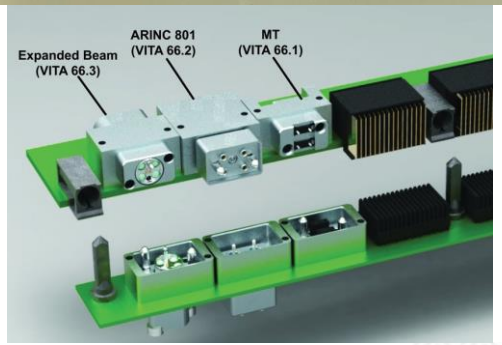


non-IQ → 50 MHz OK

Solutions

VPX™





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ERmet zeroXT

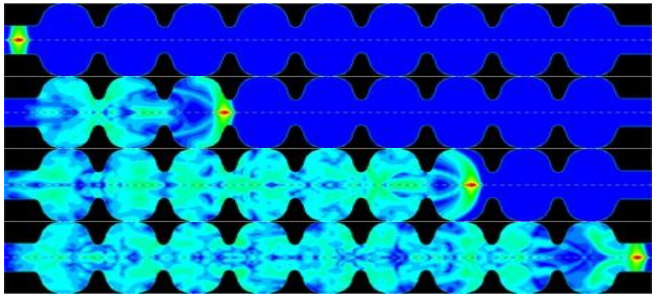
ERNI © ERNI

MTCA.4 Zone3

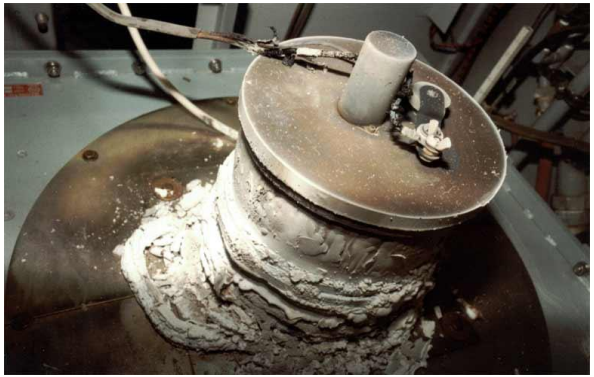
?

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

High Frequency Diagnostic Applications



bunch passing a cavity, H.Padamsee



Klystron melt-down after arc, TV transmitter

High-Order Modes

- electron bunch excites HOM in cavity, signals from HOM couplers can provide informations about:
- beam position, beam charge, cavity alignment
  - „Electronics for High-Order Modes Detection“, Uros Mavric et al.

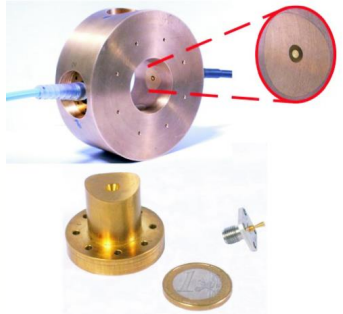
Klystron Lifetime Management

- detection of dangerous Klystron states:
- gun arcs, loss of beam, loss of RF signal
  - Model Based Fast Protection System For High Power RF Tube Amplifiers Used At European XFEL Accelerator, Lukasz Butkowski

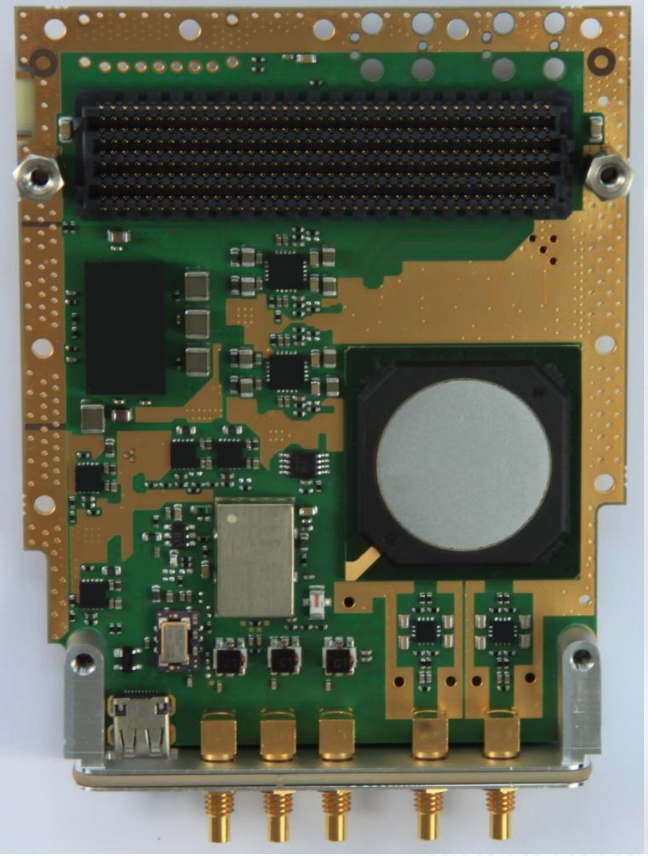
RF based Bunch Arrival Time Monitor

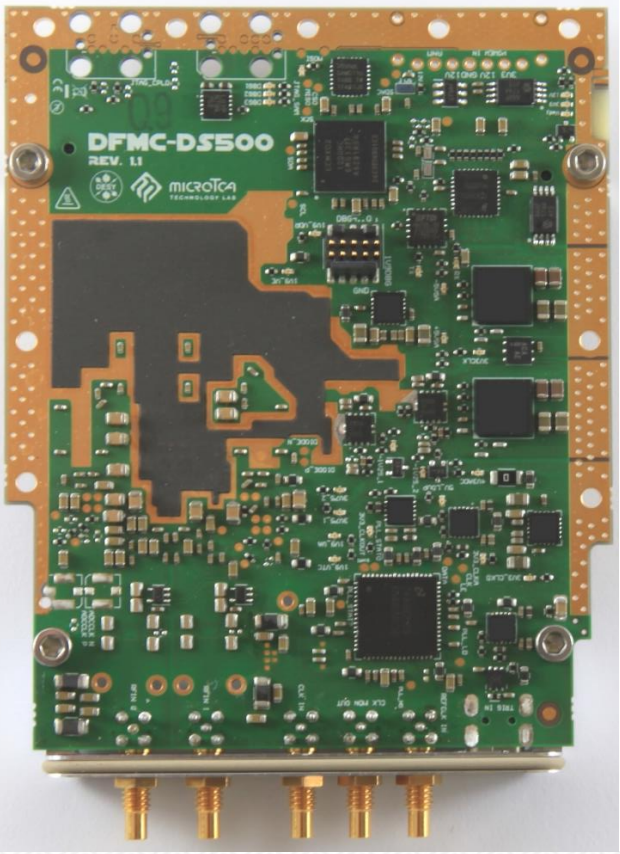
- direct sampling of pick-up signals
- reduction of bandwidth from 40 GHz to 2.4 GHz
- roughly estimate bunch arrival time
- adjust electro-optical BAM

BAM beam pick-ups



DFMC-DS800

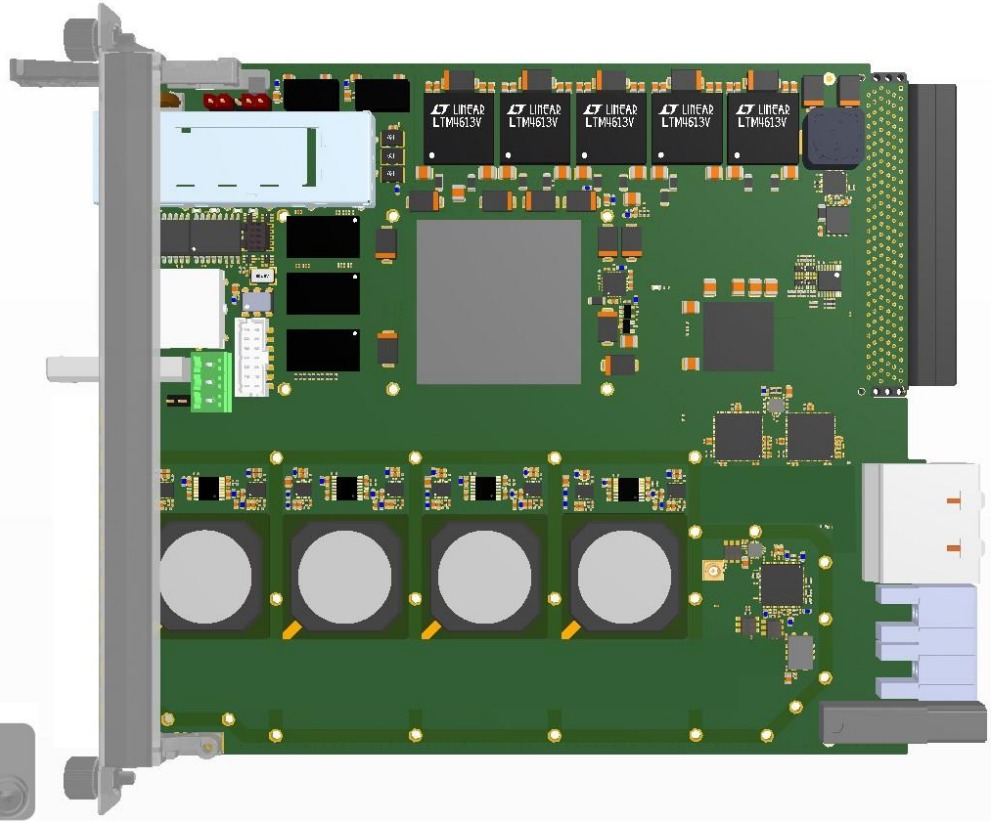




- single width FMC according to ANSI/VITA 57.1 standard
- 8.5 mm stacking height
- 12-Bit, 800 MSP/s Dual Ch., 1.6 GSP/s Single Ch.
- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier LS bandwidth: 4.8 GHz

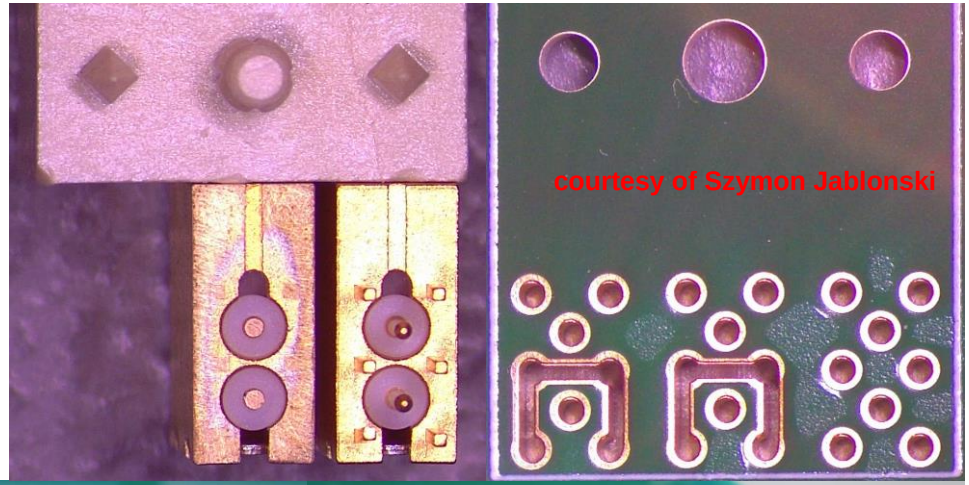
DAMC-DS800

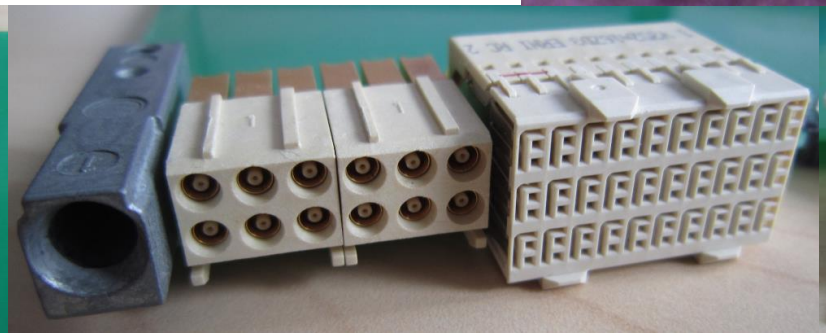
- 4x 12-Bit, 800 MSP/s Dual Ch., 1.6 GSP/s Single Ch. ADCs
- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier LS bandwidth: 4.8 GHz
- XCZU7EG F1517 ZynQ MPSoC Dual/Quad-Core ARM Cortex-A53
- Mali-400 Based GPU
- Signal feed in via Zone3 and Front Panel
- Quad SFP, COAX IO, HARLINK LVDS at FP
- First Batch Q3/2019

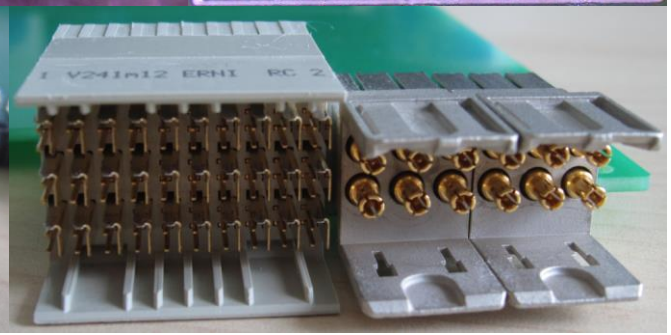


New Zone3 Class - Preliminary

- new analog Zone3 class will be introduced
- single-ended coaxial connectors
- signals up to 6 GHz can be transmitted from / to RTM side
- THT mounting or cable feed trough possible

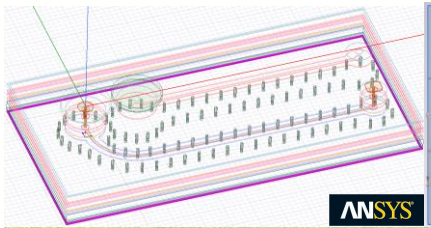


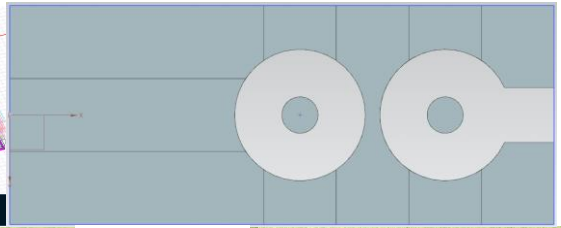


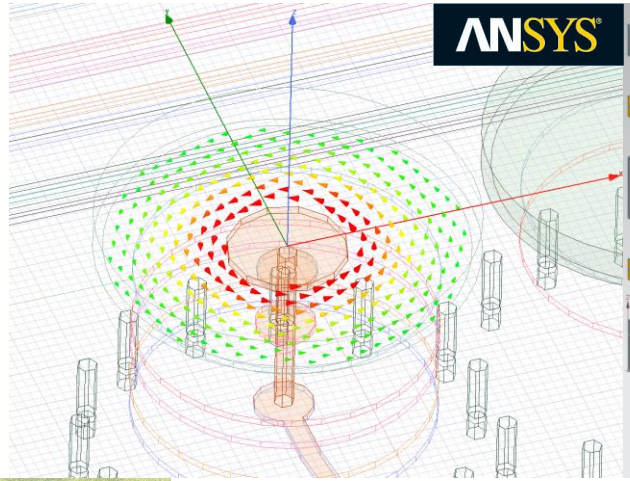


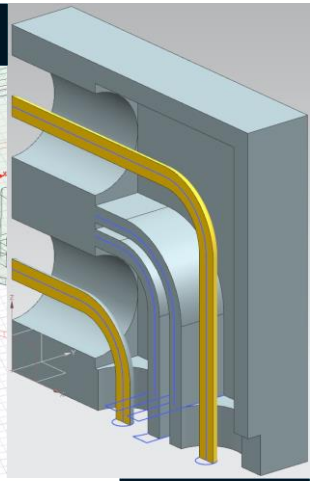
New Zone3 Class - Preliminary

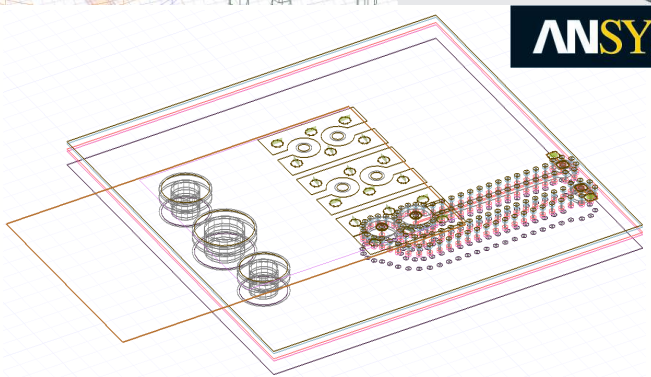
- improved isolation between conductors in one insert
- isolation of -70 dB up to 3 GHz
- connector itself is not an issue anymore
- but footprint optimization is needed











special thanks to Stanislav Chystiakov

Images used courtesy of ANSYS, Inc.

Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Analog signal transmission zone:
- 12 channel DC-coupled single-ended IO (input) signals

Digital clock signal transmission zone:
- 2 AC-coupled differential inputs for low-jitter clock signals
- 1 LVDS output clock signal

User signal transmission zone:
- 6 LVDS inputs / outputs for user-configuration
- 3 LVDS outputs with fixed output direction
- Optional dual high-speed link

Zone shielding:
- Supports ground shielding between zones

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- Multi-channel analog-to-digital converters
- Multi-channel signal shaper
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

GENERAL DESCRIPTION

This Class A3.1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring up to 12 analog signals over the Zone 3 connector. This analog class is designed for a three row ADF and two six pin coaxial Zone 3 connectors. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class A3.1 pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A3.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
User-configuration		4	D5+	D5-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		8	AMC_CLK0+	AMC_CLK0-	DAC3+	DAC3-	DAC2+	DAC2-
		9	RTM_CLK0+	RTM_CLK0-	DAC1+	DAC1-	DAC0+	DAC0-
		10	RTM_CLK1+	RTM_CLK1-	CH13+	CH13-	CH12+	CH12-
			1A		1B		1C	
Analog signals	J31	A	CH11		CH10		CH9	
		B	CH8		CH7		CH6	
	J32	A	CH5		CH4		CH3	
		B	CH2		CH1		CH0	

Table 1 : Pin assignment of Class A3.1, AMC side view

- Class A3.1
- J30 like A1 and A2 classes
- J31 / J32 Up to 12 single-ended RF signals

OUTLOOK

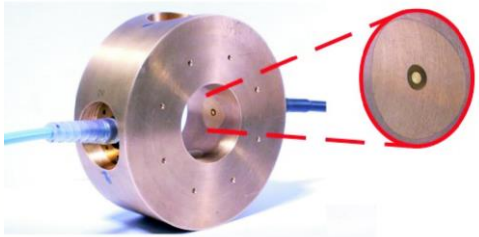
- finishing simulation and research
- waiting for prototypes of improved CoaxiPack2
- finish Class A3.1 specification early next year

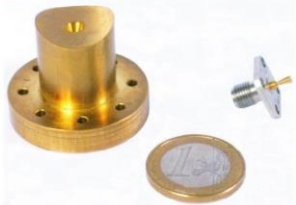
ACKNOWLEDGEMENTS

M. Fenner, S. Jablonski, F. Ludwig, U.Mavric

Thank you for your attention.

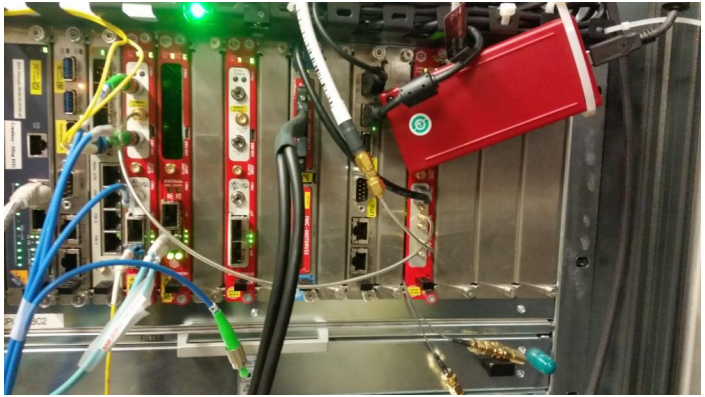
Diagnostic Applications

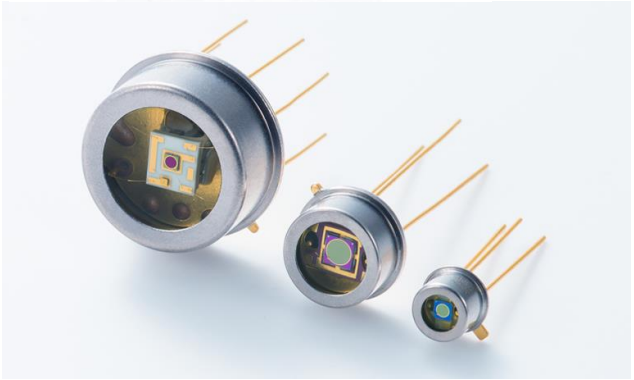




Bunch Arrival Time Monitor

- direct sampling of pick-up signals
- reduction of bandwidth from 40 GHz to 2.4 GHz
- roughly estimate bunch arrival time
- adjust electro-optical BAM





Photodiode / PSD

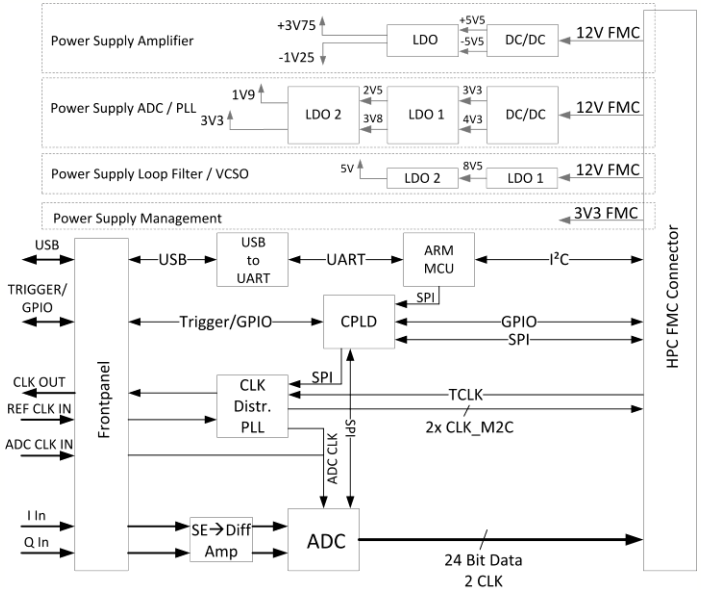
- fast photo diode and PSD readout
- beam position measurments
- light intensity measurements

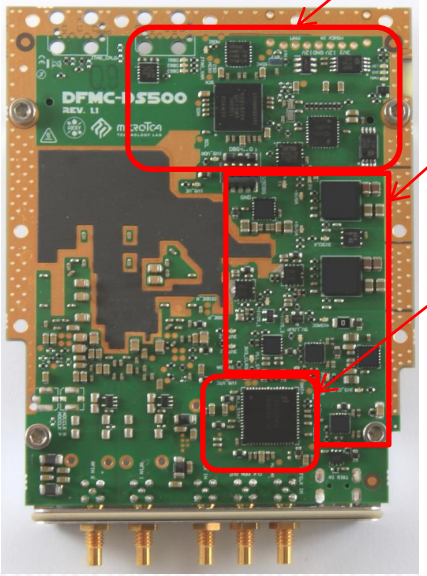
© HAMAMATSU

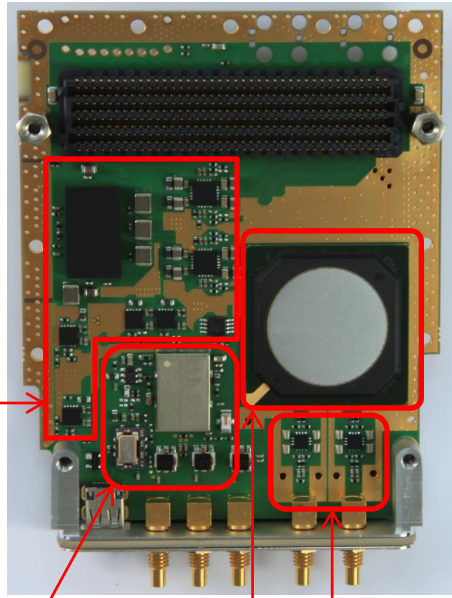
© HAMAMATSU

DFMC-DS800

- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier LS bandwidth: 4.8 GHz
- no anti-aliasing filter present
- variants with up to 3.2 GSP/s







Management

Power Supply

PLL

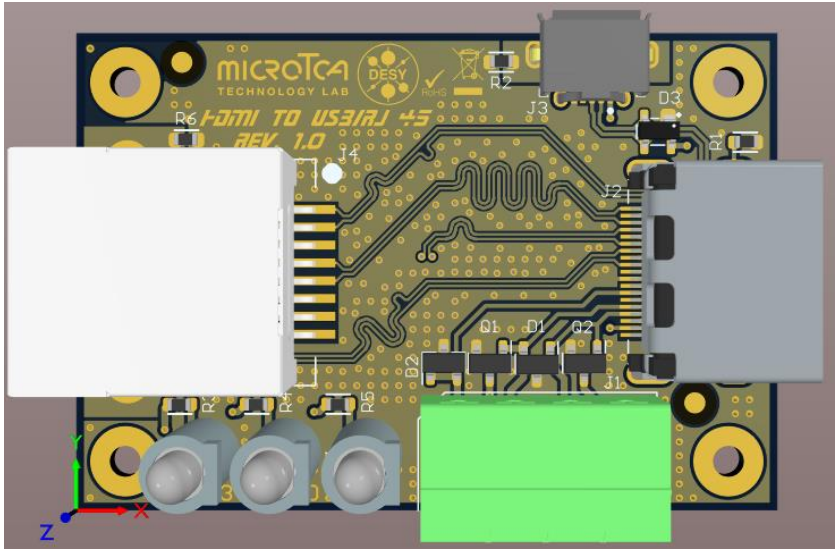
Oscillators/Loop Filters

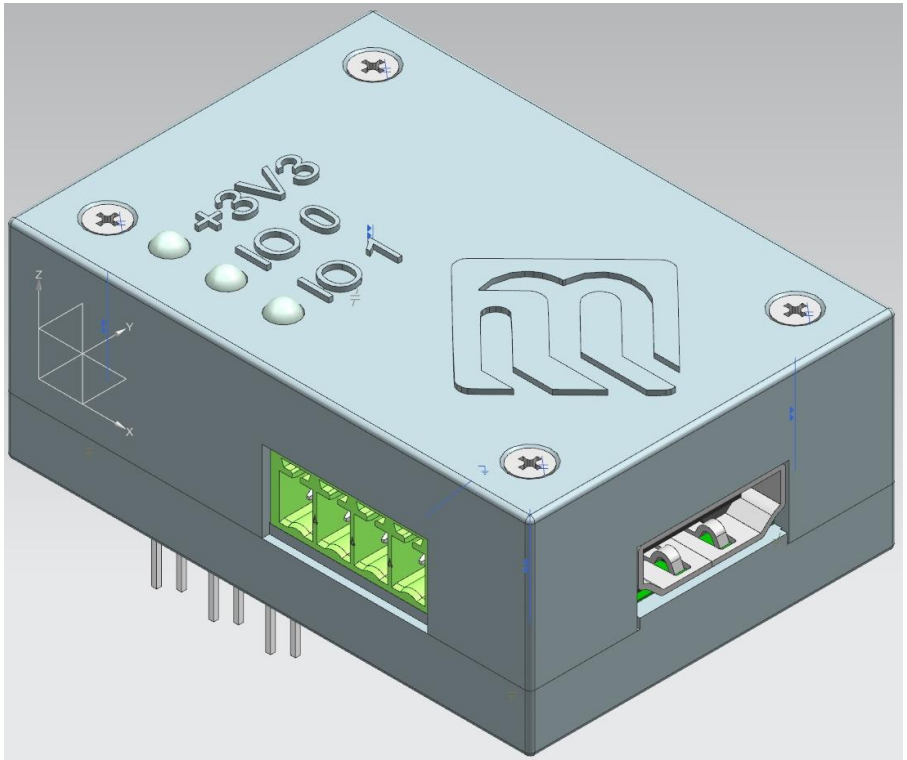
ADC

SE → DIFF Amplifiers

Break-Out board

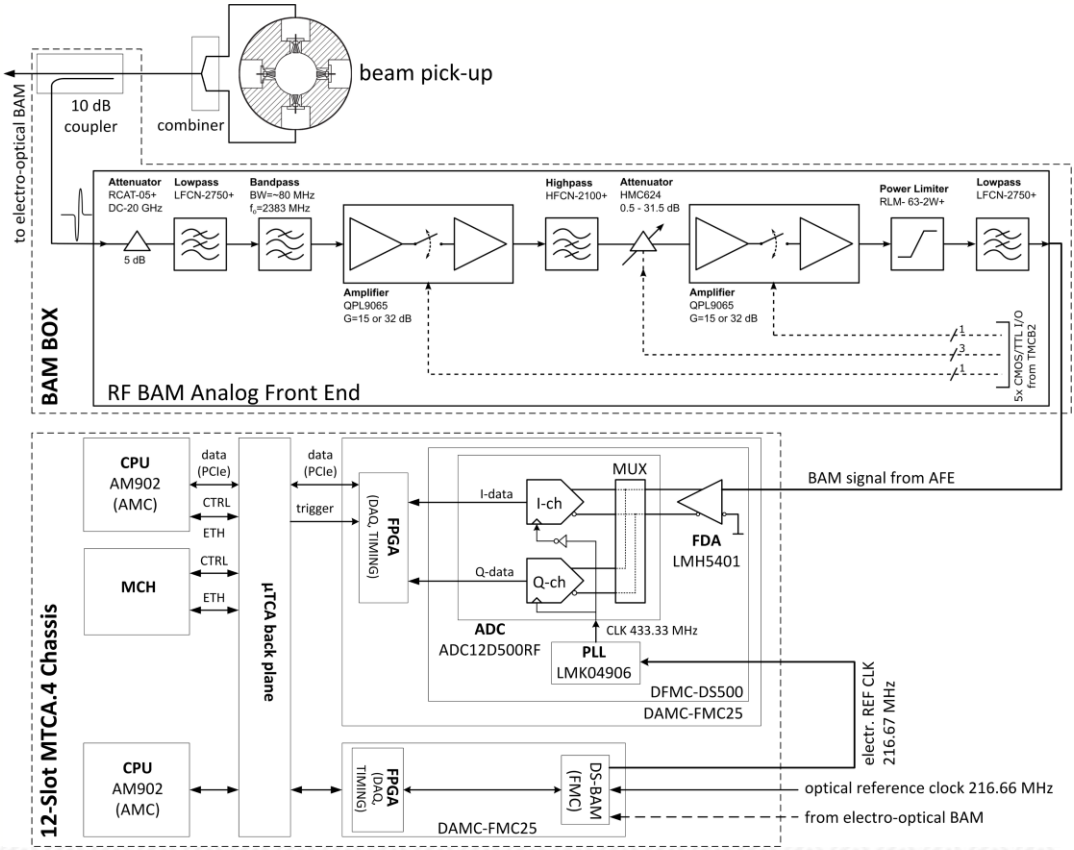
- 4 LVDS (differential) pairs → can act as input or output (trigger/control signals, 100 MHz)
- 2 single-ended bits input / ouput
- serial interface (debugging and testing)



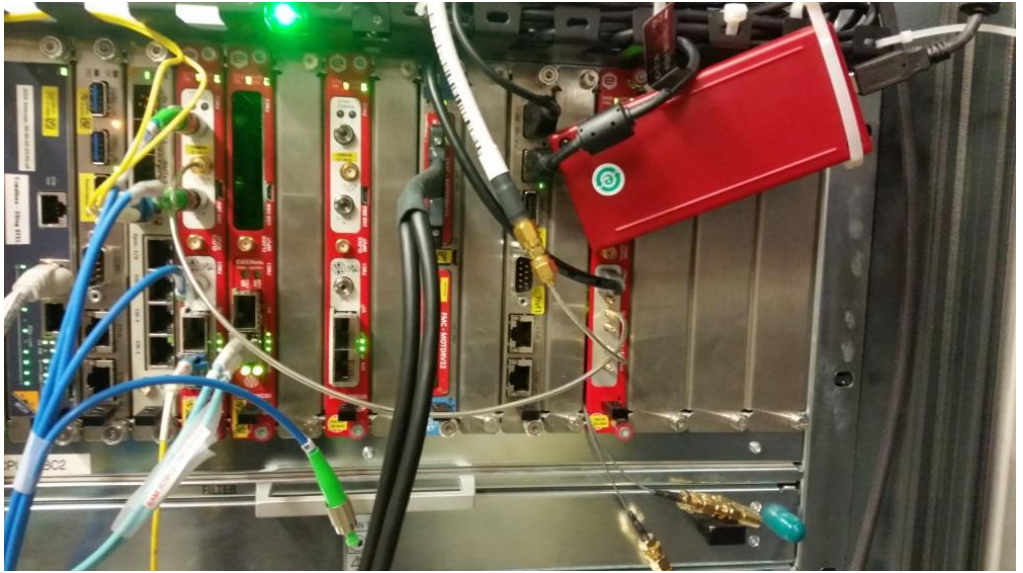


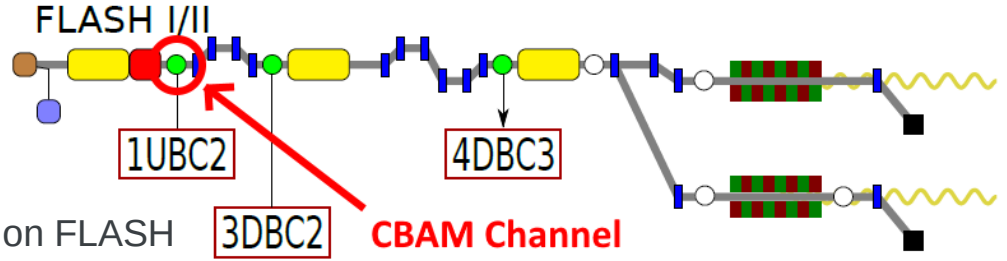
Coarse BAM Channel

- coarse BAM Channel planned in FLASH
- coarse BAM channel in addition to electro-optical BAM [1,2] → automatically adjust optical delay lines
- uses same combined high-bandwidth pick up [3] signals (40 GHz)
- analog front end bandpass filters the pick up signal
- bunch charges can vary from 20 pC up to 1 nC, which requires a dynamic range of about 34 dB
- sampling (DFMC-DS500/DAMC-FMC25) and processing in MTCA.4 crate



CBAM Channel in FLASH

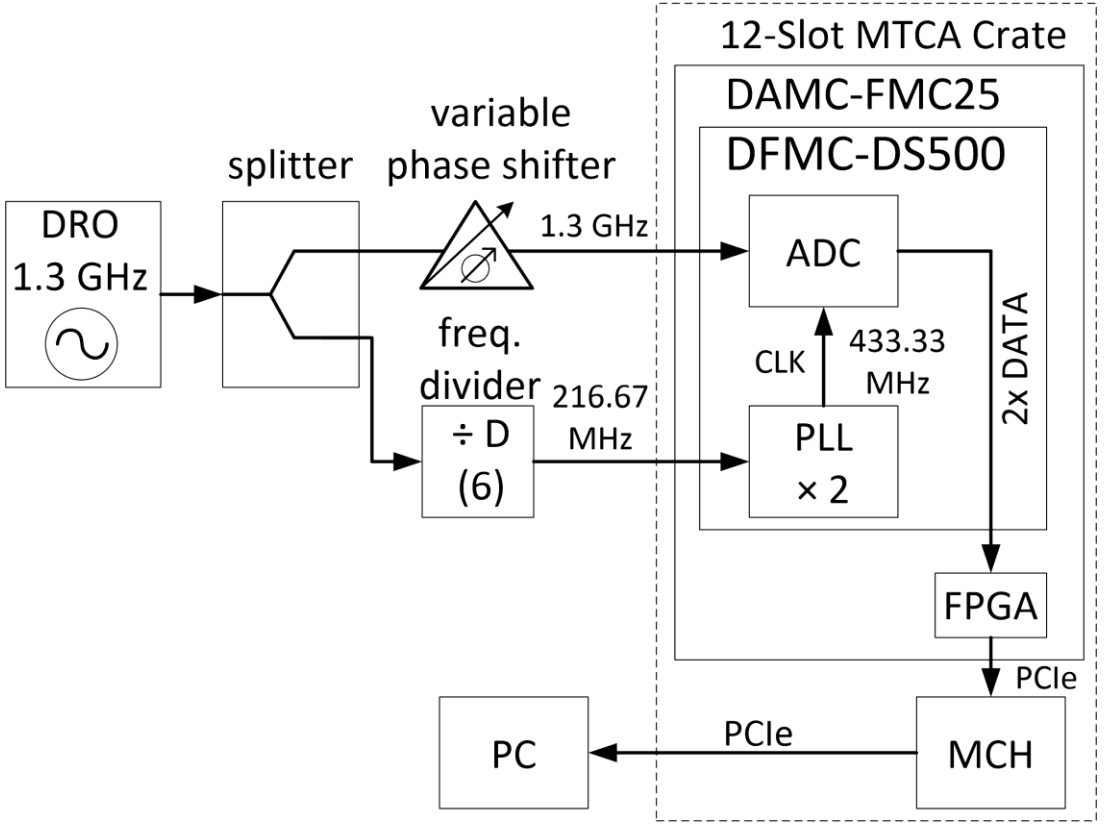




MOOB03, IBIC 2018, N. Baboi et al. for more details on FLASH

CBAM DS500 Test Setup

- complex high-bandwidth pick up signal
- testing ADC performance under ideal conditions with reduced signal bandwidth
- undersampling 1.3 GHz carrier with phase synchronous ADC clock → produces DC signal
- timing error converts into amplitude error
- roughly estimate the timing accuracy



Results

- recorded 1.6M samples
- fitting normal distribution with:

  μ = -2.93117e-21s

  σ = 726.36 fs

- timing error (p2p): 7 ps
- timing error (rms): 726 fs

- results are not outstanding but also not bad
- meet the requirements of ~1 ps