# The Digital BPM development for HEPS project in IHEP

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On behalf of Beam Instrumentation Group of IHEP

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# Outline

1. Why we need to build the digital BPM electronics
2. The BPM requirement of HEPS project
3. Digital BPM pre-research in HEPS-TF project
4. Summary and Acknowledgement

# 1. Why we need to build the digital BPM electronics

1，Beam orbit stability is key parameter of modern light sources, it can affect performances of accelerator and synchrotron light beam stations.

2，Beam users always hope beam orbit changes within 5% to 10% of beam size. For HEPS, its typical beam size is 3μm, so we need to control beam orbit stability within 0.3μm, so the resolution of beam position measurement is need to meet the requirement of 0.1μm.

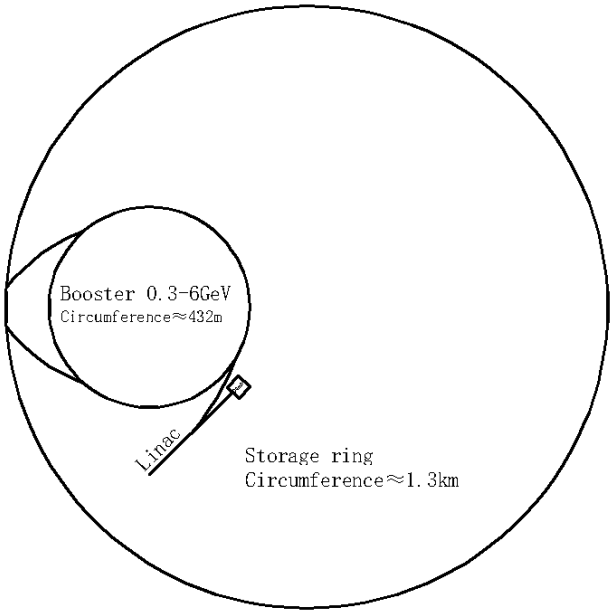
3，Commercial product is good as the beam position measurement, but the price is also “good”, and its original code is not open to users, so further development based on machine requirement and study to them is impossible.

4，Home-made electronics can develop technologies and reduce the cost.

# 2. The BPM requirement of HEPS project

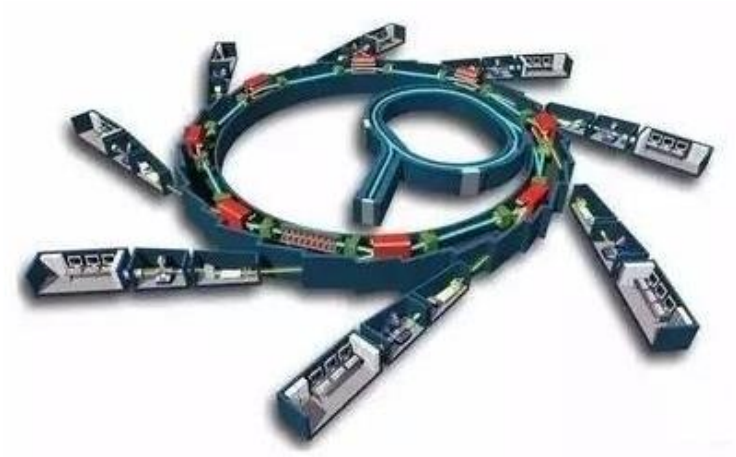
# Brief introduction to the HEPS project

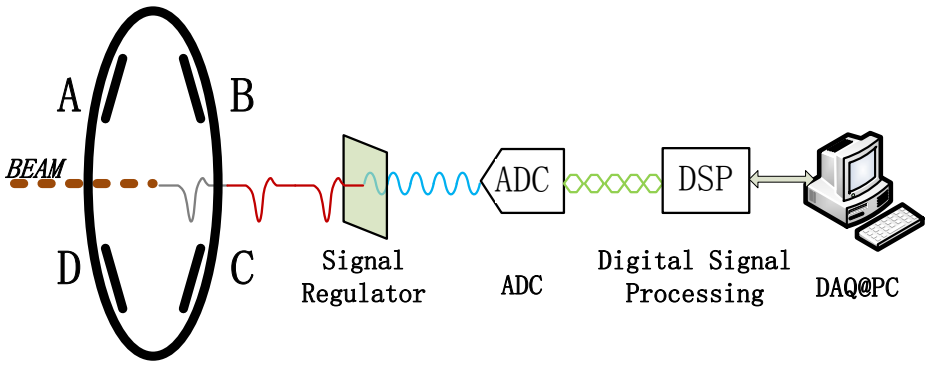
- The **High Energy Photon Source (HEPS)** is designed as an ultra-low emittance ring-based synchrotron radiation light ;
- About fourteen beamlines will be constructed in Phase I of the project;
  - Storage ring circumference: 1296m，48*7BA
  - Energy: 6GeV
  - Emittance<60pm.rad
  - Current: >200mA
  - Construction:2019-2025




Schematic of HEPS Complex

# The Digital BPM requirement of HEPS project






## ■ HEPS BPM quantities

| | BPM Quantities |
|---|---|
| Linac | 7 |
| Transfer Line | 3*10=30 |
| Booster | 80 |
| Storage Ring | 48*12=576 |
| SUM | 693 |

## ■ Storage ring BPM Parameters

| | DBPM@HEPS |
|---|---|
| Turn by Turn Data | 1μm @220kHz |
| FA data | 0.3μm @22KHz |
| COD data | 0.1μm @10Hz |

# 3. Digital BPM pre-research in HEPS-TF(Test Facility) project

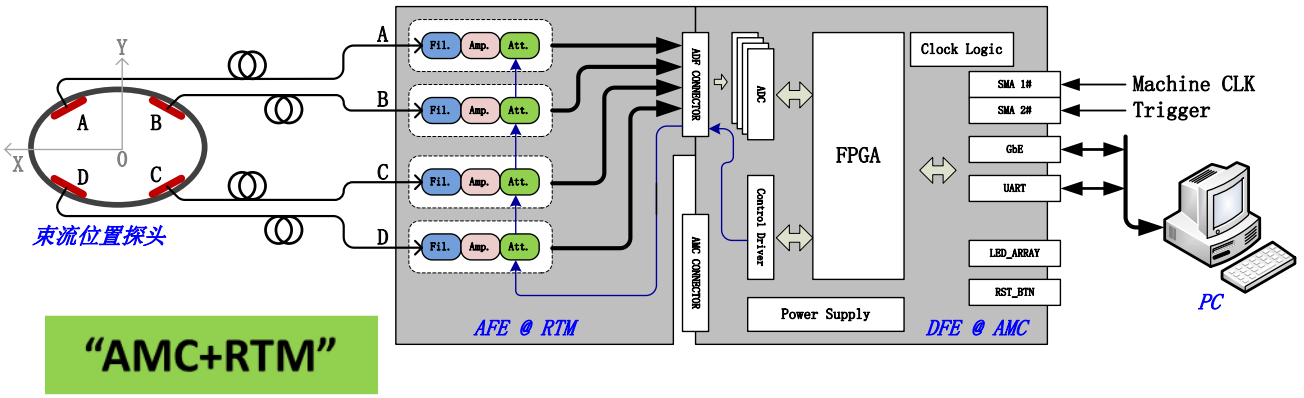
- System structure
- Hardware design
- Algorithm of Firmware
- Software design
- Digital BPM testing

# 3.1 System structure

- For the HEPS will have been built several years later, so we develop the DPBM prototype with BEPCII parameters, and DBPM system is tested in BEPCII. And main work include 3 parts:

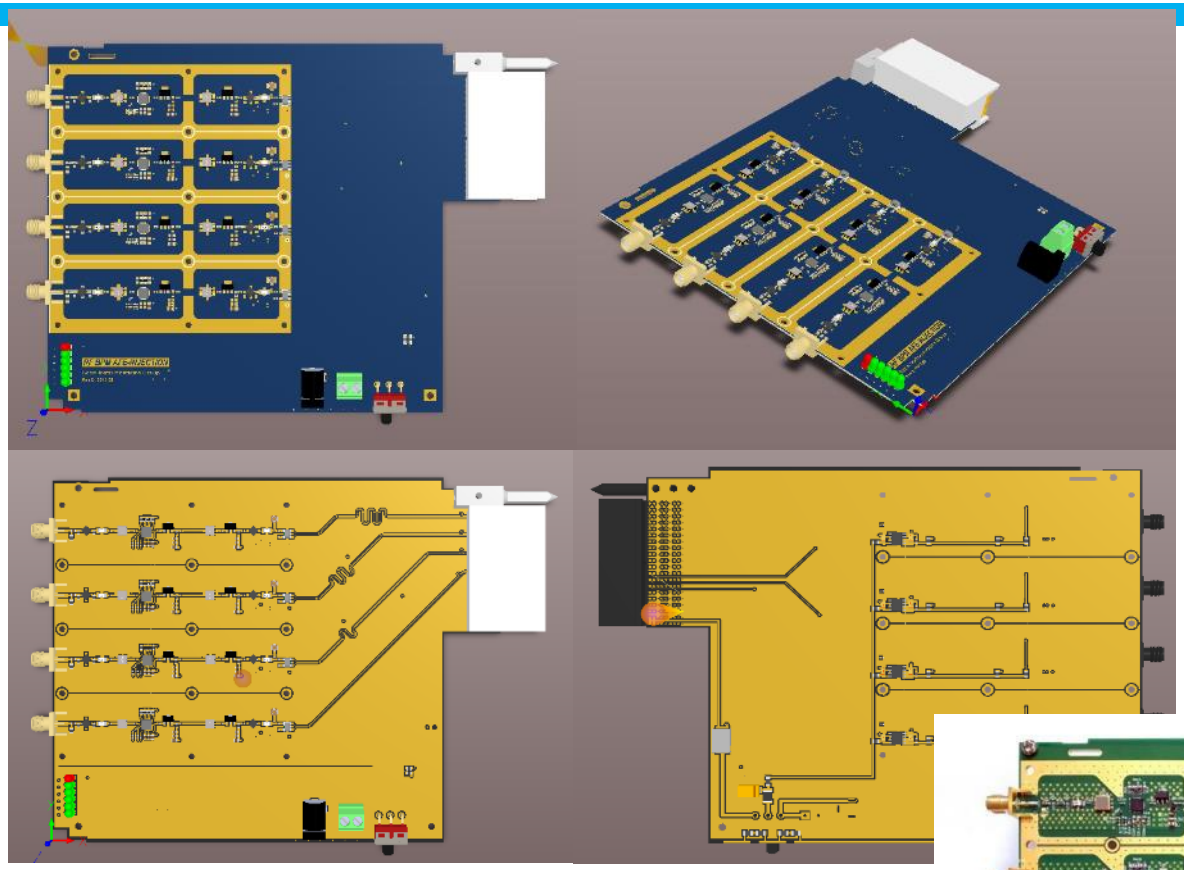
  - HW design
  - FW design
  - SW design

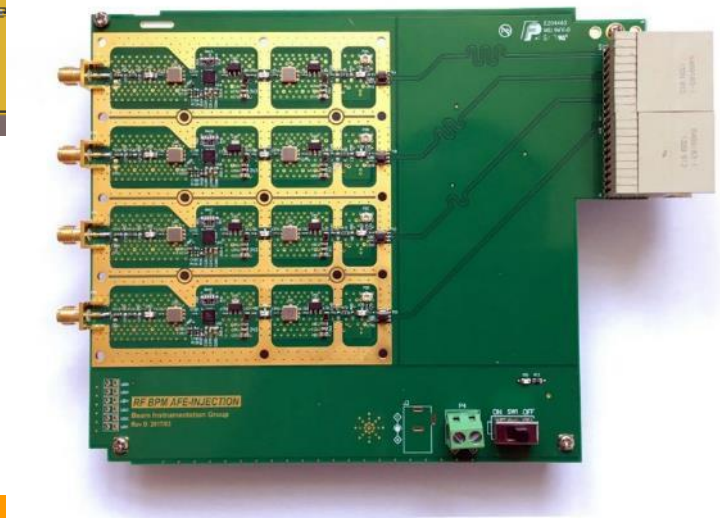
Stand-Alone




"AMC+RTM"

# RTM Module design(by Yaoyao Du)

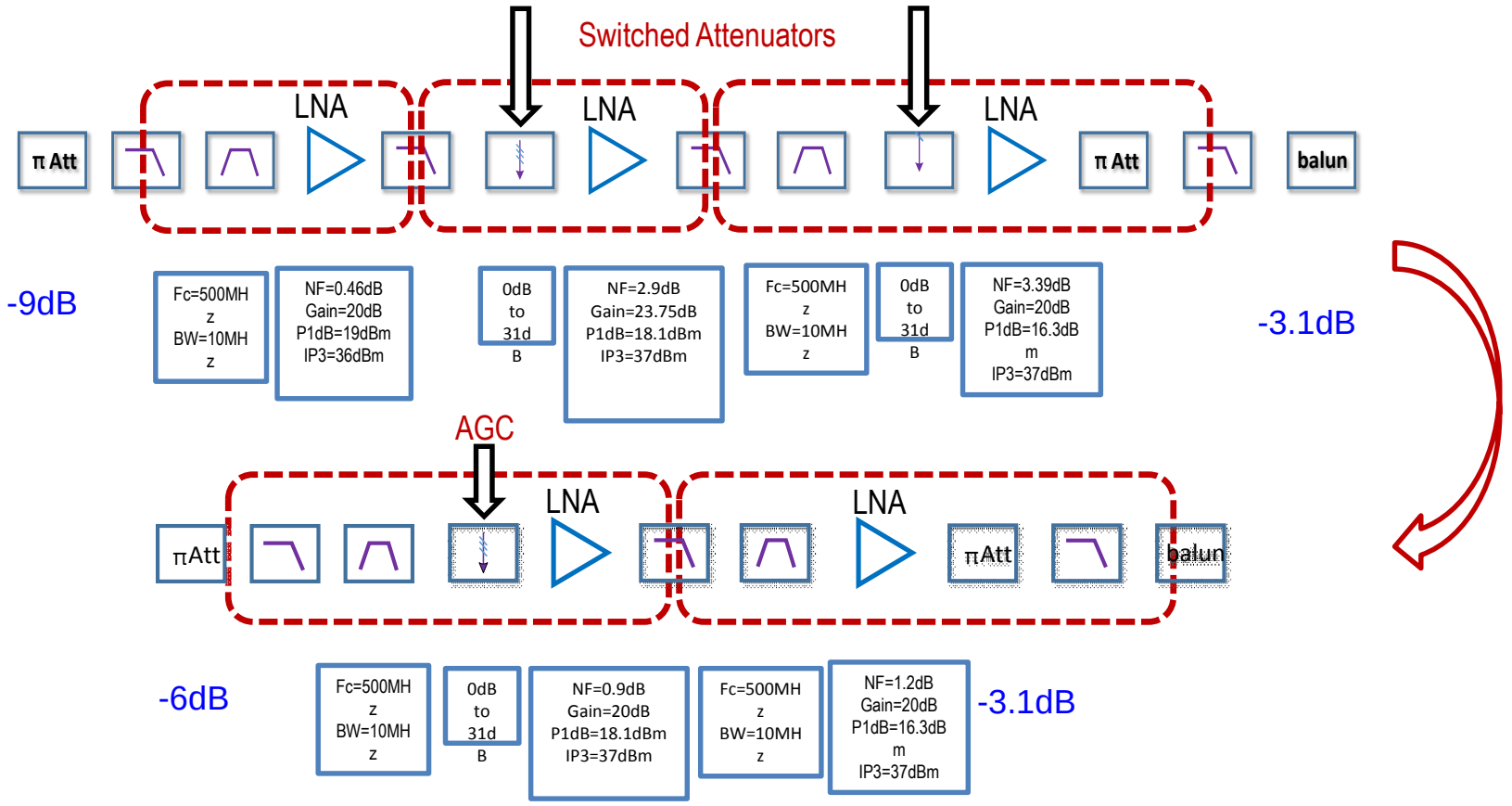




Design objective:

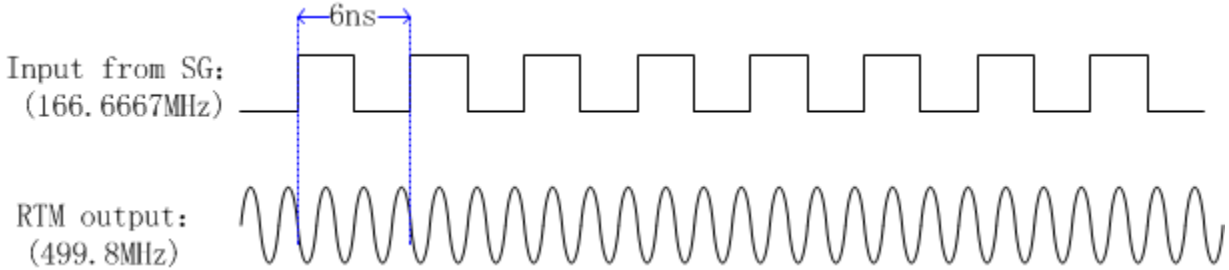
- ✓ Low Noise design
- ✓ Low power consumption

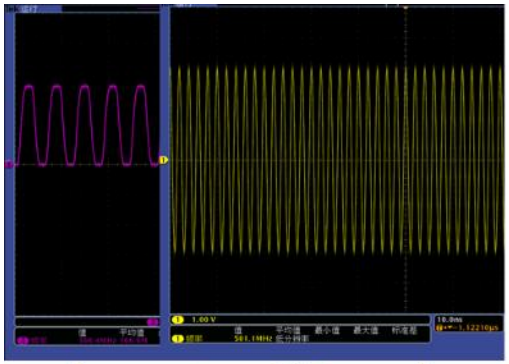
# DBPM_RTM function block

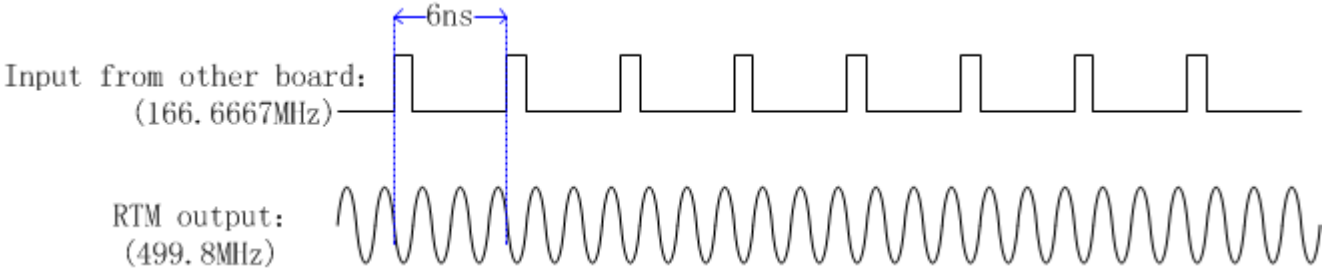



1、Two LNAs are enough
2、The place of Attenuator is designed carefully
3、Attention to the Impedance matching & Noise

# DBPM.RTM ADC clock commissioning






# DBPM.RTM S-Parameter Characterization


Receiver S-Parameter Characterization


S21-Parameter Characterization

The performance of band pass filter is good!

# DBPM.RTM Channel to Channel Isolation


**A→B**

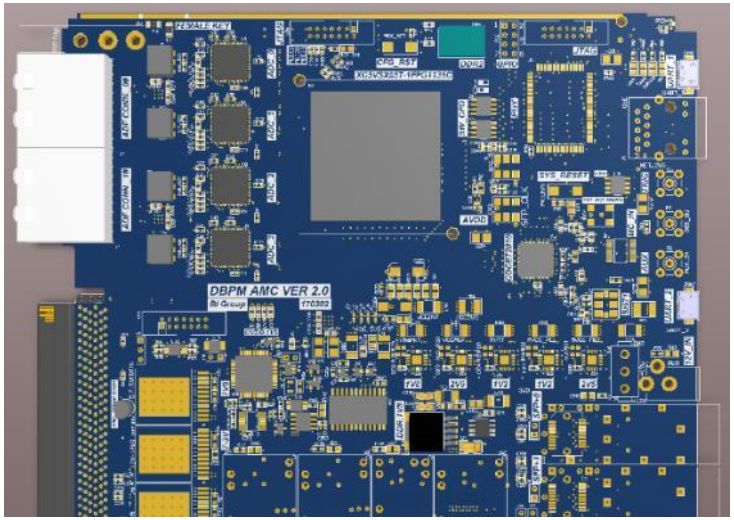
*6.5dBm→-78.8dBm*

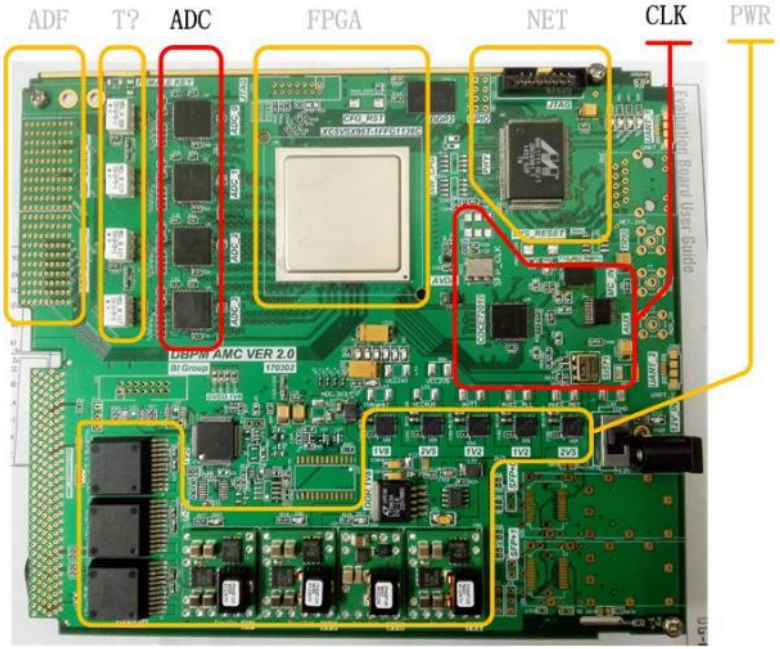

**B→A**

*6.5dBm→-77.47dBm*

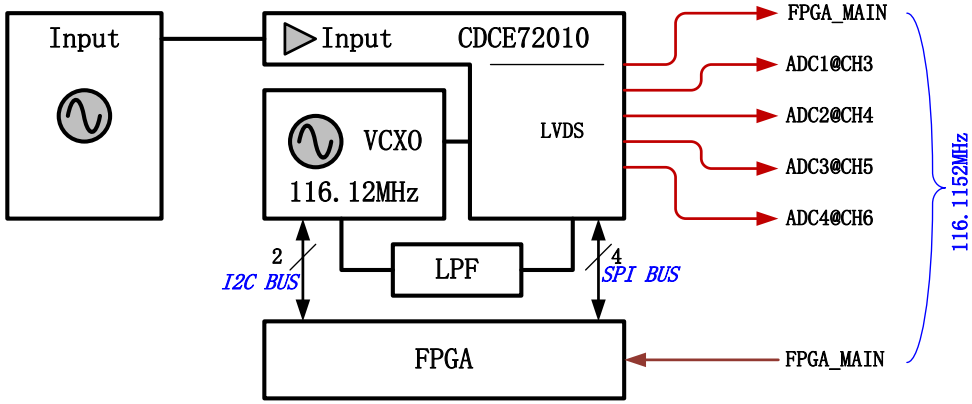
# AMC Hardware design(by Shujun Wei)

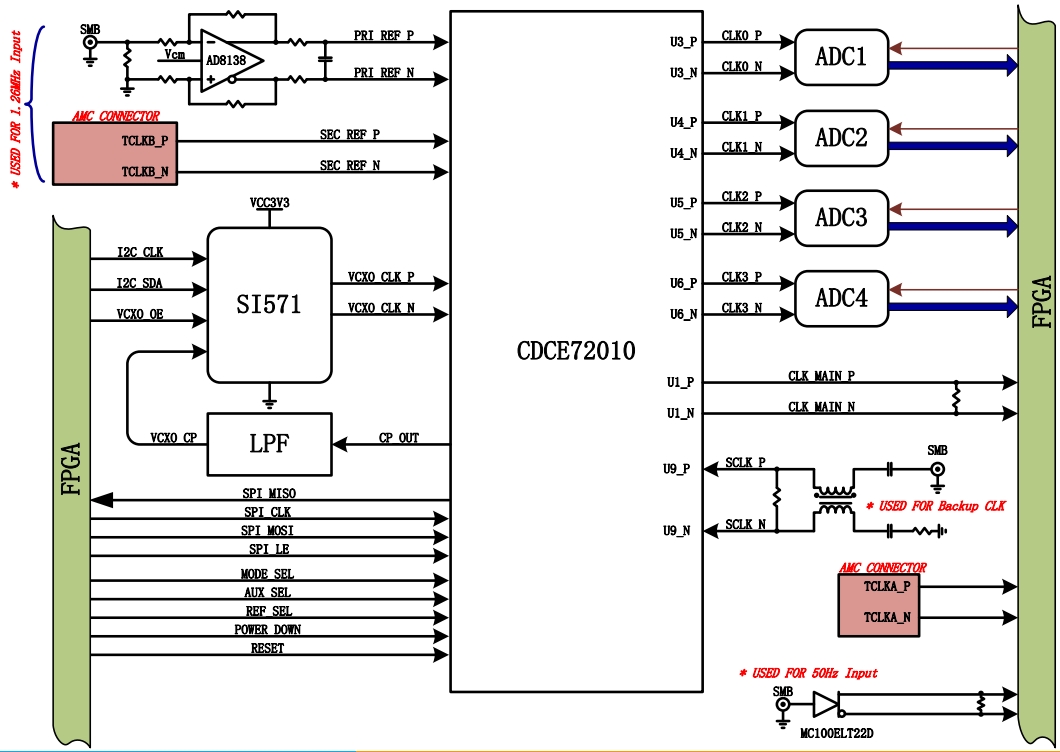
- Power Regulator
- **Clock Logic**
- FPGA Logic
- **ADC Logic**
- NET Logic
- Other Logic…



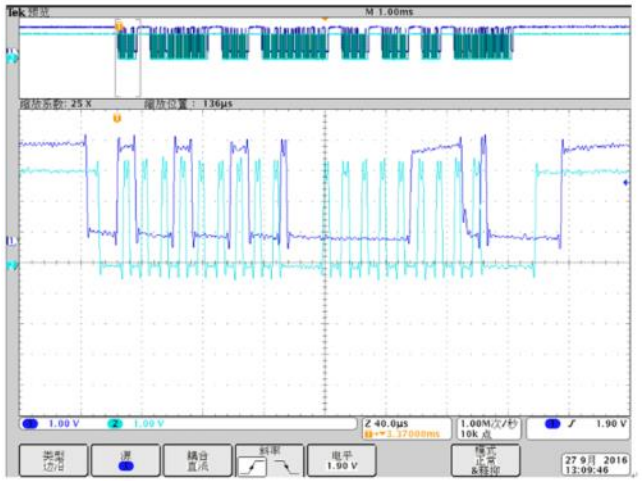



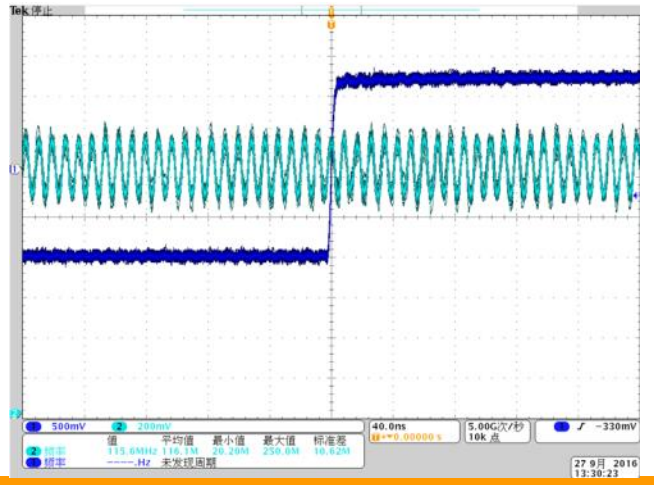
# Clock logic Scheme



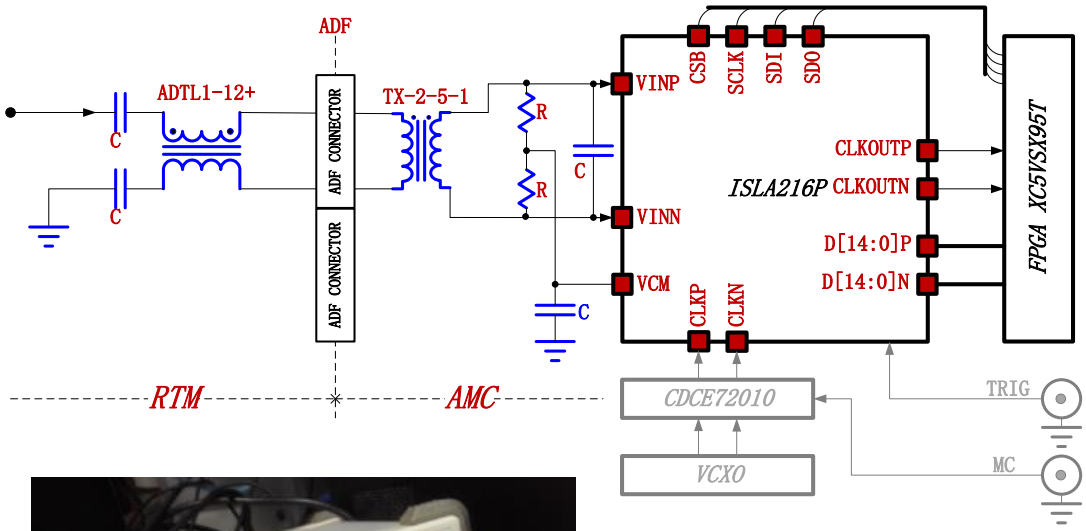



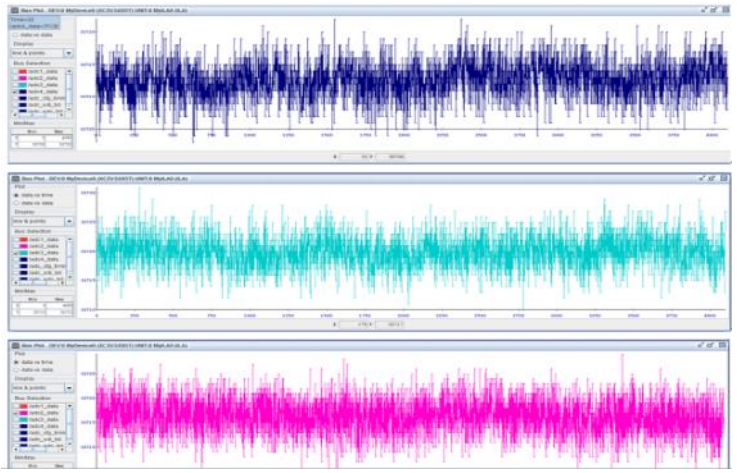

- SI571 Configuration ( I2C )
- CDCE72010 Configuration ( SPI )



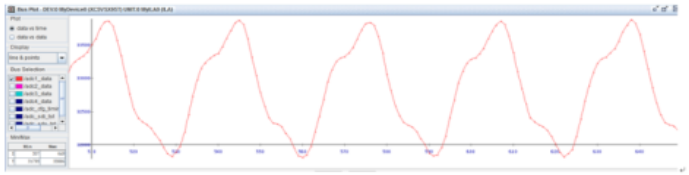


# ADC Logic Scheme

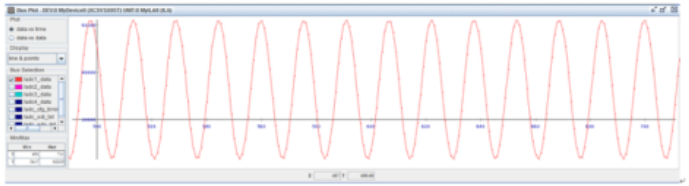


5MHz

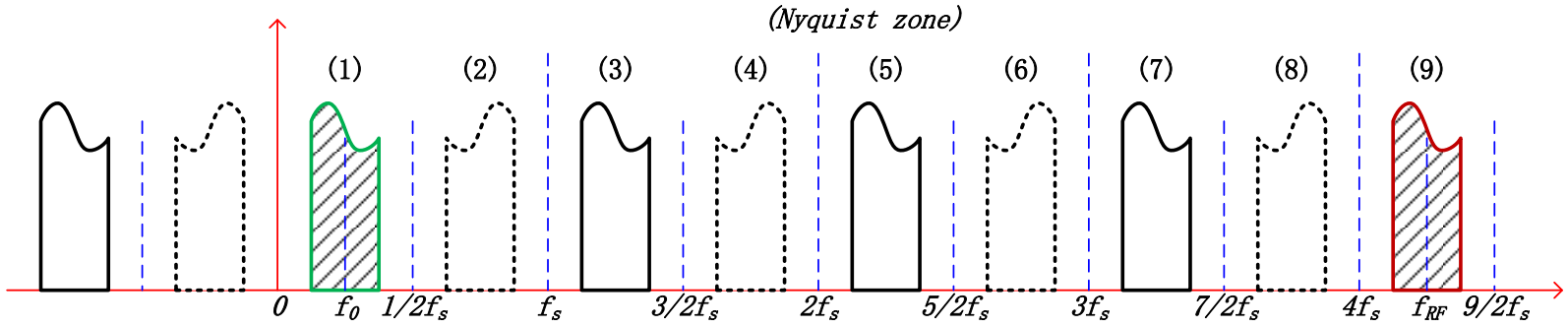


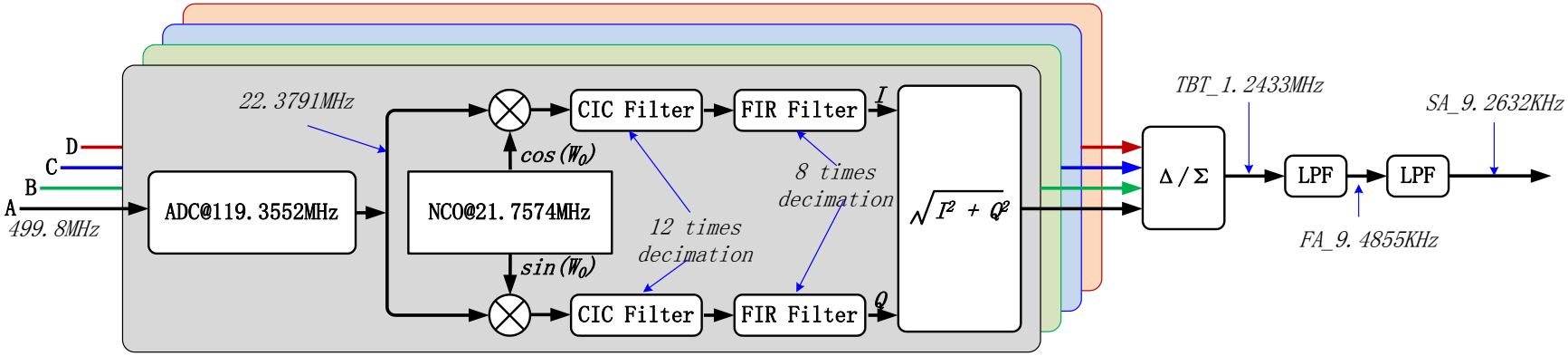
10MHz



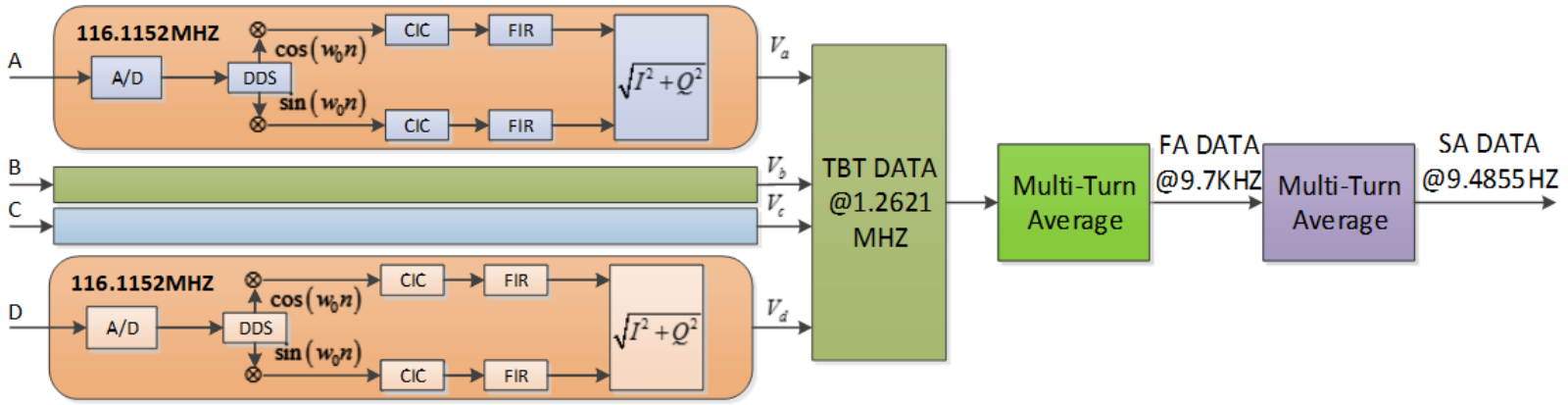
# 3.3 Algorithm of Firmware design

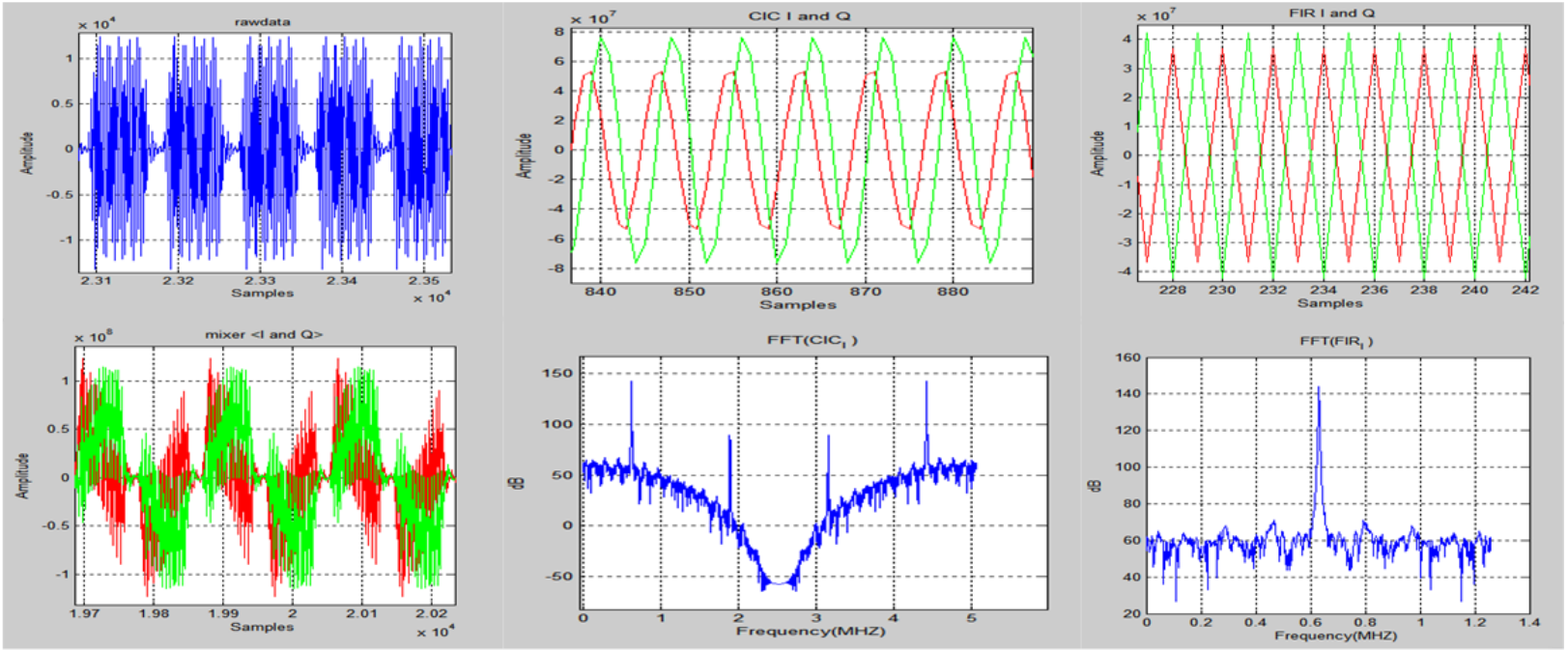
- MATLAB simulation (by YuFei Ma)
- HDL Implementation



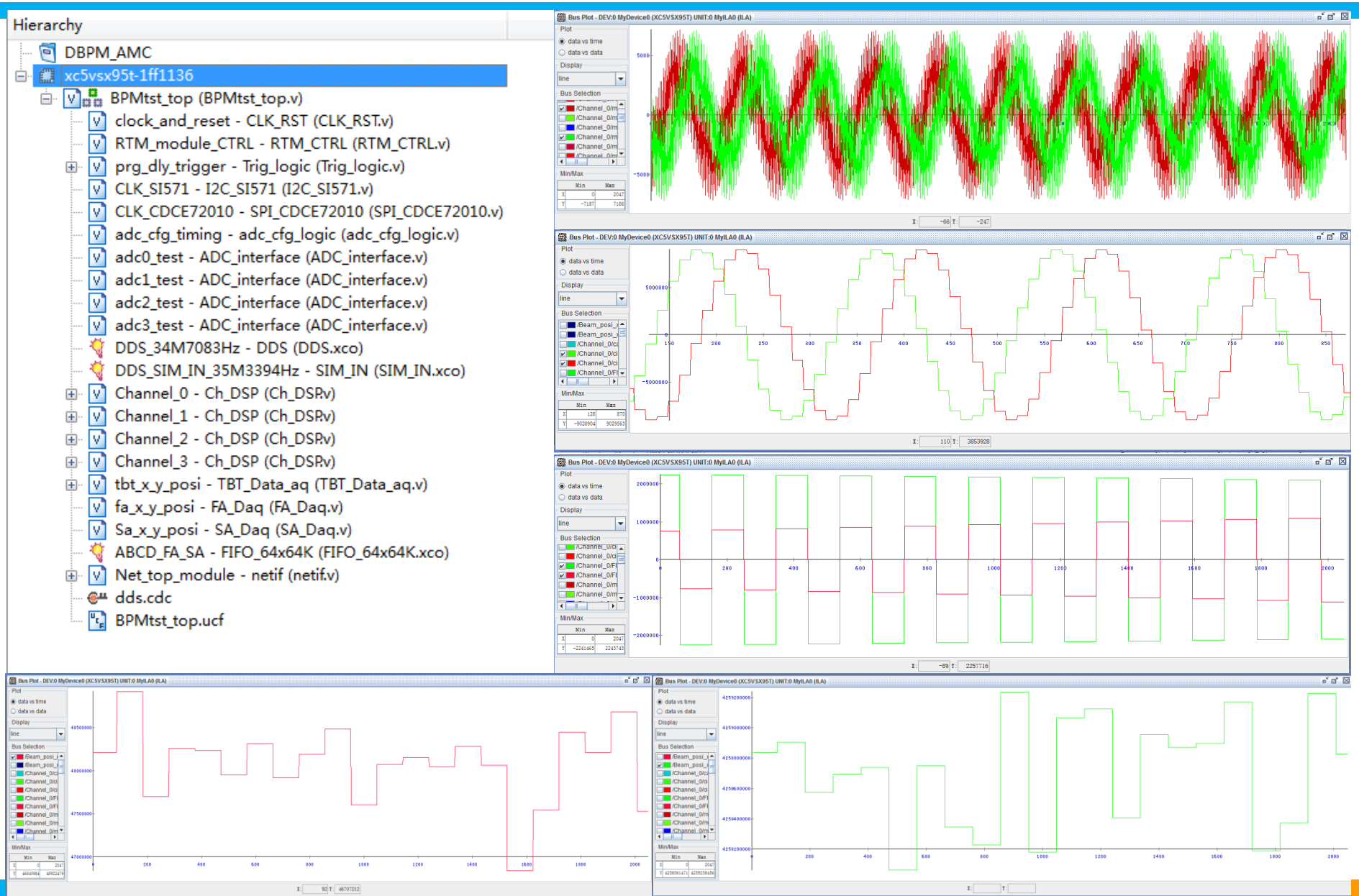



# MATLAB simulation



# HDL Implementation

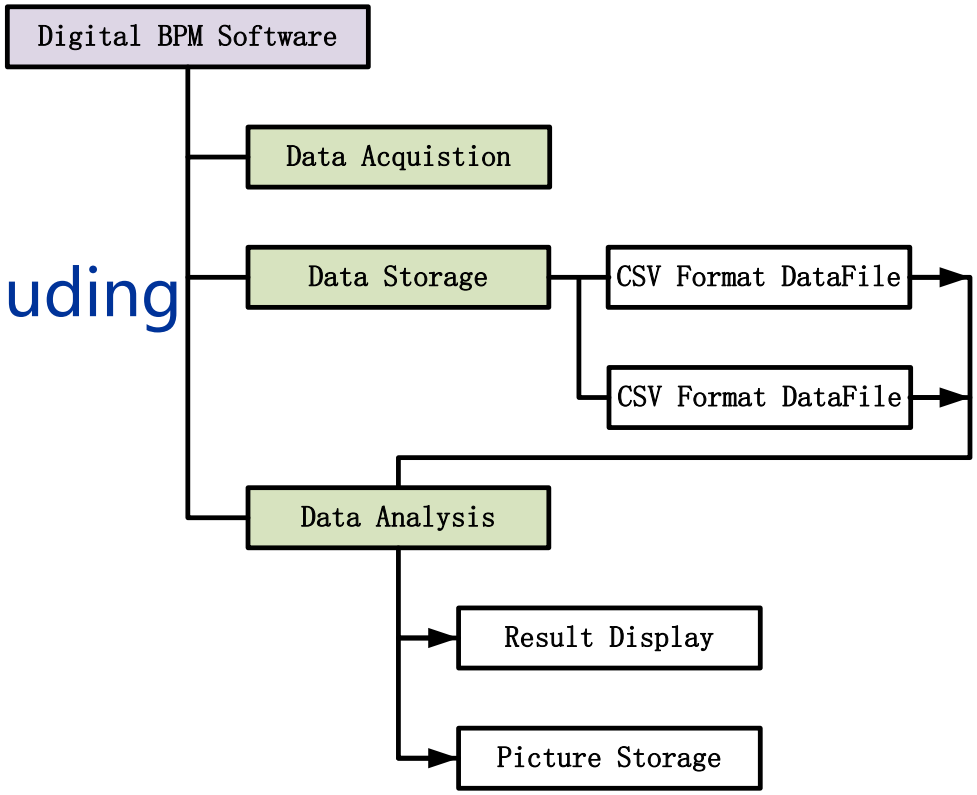


# Other Algorithm study

- DFT Algorithm(Fang Liu )
- Hilbert transformer method. ( Qiang Ye )
- Time domain dynamic window integrating method. ( YuFei Ma )

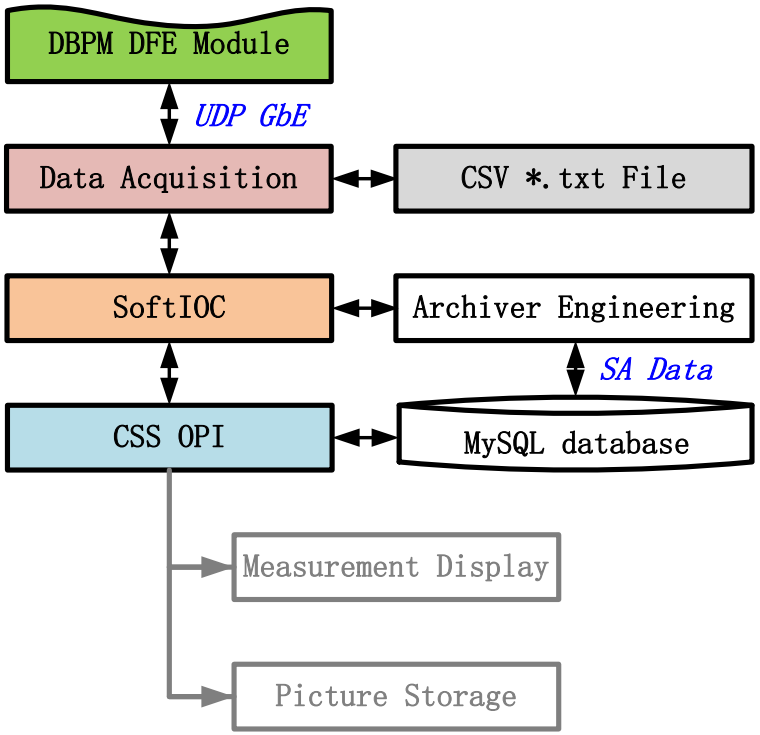
# 3.4 DBPM Software design

- Software framework include 3 main part:
  - Data Acquisition
  - Data Analysis
  - Data Storage
- The Software is built with **Python** (2.7.10) tools, including module:
  - Scipy1.0
  - Numpy
  - Pandas
  - Matplotlib
  - Pyepics
  - Pyqtgraph



# Data Acquisition Module

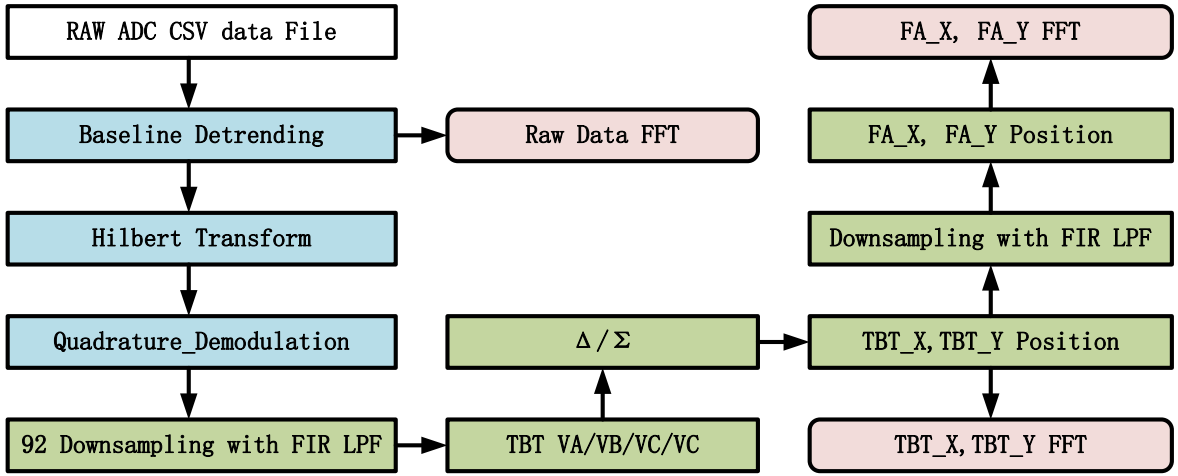
- SA Data Acquisition function block.
  - Data Acquisition control logic
  - Write/Read CSV file logic
  - EPICS IOC Logic
  - Data base logic
  - Graphical User Interface
  - …



# Data Analysis Module

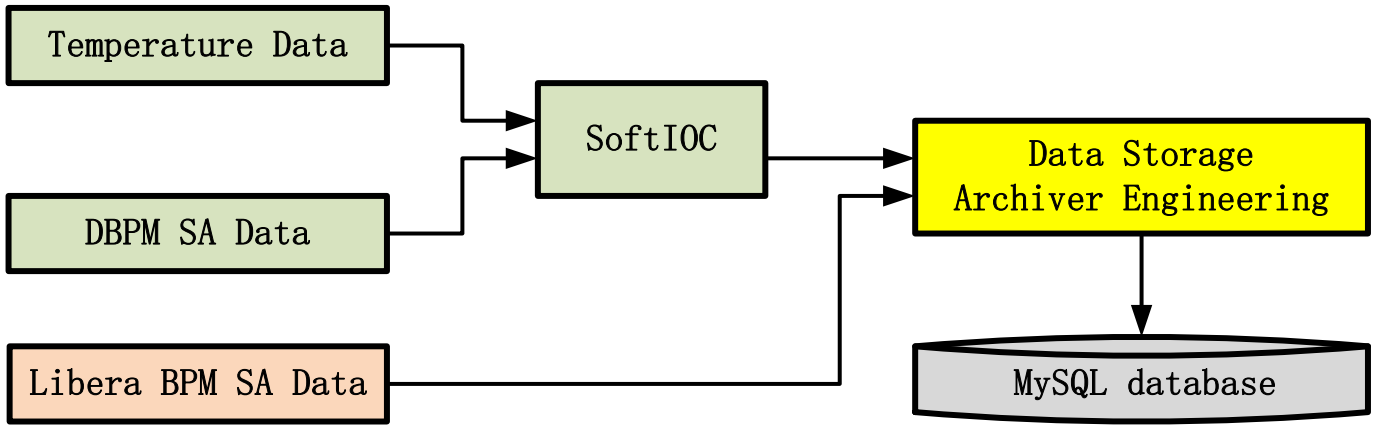
- Data Analysis function block.
  - Data Hilbert Transform and Quadrature Demodulation
  - TBT and FA Position calculation
  - FFT Analysis.

*Note: The function is designed to verify the result processed in FPGA.*

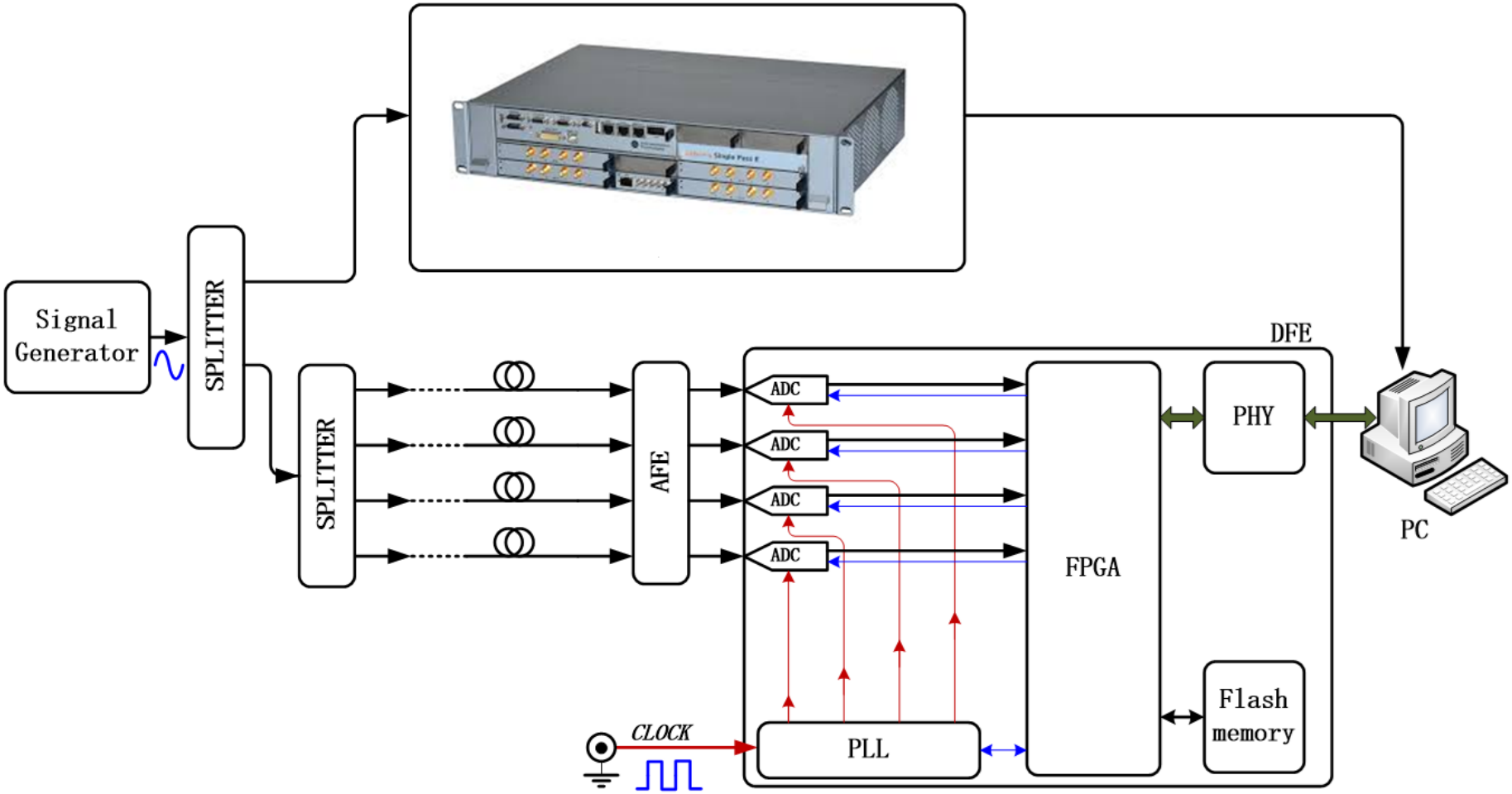


# Data Storage Module

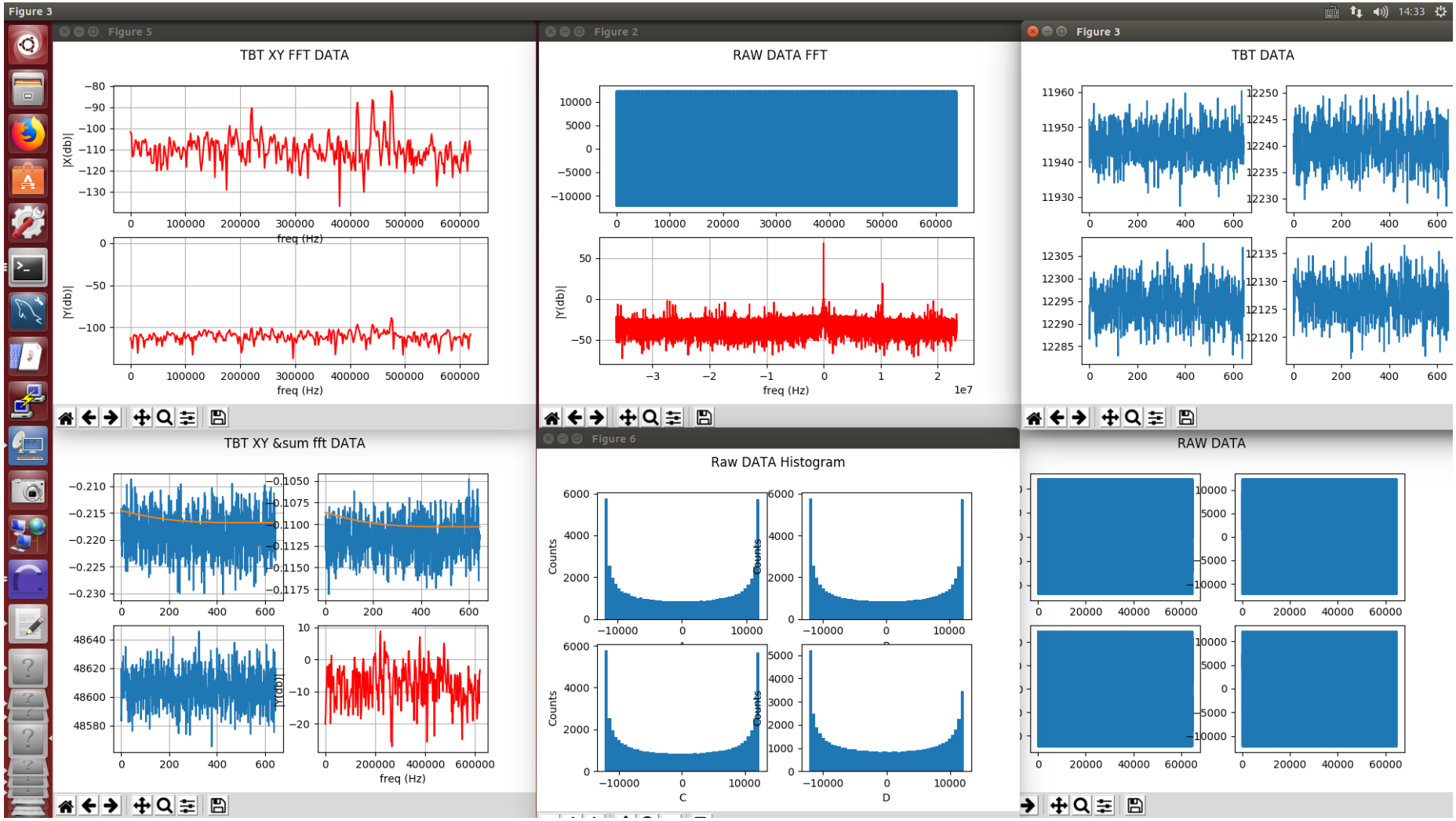
- Two Methods are used in Data Storage:
  - CSV txt format file
  - RDB  Archiver Engineering MySQL database



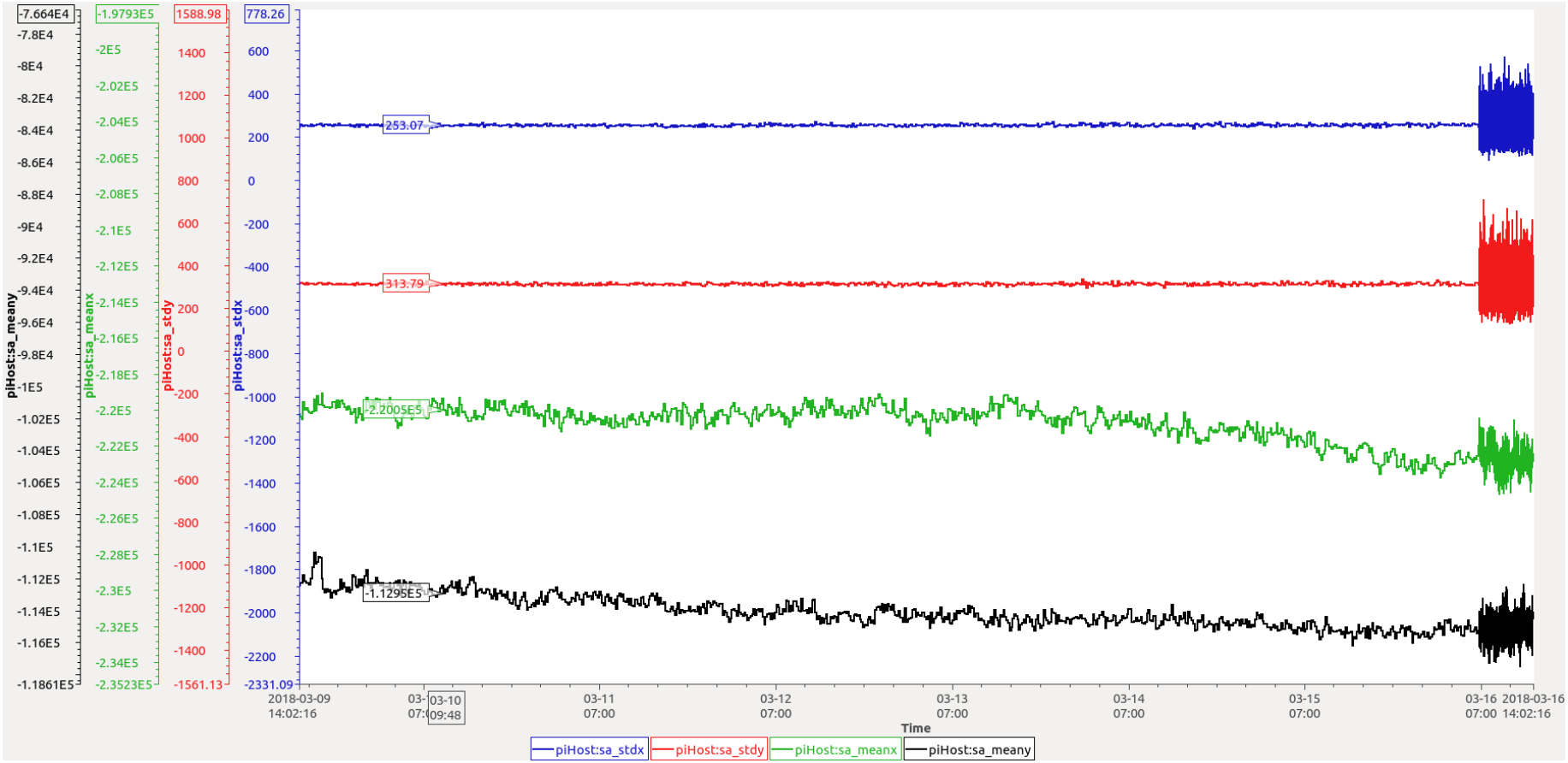
# 3.5 Digital BPM testing



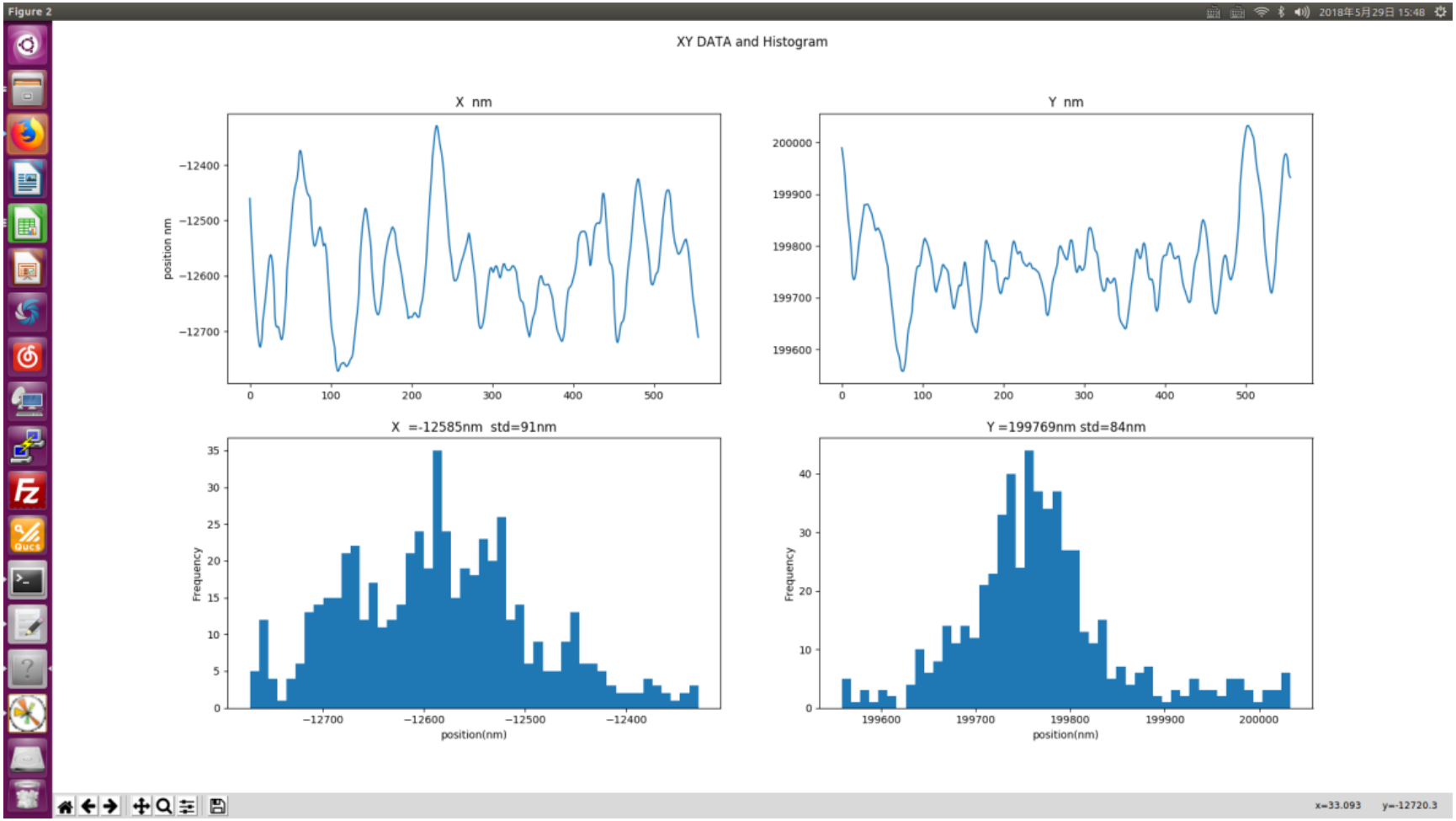
# RAW ADC data and Analysis



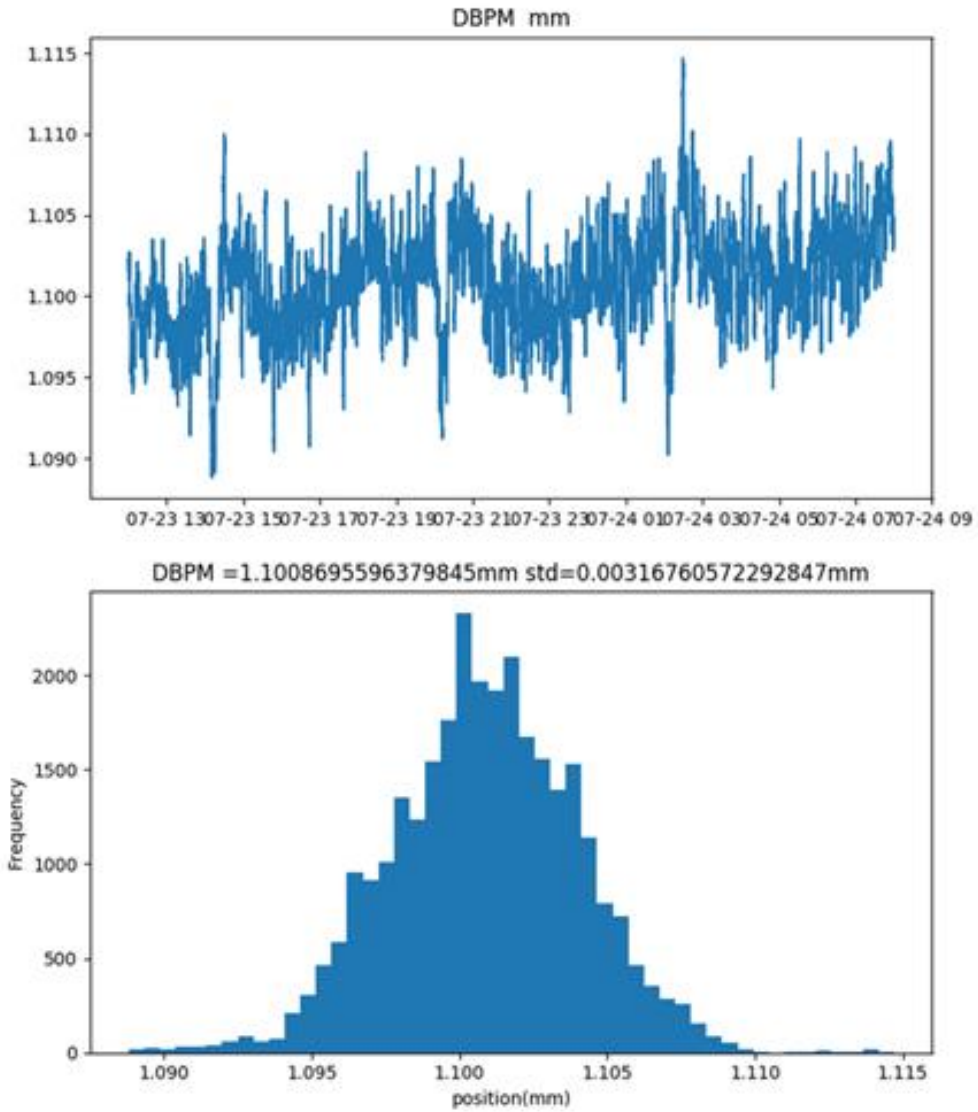
# Long term testing for 7 days



# Have Passed the Final acceptance tests



# 24 hours test with beam in BEPCII



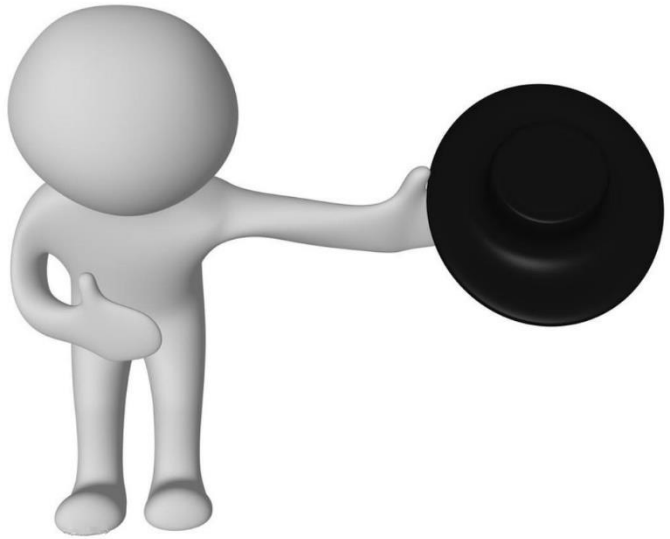
# 4. Summary and Acknowledgement

# Summary

- Digital BPM Electronics hardware has been designed carefully and had been tested in laboratory;
- The algorithm of BPM based on storage-ring has been developed;
- The digital BPM electronics have been tested with the real beam on BEPCII.
- A lot of work is on the way:
  - The HW, FW are to be optimized and improved;
  - Single pass BPM, BXB BPM is on schedule;
  - BPM's Calibrating and testing system are to be developed.
  - MicroTCA platform for DBPM in future.

# Acknowledgement


- During our Digital BPM electronic development, we got many experts help, and we would like to take this opportunity to express our sincere appreciation to them:
  - NSLSII
  - SIRIUS
  - SSRF
  - HLS
  - I-Tech
  - …

*Thanks for your attention*