7th MicroTCA Workshop

Software and Hardware Development for the MicroTCA Based LLRF System at IHEP

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Outline

Software

01 FPGA Firmware Framework

02 LLRF Control Algorithms

03 EPICS Software Design

Hardware

01 RTM RF Front-end

02 RTM LO Generator

03 DIO RTM and FMC Card

Software Development

CPU board running Linux with EPICS control system

SIS8300 series digitizer

SIS8900 and DWC8VM1 RTM

FPGA Firmware Framework

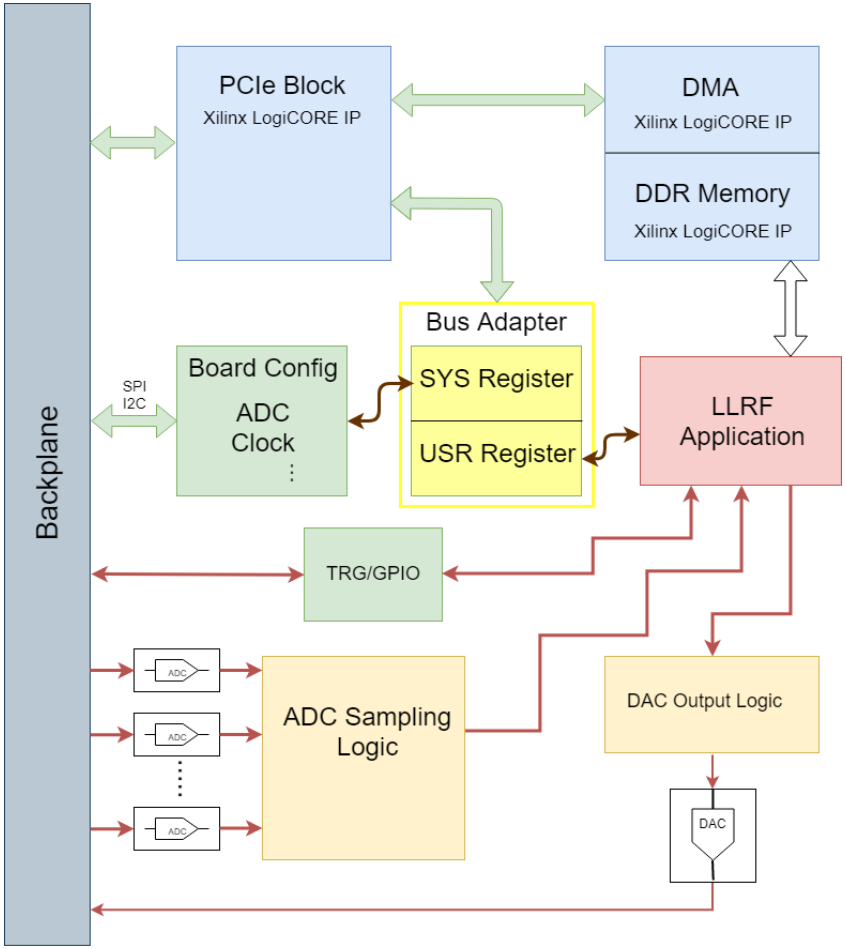
- **SIS8300-L2 MTCA.4 Digitizer**

- 4 lane PCI Express Connectivity
- 10 Channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Gigabit Link Port Implementation to Backplane
- Twin SFP Card Cage for High Speed System Interconnects (not used)
- Virtex 6 FPGA
- Dual boot
- MMC1.0 under DESY license LV91
- 2 GByte DDR3 Memory (flexible partitioning scheme)
- In Field Firmware Upgrade Support
- Zone 3 class A1.0, A1.0C or A1.1CO compatible

Major requirements of the framework:

- Peripherals on the board configuration: clocks, I/O buffers, ADCs, DACs, RTM configuration, etc.
- PCIe bus: provide high-throughput communication interface with other AMCs and CPU.
- DAQ: allows to read or write data stream in the external memory using Direct Memory Access (DMA) over communication interface.
- Provide interconnect between board section and the LLRF application.

FPGA Firmware Framework



- **FPGA Framework Structure**

Design of the framework:

- Same framework for different board:
  SIS8300 / SIS8300L2
  SIS8900 / DWC8VM1
- Function blocks are packed as different modules.
- PCIe, DDR, DMA using Xilinx LogiCORE IP
- Resource saving
- LLRF application fully separated from framework, user can concentrate on algorithms design without dealing with board-specific devices and functions

LLRF Control Algorithms

Various LLRF Control Requirements:

- Accelerator Driven System (ADS) Project:

superconducting cavity, CW feedback control, A/P control scheme, Feedforward beam load compensation, *GDR* (Generator Driven Mode), *SEL*(Self-Excited Loop)

- BEPCII Linac sub-harmonic bunchers:

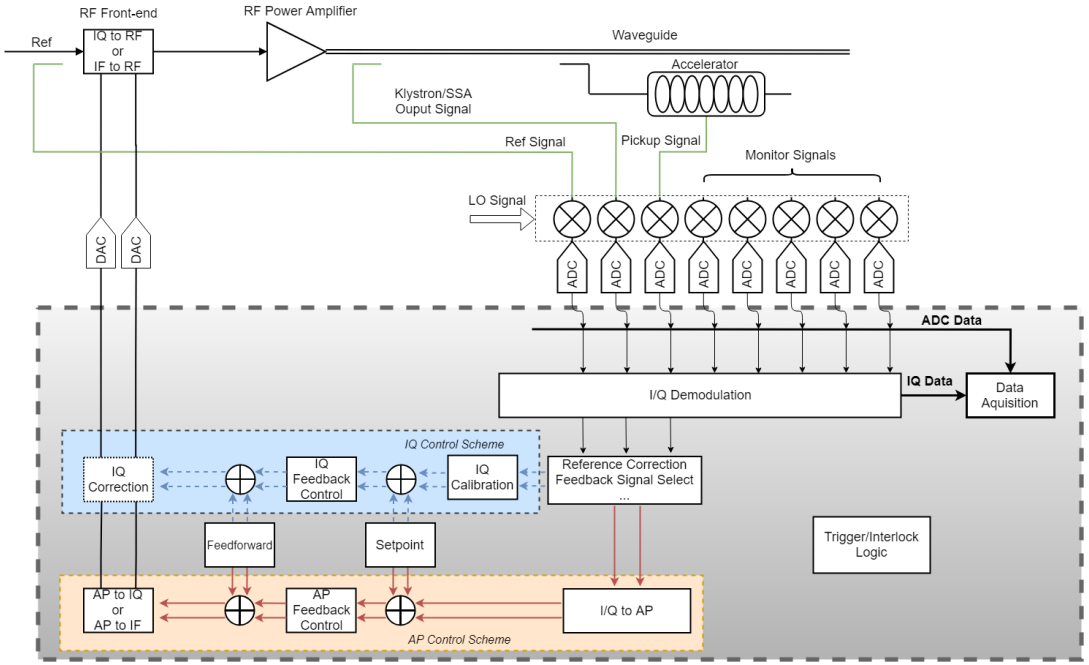
normal conducting cavities, intra-pulse feedback control, A/P control scheme, operating mode switch between E- and E+

- High Energy Photon Source (HEPS) Linac, BEPCII klystron phase control

normal conducting cavities, inter-pulse feedback control, phase shift keying (PSK), I/Q control scheme, adaptive feedforward

LLRF control algorithms must be versatile: Contains various functionalities so that it can be adapted to different applications without modification.

LLRF Control Algorithms



- **LLRF Application Structure**

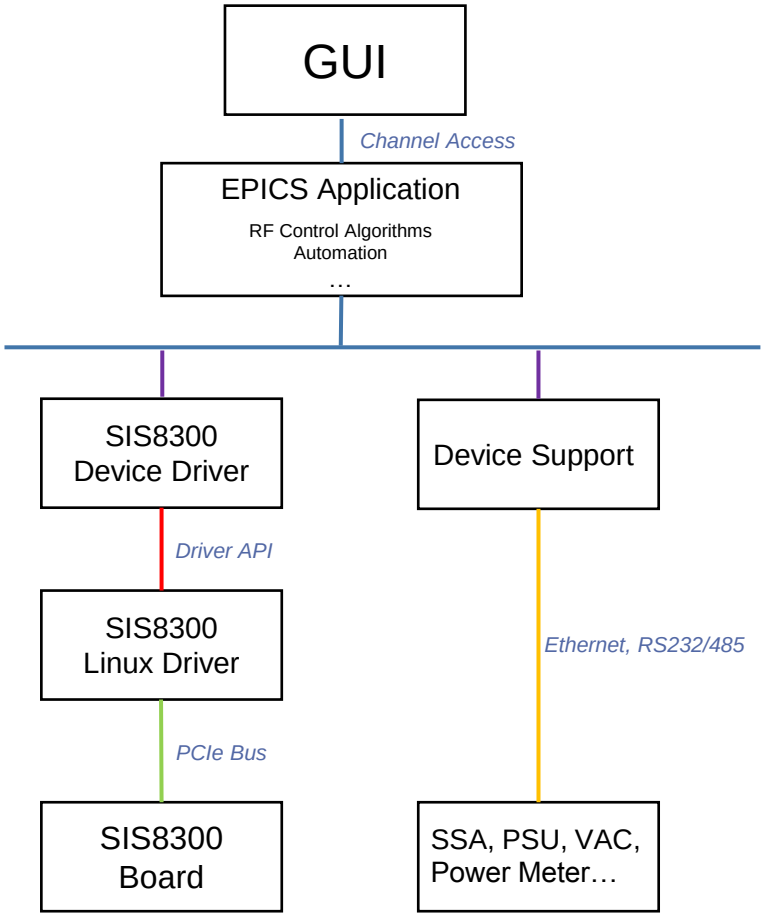
Major functions:

Multi-channel monitor and DAQ
A/P and I/Q control schemes
Feedback and feedforward
Intra-pulse and inter-pulse feedback
Trigger I/O and interlock logic
Configurable data stream bit width
...

Additional functions:

memory for open/close loop setpoint table, feedforward table storage
Waveform generator: arbitrary、frequency sweep、white noise
Ramp output
GDR/SEL Mode
...

EPICS Software Design



Hardware

SIS8300 AMC Board, SSA, VAC Meter, Power Meter…

Linux Driver

PCIe drive: support data exchange between the hardware and Linux system, access hardware register and memory.

EPICS Device Support

AMC board initialization
RTM I2C/SPI configuration
Register, DMA read and write using Linux driver API
Ethernet, RS232 device support

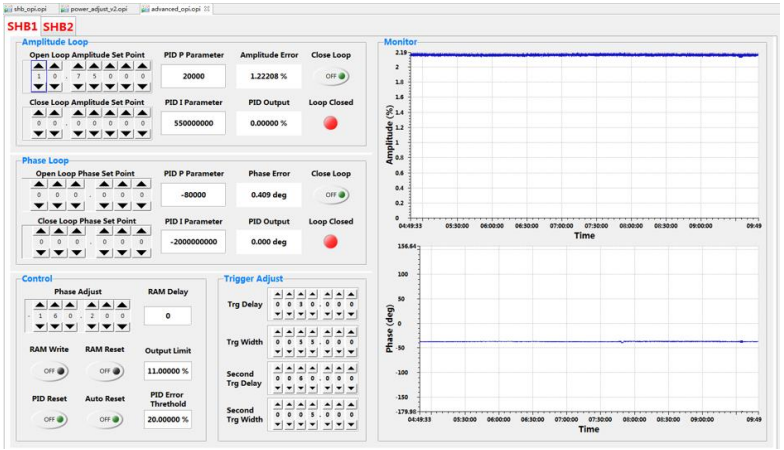
EPICS Application

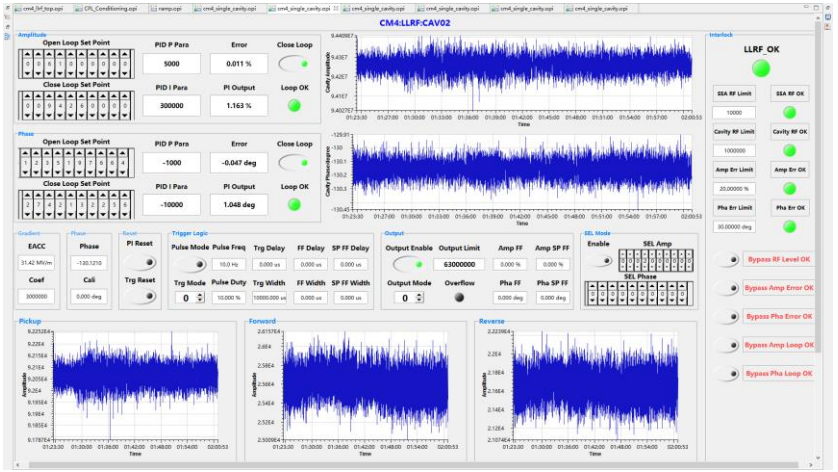
RF Control Algorithms:
DAQ data handling
Amplitude and phase calculation
Inter-pulse feedback
System exception handling
…

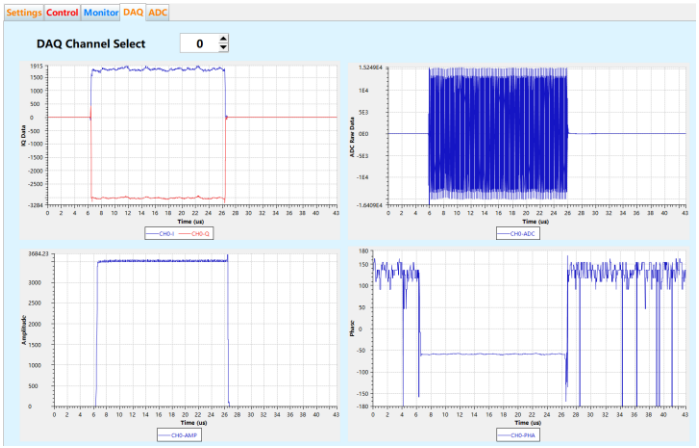
Automation program:
automatic RF aging
phase scan
…

EPICS Software Design

CSS based LLRF OPI:







LLRF Software Design

To be improved

Framework:
SIS8300-KU support
Internal memory bus for registers and memory areas access will be updated to AXI4 interface
Automated project generation and build workflow based on TCL script
…

LLRF Algorithms:
Adaptive feedforward, MIMO control
System identification and simulation
…

EPICS Software:
RF system measurement and conditioning
System monitoring/diagnosis
…

RTM RF Front-end

Main Features

- 8-channel 300 – 6000 MHz broad band down-converter
- 4 LVDS I/O
- Board status monitor
- 1-channel 50 – 6000 MHz broad band vector modulator
- Baseband low-pass filtered DC - 5 MHz
- VM output interlock

- 8-channel downconverter

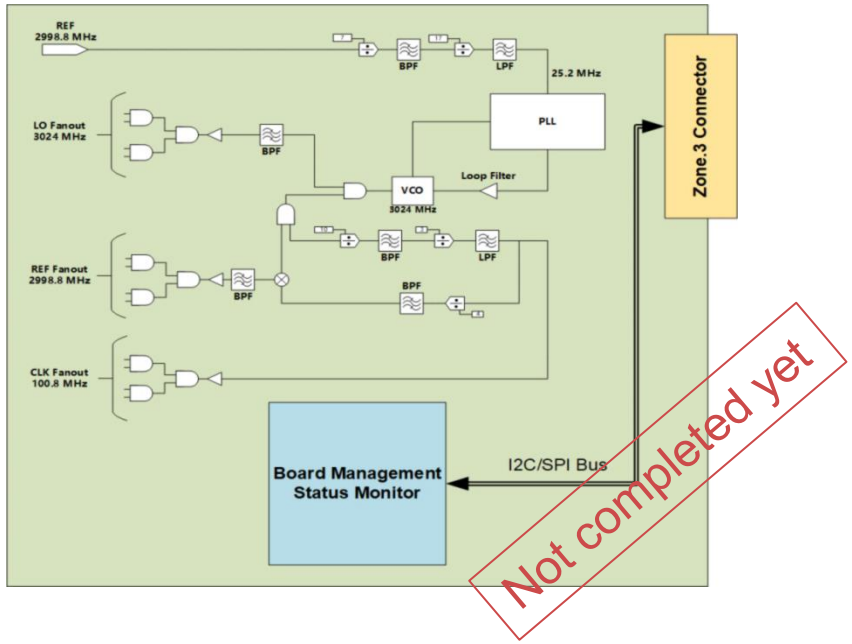
Tested Results (@325MHz, 650 MHz, 1.3GHz, 2.856GHz, 3.9GHz, 5.712GHz):

- RF return loss < -12 dB
- Channel crosstalk < -70 dB
- Downconverter P1dB > 12 dBm
- Downconverter 2nd Harmonic < -50 dBc
- VM carrier feedthrough < -45 dBm
- VM sideband suppression < -50 dBc
- VM output P1dB > 10 dBm
- Amplitude stability < ±0.03%
- Phase stability < ±0.03°

- 8-channel downconverter with 1-channel VM

RTM LO Generator

- Large in scale
- Difficult to maintain



- Single unit of the LO Generator RTM be responsible for generation of LO and clock signals and reference distribution for maximum 4 LLRF systems.

- Frequency:

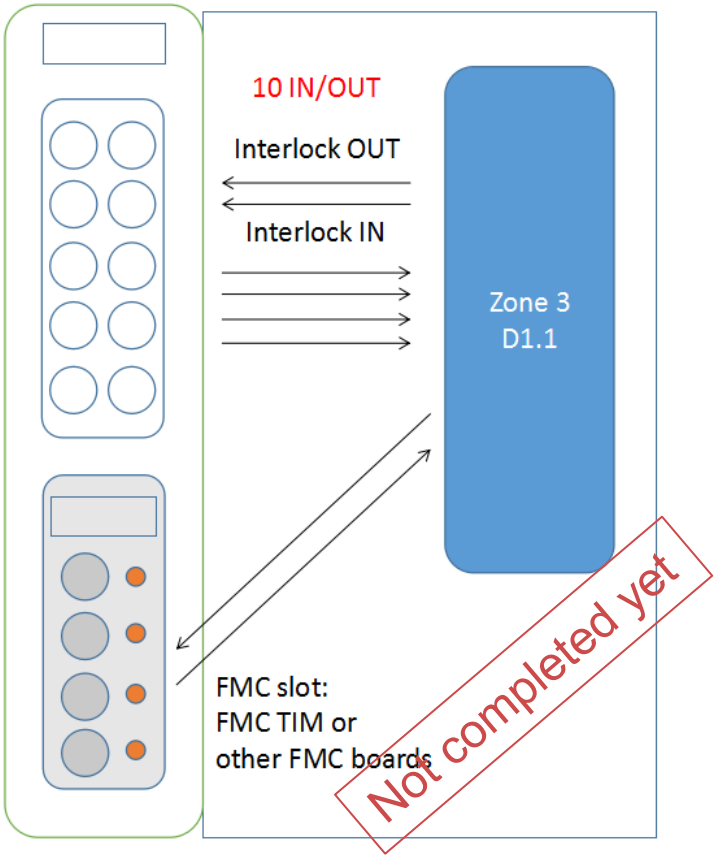
Reference signal: 2998.8 MHz LO signal: 3024 MHz
Clock signal: 100.8 MHz IF signal: 25.2 MHz

- AMC board for management, status monitor, temperature control need to be designed.

RTM-DIO board

General board for digital input/output applications: e.g. machine protection interlock

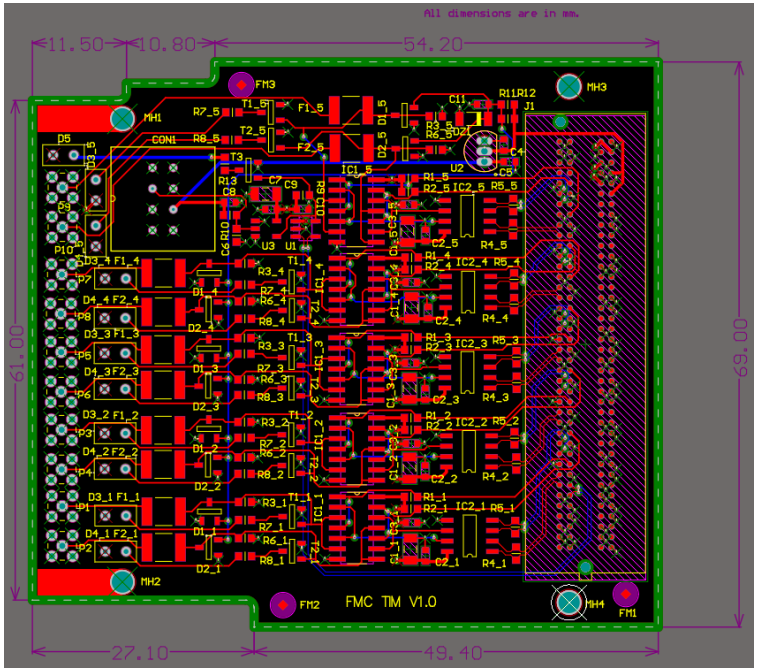
- Compatible with Class D1.1 (42 I/O, 2 high speed link) Zone.3 specification
- Each channel can be configured as input or output, also terminal impedance
- 10 DIO channels: 2 rows LEMO or 1 row MMCX connectors
- One FMC slot brings flexible functions: e.g. FMC TIM board, Fast Machine Protection using SFP connector
- All digital signals logical processed in the AMC FPGA through Zone.3 connector



FMC-TIM board

Used for local timing fanout: mainly pulsed machine (trigger for modulator/SSA/LLRF...)

- Compatible with DAMC-FMC25 or other FMC carrier board (with clock input)
- 10 LVTTL/TTL output or 1 optical TTL input/8 LVTTL/TTL output
- Optical connector: Avago HFBR-2412
- MMCX/SSMC connector
- LED blinks for each channel
- Terminal: 50Ω
- Rising/falling edge: <5ns/3ns
- Repetition frequency/pulse width/delay/polarity can be controlled in the FPGA on the FMC carrier board



Thank you for your attention!