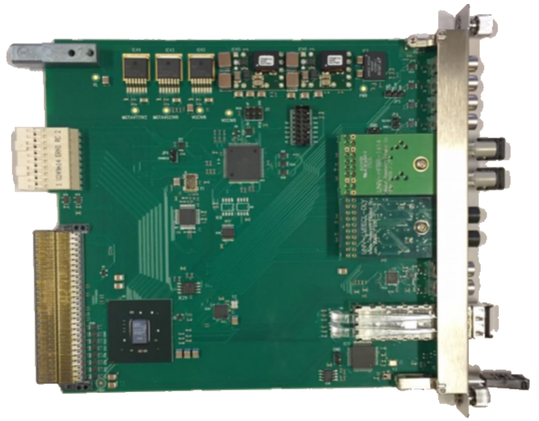
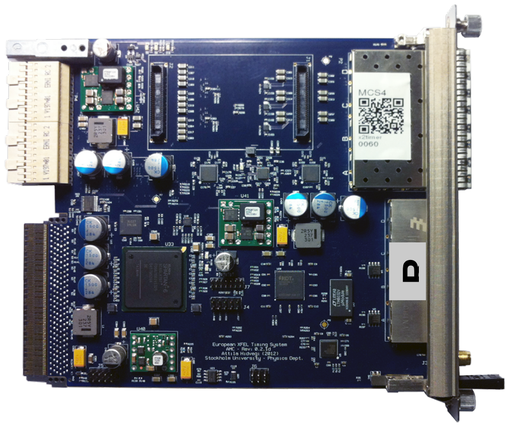
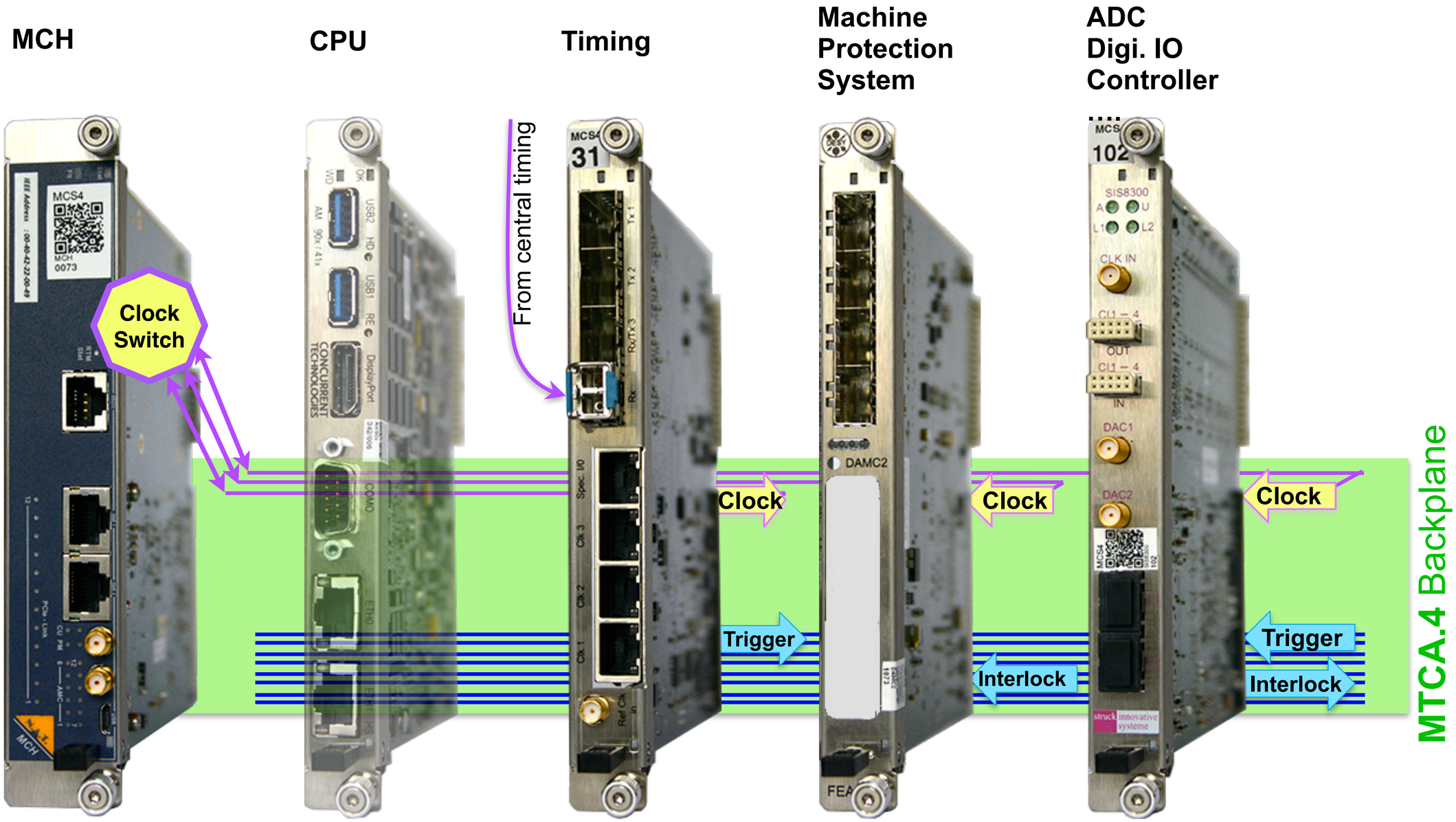
Timing in MicroTCA

MicroTCA Timing: Agenda

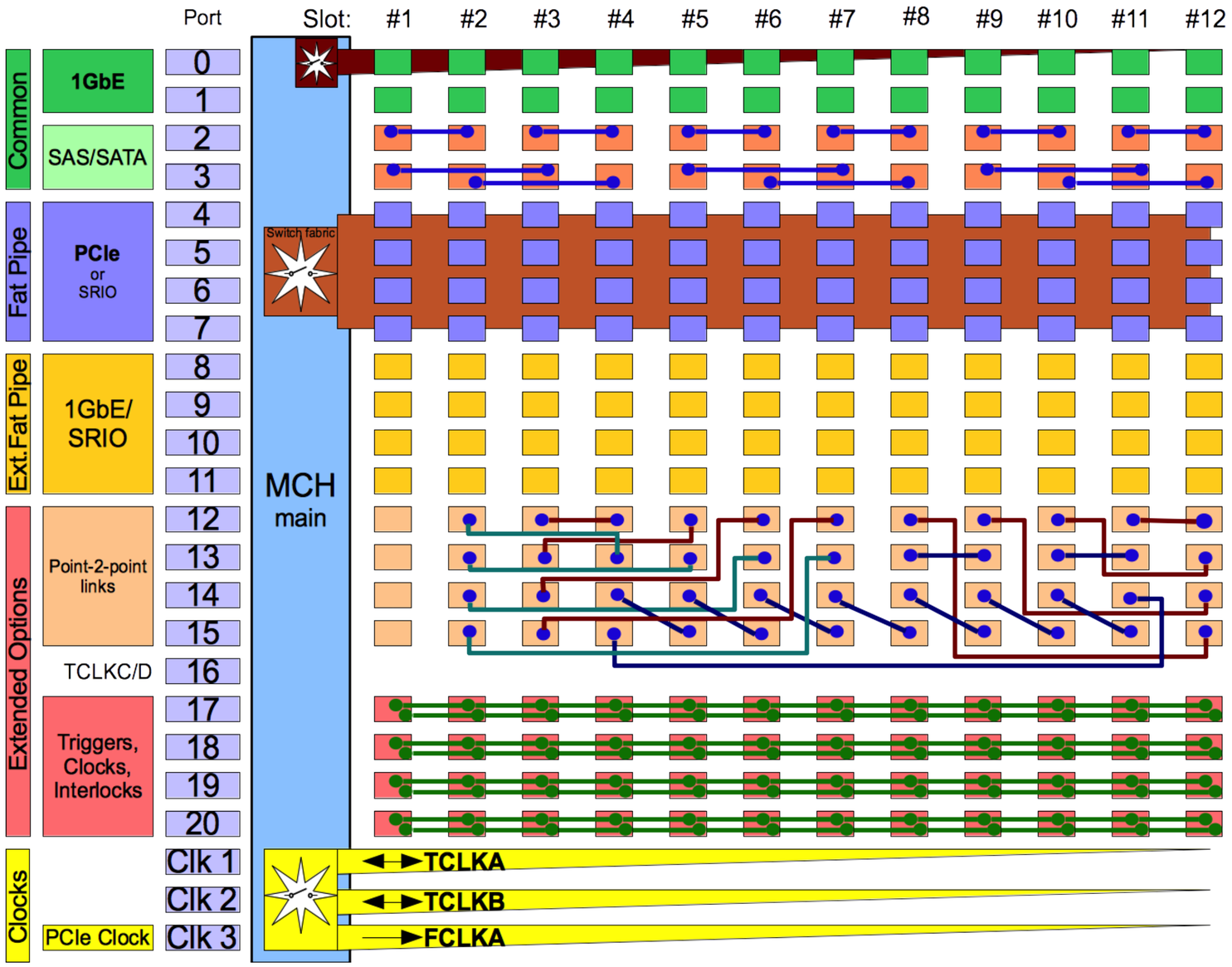
Start	Title	Presenter
15:30	Introduction	Kay Rehlich
15:35	The MRF timing system	Jukka Pietarinen
16:03	White Rabbit timing system	Miguel Méndez
16:31	The XFEL timing system	Kay Rehlich
16:59	End	



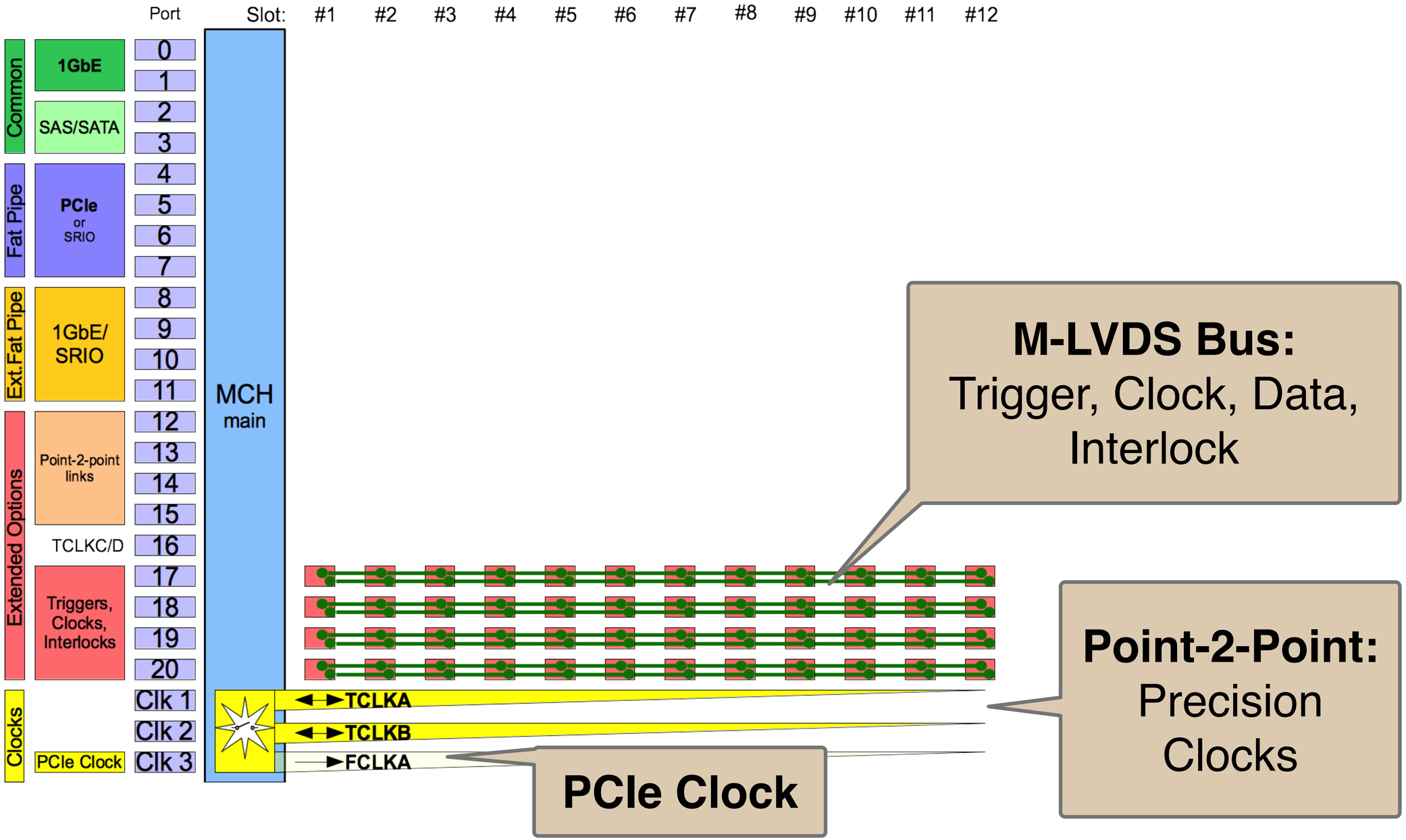



MCH
CPU
Timing
Machine Protection System
ADC Digi. IO Controller
Clock Switch
From central timing
Clock
Trigger
Interlock
Clock
Interlock
Clock
Trigger
Interlock
MTCA.4 Backplane

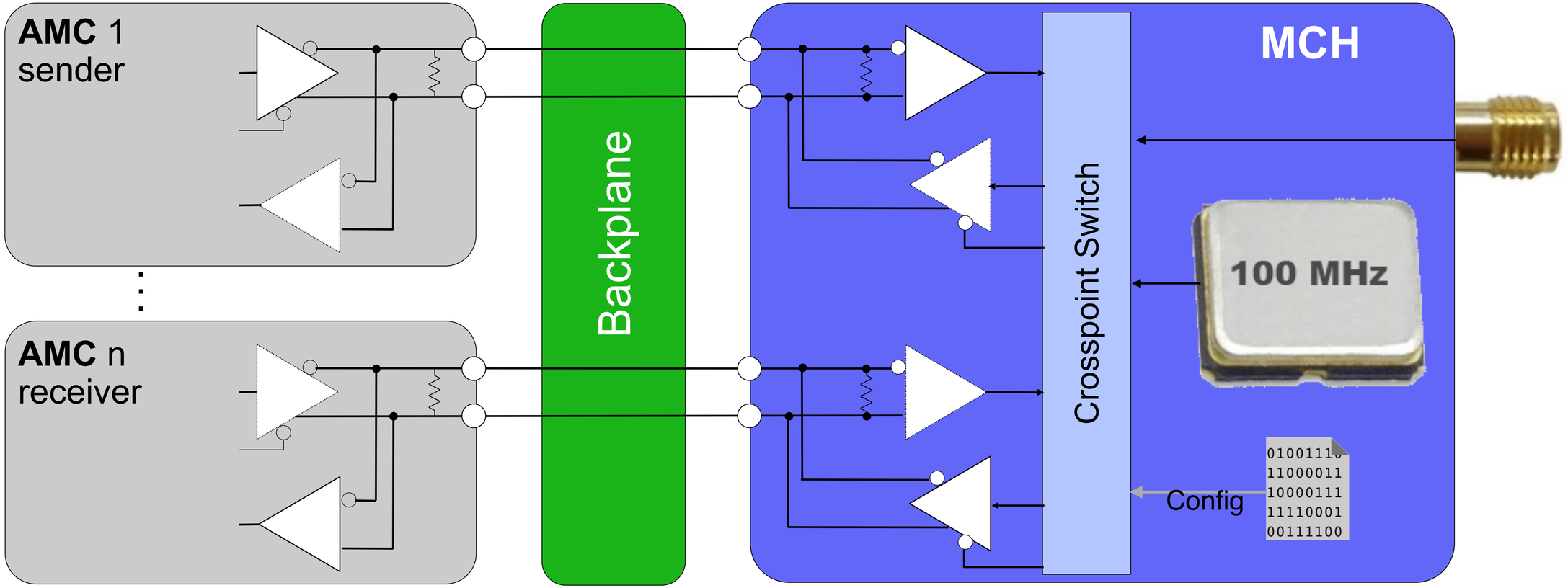
MicroTCA.4 Backplane



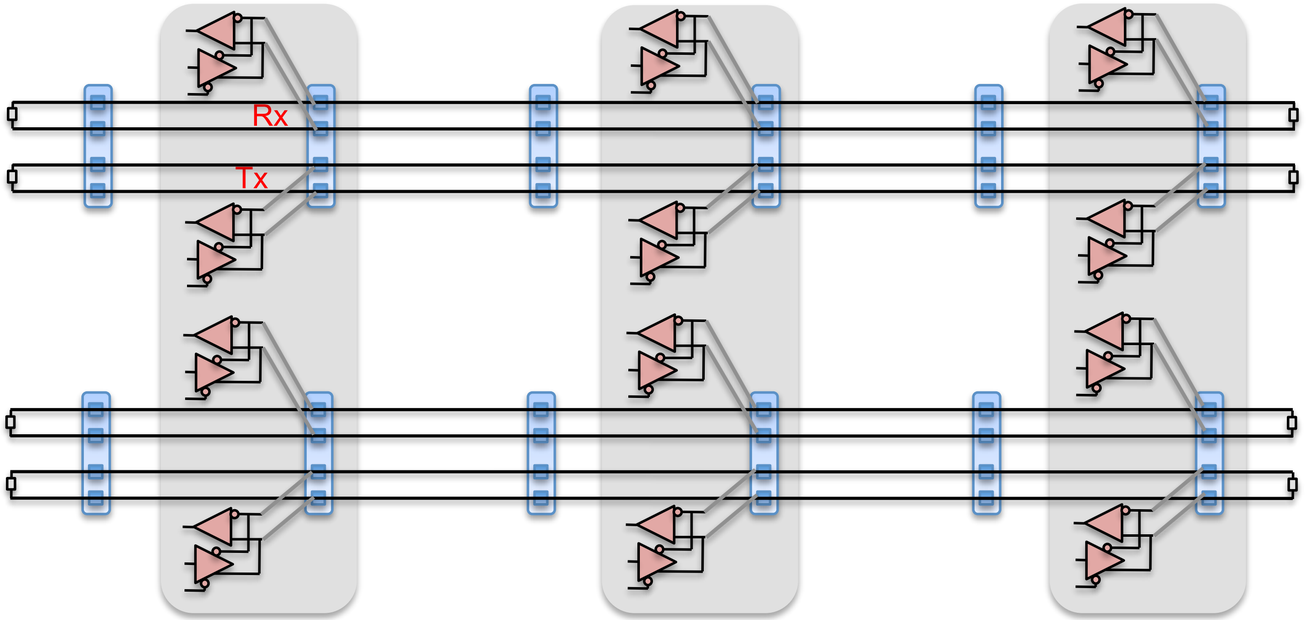
MicroTCA.4 Timing Part of the Backplane



MicroTCA.4 Timing Distribution Point-to-Point

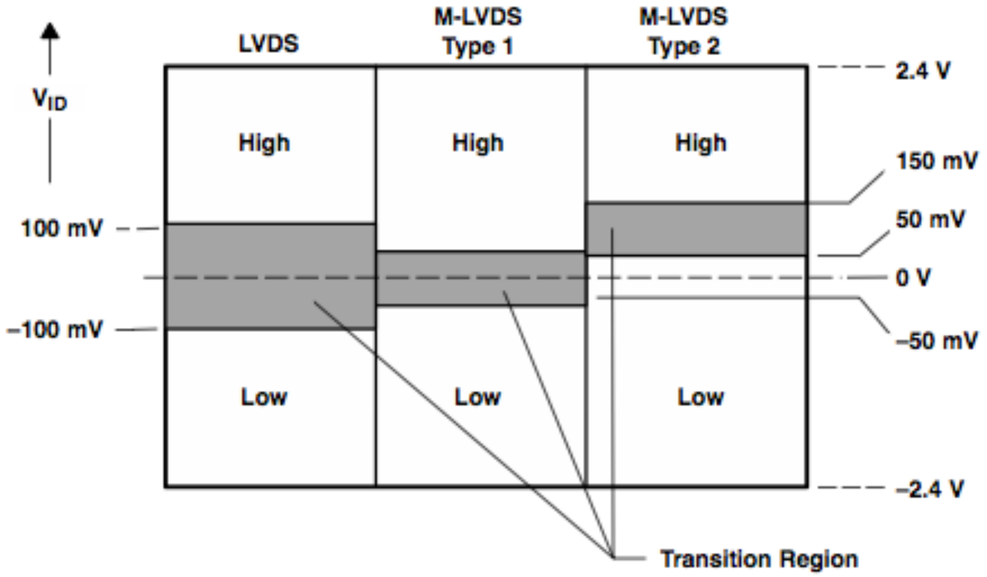


MicroTCA.4 Timing Distribution M-LVDS Bus



M-LVDS Type-2 receivers (SN65MLVD082) implement a failsafe by using an offset threshold. In addition, the driver rise and fall times are between 1 and 2.0 ns to provide operation at 250 Mbps while also accommodating stubs on the bus.
Outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

M-LVDS



LVDS and M-LVDS Differential Input Voltage Thresholds