struck innovative systeme

www.struck.de

How to talk to the hardware from the OS illustrated with Struck Digitizer AMC/RTM Combination



Tino Häupke

MTCA.4 Crate with a CPU, NAT-MCH and AMCs (SIS8300KU)







4. Dec. 2018 MicroTCA Beginners Tutorial

RMS for open AC/DC channel

PCI Express is used as Communication/Transfer bus



Struck SIS8300KU AXI-Based Xilinx Vivado FPGA Famework



"Hardware side"

SIS8300KU FPGA PCI Express Configuration

customize IP aScale FPGA Gen3 integrated Block for PCI Expre	255 (4.4)	SIS8300KU FPGA
ocumentation 🕞 IP Location C Switch to Defaults		Application/Functions
Show disabled ports	Basic Capabilities PF0 IDs PF0 BAR Legacy/MSI Cap MSI-X	 ↑
	Vendor ID 1796 Range: 0000FFFF Device ID 24 Range: 0000FFFF Revision ID 00 Range: 00FFF	Register Set
	Subsystem Vendor ID 1796 Range: 0000FFFF Subsystem ID 24 Range: 0000FFFF	↓
m_axis_cq +	Class Code	Xilinx PCIe IP
mi_cas_jct pice 7x_mgt pice 7x_mgt pice_cfg_mgt pice_cfg_mgmt pice_cfg_mgmt pice_cfg_mgmt pice_cfg_mcg_tx+ + pice_cfg_mgmt pice_cfg_mcg_tx + pice_cfg_mgmt pice_cfg_mgt pice_cfg	Base Class Menu Simple communication controllers Base Class Value 07 Sub Class Interface Menu Generic XT compatible serial controller Sub Class Value 00	PCIe Configuration: - Vendor ID = 0x1796 (*) - Device ID = 0x0024 (SIS8300KU)
sys_tak_us poles_us_mt_shared.ogic + sys_reset user_cik user_cik user_cik user_nk_up = user_ink_up = phy_rdy_out =	Interface Value 00 Class Code 070000	PCIe PHY



"Software side"





sis_root_gui_V2.3

4. Dec. 2018 MicroTCA Beginners Tutorial

A device driver enables the Access from a Userspace Application to a Hardware Device (Kernel space)

The driver provides:

Address-Mapped I/O (ioctl)

- the SIS8300KU "PCI bar 0 address space" is mapped into the "processor address space"

- enables processor reads/writes from/to the SIS8300KU Register Set with the system call "ioctl"

Stream-Oriented I/O (DMA)

- are handled/triggered by writing to the "DMA" and "IRQ" register set

- enables data transfer from/to the User-Memory (PC) to/from the AMC (SIS8300KU) Memory

Interrupts

- are handled by writing to "IRQ" register set

Install the SIS830x driver



1.

Copy the directory "sis8xxx-Linux" from the DVD to a local directory on the PC

2.

Go to the directory "driver"

3.

Execute "make"

4.

Execute ",sudo make install" (as root)

5.

The kernel object "sis8300drv.ko" is generated

	th@th-CELSIUS-M740: ~/SIS/testroom/driver
File Edit View Search Terminal H	Help
th@th-CELSIUS-M740:~/SIS/test	troom/driver\$
th@th-CELSIUS-M740:~/SIS/test	troom/driver\$
th@th-CELSIUS-M740:~/SIS/test	troom/driv <mark>er</mark> \$ dmesg grep sis8300
[513.414399] <mark>sis8300:</mark> drive	er unloade <mark>t</mark>
[513.913174] <mark>sis8300</mark> : Drive	er Version: v1.13 (c)SIS GmbH 2018-11-28
<pre>[513.913177] sis8300: regis</pre>	stering for devices:
[513.913179] sis8300: Vendo	or/Device: 1796/0018
[513.913181] sis8300: Vendo	or/Device: 1796/0019
[513.913183] sis8300: Vendo	or/Device: 1796/0022
[513.913184] sis8300 : Vendo	pr/Device: 1796/0023
[513.913186] 5158300: Vendo	Dr/Device: 1796/0024
[513.913187] 5158300: Vendo	DF/Device: 1796/0028
[513.913189] 5158300 ; Vendo	price index @
$\begin{bmatrix} 513,913283 \end{bmatrix} \\ 513,913414 \end{bmatrix} \\ cic 8300 \\ c32 \end{bmatrix} \\ 0$	CIEVORASS link status: 4 lanes at 2 5Ch/s
$\begin{bmatrix} 513.913414 \end{bmatrix} = 5136500-53.$	endor id: 1796/device id: 0019
[513.913440] sis8300-s3: ba	ard mapped to:000000000ceec0a8c size:16384
513.913569] sis8300-s3: de	evice number: major:0 minor:235
513.913585] sts8300-s3: dr	ma sw buffer:0000000058330443 len:131072
513.913587] sis8300-s3: dr	na hw buffer:0000000031020000 len:131072
513.913602] sis8300-s3: dr	na 2 sw buffer:0000000013252112 len:131072
[513.913603] sis8300 -s3: dr	ma_2 hw buffer:0000000031040000 len:131072
[513.913604] sis8300-s3: ir	rq line: 27
[513.913623] <mark>sis8300</mark> -s3: ma	odule firmware/revision: 83022012
[513.913024] 5136300-53 ; at	tternative device handle: /dev/stsobou-u
513.913708] 5158300 -51: de	evice index 1
[513.913/85] 5158300 -51: PC	LIEXPRESS LINK STATUS: 4 Lanes at 5.0GD/S
[513.913/8/] St\$8300-S1: Ve	endor (d: 1790/device (d: 0024
[513.913001] 5158300-51; de	a_10 a_1a_2 a_2a_2 a_2
[513.913097] St38500-S1. de	na sw huffer:00000000000522514 len:131072
[513.913912] sts0500-s1: dr	na hw buffer:00000000000000000000000000000000000
[513.913928] sis8300-s1: dr	na 2 sw buffer:00000000000000000000000000000000000
513.913930] sis8300-s1: dr	na 2 hw buffer:0000000031080000 len:131072
[
[513.913936] sis8300-s1: mo	odule firmware/revision: 83031911
513.913937] sis8300-s1: al	lternative device handle: /dev/sis8300-1
the the CELSTUS-M740 /STS /test	



the driver generates two Device Handles/Names for each hardware device:

- 1. an enumerated Name: sis8300-1
- 2. a PCIe Slot dependent Name: sis8300-s1

A Desy SIS8300 driver is available, also (https://github.com/MicroTCA)

MicroTCA		
Repositories 6		
GitHub is home to over 28 million developers development teams, manage per	eam on GitHub s working together. Join them nissions, and collaborate on pi gn up	to grow your own rojects.
Find a repository Type: All Language: All Upciedev		Top languages
universal PCIe driver, provides the base PCIe functionality to be used by the top level drivers	^	● C ● C++
● C ¥1 1 GPL-2.0 Updated on 22 Feb		People 0>
pciedev Simple PCIe driver builded on top of upciedev	۸	This organization has no public members. You must be a member to see who's a part of this organization.
C++ 4 GRI-2.0 Updated on 22 Feb		
x1timer Device driver for DESY FLASH and XFEL x1timer, x2timer, and NAT NAMC- psTimer AMC Fast Timing System with ps resolution ● C ✿ GPL-20 Updated on 22 Feb	۸ <u>ـــــ</u>	
sis8300 device driver for STRUCK SIS8300 board based on upciedev ● C ⊈ GPL-2.0 Updated on 11 Dec 2017	۸	

Register Read Example with the system call "ioctl"

Application: \universal_tests\register\regread_iocall.c



reg = 0x00000081
th@th-CELSIUS-M740:~/SIS/testroom/universal_tests/register\$./regread_iocall /dev/sis8300-s1 0x0
reg = 0x83031911

Register Address Map for Identification ...

Offset	Access	Function
0x00	R	Module Identifier/Firmware Version register
0x01	R	Serial number register
0 x 02	R/W	reserved
0x03	R/W	reserved
0x04	R/W	User Control/Status register (JK)
0x05	R	Firmware Options register
0x06	R/W	ADC Temperature Sensor interface register
0x07	R	PCIe Status register

Register Address Map for the Application like "Sample Block Length"

0x120	R/W	ADC ch1 Memory Sample Start Block Address / Actual Block Address register
0x121	R/W	ADC ch2 Memory Sample Start Block Address / Actual Block Address register
		•••
0x129	R/W	ADC ch10 Memory Sample Start Block Address / Actual Block Address register
0x12A	R/W	ADC chx Sample Block Length register
0x12B	R/W	ADC chx Ringbuffer Delay register (0 to 2046)

Register Address Map for Stream-Oriented I/O (DMA)

0 x 200	R/W	DMA_READ_DST_ADR_LO32
0x201	R/W	DMA_READ_DST_ADR_HI32
0 x 202	R/W	DMA_READ_SRC_ADR_LO32
0 x 203	R/W	DMA_READ_LEN
0x204	R/W	DMA_READ_CTRL
0 x 205	R/W	DMA Readout Sample byte swap control
0x210	R/W	DMA_WRITE_SRC_ADR_LO32
0 x 211	R/W	DMA_WRITE_SRC_ADR_HI32
0 x 212	R/W	DMA_WRITE_DST_ADR_LO32
0x213	R/W	DMA_WRITE_LEN
0×214	R/W	DMA WRITE CTRL

Register Address Map for Interrupts

0 x 220	R/W	IRQ Enable
0x221	R	IRQ Status
0 x 222	W	IRQ Clear
0 x 223	KA	IRQ Refresh



Standard Hardware API Design Guide

Guideline for designing Hardware Access APIs for MTCA.4 Systems

MTCA_DG.1 R1.0 January 9, 2017



SHAPI Register Address Map

Table 3-1: Standard	Device Identification an	d Control	Registers
31 16	15 0		
Magic Word	SHAPI Version	0x00	ro
First Mod	ule Address	0x04	ro
Hardware ID	Hardware Vendor ID	0x08	ro
Device Firmware ID	Device Vendor ID	0x0C	ro
Firmwar	e Version	0x10	ro
Firmware	Timestamp	0x14	ro
	0x18	ro	
Firmwa	0x1C	ro	
		0x20	ro
Device C	apabilities	0x24	ro
Devic	e Status	0x28	ro
Device	0x2C	rw	
Device Int	0x30	rw	
Device In	0x34	ro	
Device Interrupt Active		0x38	ro
Scratch	0x3C	rw	

The SIS8300KU IOCTL Register Access implementation looks like the SHAPI IOCTL Register Access implementation The SIS8300KU DMA/IRQ implementation is similar to the SHAPI DMA/IRQ implementation The SIS8300KU Register Address Map is NOT identical to the SHAPI Register Address Map The Library contains functions/calls which correspond to the SIS8300KU FPGA Firmware Functions

a Library call contains multiple cycles to execute a "function" on the SIS8300KU for example: setup of the ADC chips via SPI



Struck SIS8300-KU AXI-Based Xilinx FPGA Framework



Startup Controller

 (initially proposed by ESS)

 Allows the complete Configuration
 of a SIS8300-KU Digitizer
 and an attached RTM
 without MTCA CPU Interaction

Vivado FPGA Famework: Startup Controller



Xilinx Software Development Kit: SDK



Build the SIS830x library (libSIS830x.so)

th@th-CELSIUS	-M740	m/1103			
th@th-CELSIUS	-M740:~/SIS/testroo	m/lib\$ ls libSIS830	x,		
ad9268.c	ads4 <mark>2lb69.c</mark>	libSIS830x.layout	si5326.c	sis830x.h	spiFlash.h
ad9268.h	ads42lb69.h	main.c	si5326.h	sis830xReg.h	
ad9510.c	internal.c	Makefile	si5338aSynth.c	sis830xStat.h	
ad9510.h	internal.h	obj	si5338aSynthDefault.h	sis830xType.h	
adc_ad9268.c	libSIS830x.cbp	rtmI2C.c	si5338aSynth.h	sis830xVer.h	
adc_ad9268.h	libSIS830x.depend	rtmI2C.h	sis8300kuReg.h	spiFlash.c	
th@th-CELSIUS	-M740:~/SIS/testroc	Μ/ LLDŞ			
th@th-CELSIUS	-M740:~/SIS/testroo	m/lib\$ make			
for dir in li	bSIS830 <mark>x/ libSIS886</mark>	<mark>0/ libsIs016</mark> 0/ libs	IS8864/; do make -C \$di	.r; done	
make[1]: Ente	ring directory '/ho	ome/th/SIS/testroom/	lib/libSIS830x'		
test -d obj/R	elease mkdir -p	obj/Release			
gcc -Wall -fP	IC -02 -fPIC -I/.	./driver -c si5326.	c -o obj/Release/si5326	.0	
gcc -Wall -fP	IC -02 -fPIC -I/.	./driver -c spiFlas	h.c -o obj/Release/spiF	lash.o	

1.	
Go to the directory	"lib"

2. Execute "make"

		th@th-CELSIUS-M	1740: ~/SIS/testroom/lib		●
File Edit View	Search Terminal Help				
th@th-CELSIUS	-M740:~/SIS/testroo	m/lib\$			
th@th-CELSIUS	-M740:~/SIS/testroo	m/lib\$			
th@th-CELSIUS	-M740:~/SIS/testroo	m <mark>/lib</mark> \$ ls libSIS830	x/		
ad9268.c	ads42lb69.	libSIS030x.layout	-rtnI2C.h	sis8300kuReg.h	spiFlash.c
ad9268.h	ads42lb69.	libSIS830x.so	si53 <mark>26.c</mark>	sis830x.h	spiFlash.h
ad9510.c	internal.c	main.c	si53 <mark>2</mark> 6.h	sis830xReg.h	
ad9510.h	internal.h	Makefile	si5338aSynth.c	sis830xStat.h	
adc ad9268.c	libSIS830x.cbp	obj	si5338aSynthDefault.h	sis830xType.h	
adc_ad9268.h	libSIS830x.depend	rtmI2C.c	si5338aSynth.h	sis830xVer.h	
thath CELETUE	M740 JETE Itosteoo	m/1+b¢			

3. The library "libSIS830x.so" is generated

// device handling

SIS830X_STATUS sis830x_GetNumberOfDevices(int *num); SIS830X_STATUS sis830x_OpenDeviceOnIdx(int idx, PSIS830X_DEVICE device);

```
SIS830X_STATUS sis8325_GetNumberOfDevices(int *num);
SIS830X_STATUS sis8325_OpenDeviceOnIdx(int idx, PSIS830X_DEVICE device);
```

```
SIS830X_STATUS sis830x_OpenDeviceOnPath(char *path, PSIS830X_DEVICE device);
SIS830X_STATUS sis830x_CloseDevice(PSIS830X_DEVICE device);
```

// general purpose register i/o

SIS830X_STATUS sis830x_ReadRegister(PSIS830X_DEVICE device, uint32_t addr, uint32_t *data); SIS830X_STATUS sis830x_WriteRegister(PSIS830X_DEVICE device, uint32_t addr, uint32_t data);

// memory i/o

```
SIS830X_STATUS sis830x_ReadMemory(PSIS830X_DEVICE device, uint32_t addr, uint32_t *data, uint32_t len);
SIS830X_STATUS sis830x_WriteMemory(PSIS830X_DEVICE device, uint32_t addr, uint32_t *data, uint32_t len);
```

// ad9510 divider setup

SIS830X_STATUS sis830x_AD9510_SPI_Setup(PSIS830X_DEVICE device, unsigned int* ch_divider_configuration_array, unsigned int ad9510_synch_cmd);

// adc ad9268 setup (SIS8300/SIS8300L/SIS8300L2/SIS8300KU)

SIS830X_STATUS sis830x_ADC_AD9268_SPI_Setup(PSIS830X_DEVICE device); SIS830X_STATUS sis830x_ADC_AD9268_SPI_Read(PSIS830X_DEVICE device, unsigned int adc_device_no, unsigned int spi_addr, unsigned int* read_data);

Register Read Example with a SIS83xx Library call "sis830x_ReadRegister(...)"

Application: \universal_tests\register\regread.c

#include "../../lib/libSIS830x/sis830x.h"



th@th-CELSIUS-M740:~/SIS/testroom/universal_tests/register\$./regread /dev/sis8300-s1 0x1
reg = 0x00000081

SIS830x Root GUI Application

SIS ROO	T GUI V2.3 (15.10.2018)	•••
File Open Device	<u>T</u> ools	<u>H</u> elp
struck	innovati systeme	ve
Crate Information — Device 1 (/dev/sis8 Device 2 (/dev/sis8	300-0) 300-1)	
Select Device	3300-0) 3300-1)	-
- Selected device info	rmation	
Type Firmware Version	SIS8300KU 0x83032010	
Serial Number	123	
ADC chip ID	0x32 -> 125MHz 16 bit	

The "SIS830x Root GUI" is a graphical application that provides access to serveral SIS ADC cards with different RTMs

The "SIS830x Root GUI" application requires an installation of the CERN ROOT framework → https://root.cern.ch/downloading-root

Device	Supported
SIS8300	yes
SIS8300 v2	yes
SIS8300L	yes
SIS8300L v2	yes
SIS8300L2	yes
SIS8300KU	yes
SIS8300KU-250MHz	yes
SIS8325	yes
SIS8900	yes
DWC8300	yes
DWC8VM1	yes
DS8VM1	yes

Build the SIS830x Root GUI Application

SIS ROOT GUI V2.3 (15.10.2018) 😑 🗈 😣	_tests\sis_root_gui_Vx.y" and excute "make"
<u>F</u> ile <u>O</u> pen Device <u>T</u> ools <u>H</u> el	n@th-CELSIUS-M740: ~/SIS/testroom/universal_tests/sis_root_gui_V2.3
struck innovative systeme	<pre>_root_gui_V2.3\$ _root_gui_V2.3\$ _root_gui_V2.3\$ _root_gui_V2.3\$ make I//lib/libSIS830x -I/home/th/root/include -c sis_rtm_device.cpp -o obj/Release/sis_rtm_device.o I//lib/libSIS830x -I/home/th/root/include -c sis_root_gui_tools.cpp -o obj/Release/sis_root_gui_tools.o I//lib/libSIS830x -I/home/th/root/include -c sis_root_gui_test1.cpp -o obj/Release/sis_root_gui_test1.o</pre>
Crate Information	'sis_root_gui"
Device 1 (/dev/sis8300-0) Device 2 (/dev/sis8300-1)	root_gui obj/Release/sis_rtm_device.o obj/Release/sis_root_gui_tools.o obj/Release/sis_root_gui_test1.o obj o obj/Release/sis_dwc8300_class.o obj/Release/sis_dummy_rtm_class.o obj/Release/sis_ds8vm1_class.o -lCore → -lRint -lPostscript -lMatrix -lPhysics -lMathCore -lThread -lGui -pthread -lm -ldl -rdynamic -lfftw3 -s
	_root_gui_V2.3\$ _root_gui_V2.3\$./sis_root_gui [
Select Device Device 1 (/dev/sis8300-0) Device 2 (/dev/sis8300-1)	and the "main control panel" will appear and displays all detected SIS devices
Selected device informationTypeSIS8300KUFirmware Version0x83032010Serial Number123ADC chip ID0x320x32-> 125MHz 16 bit	4. Dec. 2018 MicroTCA Beginners Tutorial

SIS830x Root GUI / Tools / Direct Register Access



Use Vivado chipscope to observe what happens inside the FPGA with a "Register Write"

SIS830x Root GUI / Tools / Direct Register Access



Use Vivado chipscope to observe what happens inside the FPGA with a "Register Read"

4. Dec. 2018 MicroTCA Beginners Tutorial

SIS830x Root GUI / Tools / FPGA programming menu

SIS ROO	T GUI V2.3 (15.10.2018) 🖨 🗊 😣
struck	Iools <u>H</u> elp Register Read/Write FPGA programming menu INNOVATIVE Systeme
Crate Information — Device 1 (/dev/sis8: Device 2 (/dev/sis8:	300-0) 300-1)
Colort Device	
Select Device	
Device 1 (/dev/sis8	300-0)
	300-1)
Selected device infe	rmation
Type	SIS8300KU
Firmware Version Serial Number	0x83032010 123 0x22 > 125MHz 16 bit
ADC crip iD	

Select "Tools/FPGA programming menu" and the "FPGA programming menu" canvas will appear"

FPGA Flash Programmer 🛛 💿		
Update Control Select FPGA Image h/SIS/sis8300KU_top_v2010_elf_scope.bin		
Verify FLASH Program FLASH		
Update Status Current Process		
0%		
Exit		

SIS830x Root GUI / Tools / FPGA programming menu

SIS ROOT GUI V2.3 (15.10.2018) 😑 🗈 😣		
struck	Iools Help Register Read/Write FPGA programming menu Innovative Systeme	
Crate Information Device 1 (/dev/sis83 Device 2 (/dev/sis83	300-0) 300-1)	
Select Device	300-0)	
Device 2 (/dev/sis8	300-1)	
- Selected device info	mation	
Туре	SIS8300KU	
Firmware Version Serial Number ADC chip ID	0x83032010 123 0x32 -> 125MHz 16 bit	

Select the "..." button to get browser window to search for and select a FPGA image file (*.bin)

Start "Program FLASH"

FPGA Flash Programmer 🛛 🛞			
Update Control			
h/SIS/sis8300KU_top_v2010_elf_sco	Decembra El AQU		
Verity FLASH	Program FLASH		
Update Status Current Process			
0%			
<u> </u>			

SIS830x Root GUI / Tools / FPGA programming menu

elp

FPGA Flash Programmer 🛛 😣			
Update Control Select FPGA Image n/SIS/sis8300KU_top	_v2010_elf_sco	pe.bin	
Verify FLAS	H	Program FL	ASH
Update Status Current Process: Flashing successful			
	Exit		
	<u></u> /		

SIS830x Root GUI / Tools / Test / FFT



SIS830x Root GUI / Tools / Test / FFT



SIS830x Root GUI / Tools / Test / FFT







4. Dec. 2018 MicroTCA Beginners Tutorial



4. Dec. 2018 MicroTCA Beginners Tutorial





Thank you!

