Microelectronics and ASIC developments

IHP – Technology Department

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05.03.2019

"Matter and Technologies“, Helmholtz Institute Jena

innovations
for high
performance
microelectronics

IHP – Innovation for High Performance Microelectronics

Institute of the Leibniz Association

- 320 employees from 27 countries, including 134 scientists
- Founded in 1983 ➔ R&D 8“ pilot line since 2000
- Shareholder is the state of Brandenburg
- Member of the „Research Fab Microelectronics Germany“ (FMD) ➔ cooperation with Fraunhofer VµE & FBH

Financing 2017

- Basic funding from the German and local government: ~29 Mio. Euro (including basic invest)
- Third party funds: ~19 Mio. Euro (e.g. EU-Projects, MPW-LVP, FMD)

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IHP – Innovation for High Performance Microelectronics

Research programs

- Material Research
- More than Moore technologies
- Analogue circuit design for mm-wave & THz
- System design for broadband communication

IHPs Pilot line(s) for R&D & prototyping

IHP SiGe BiCMOS Pilot Line

Cleanroom area

- 1000m² class 1 for 100wspw

Technology & operation

- RF SiGe BiCMOS @ 24/7 mode

Technology level

- 8" @ 0.25µm and 0.13µm

IHP Wafer Bonding Pilot Line

- Temporary & permanent wafer bonding
- Metal bonding (wafer-level)
- Ultra-thin silicon BiCMOS technologies
- Wafer-level integration of microfluidics

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IHP Technology Department

MPW Service

Low Volume Production

Technology Service and Operation

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IHP SiGe-BiCMOS Technologies for MPW and LVP

Baseline BiCMOS Technologies

0.25µm CMOS → V_{dd}=2.5V

Dual-gate 0.13µm CMOS → V_{dd}=1.2V and 3.3V

SG25H4
f_t/f_{max}=180/220GHz

SG25H3
f_t/f_{max}=110/180GHz
$V_{breakdown}$ up to 7V

SGB25V
f_t/f_{max}=95/75GHz
$V_{breakdown}$ up to 7V

SG13S
f_t/f_{max}=250/300GHz
$V_{breakdown}$ up to 3.9V

SG13G2
f_t/f_{max}=300/500GHz

Qualified
(wrt JEDEC standards)

RF-LDMOS
Compl. and iNLDMOS
BV > 15V and f_T/f_{max}>10/30 GHz

Add-on Modules

pnp-HBT option
f_t/f_{max}=120/190GHz
$V_{breakdown}$ up to -2.5V

LBE, TSV, MEMS

Photonic SiGe-BiCMOS
f_t/f_{max}=180/200GHz
Ge-PD, MZM, WG, GC,…

RadHard SiGe-BiCMOS
RF-LDMOS, JIC-MOS
HP- & HV-HBT

In Development

SG25H5-EPIC
f_t/f_{max}=240/300GHz
Ge-PD, MZM, WG, GC,…

- W2W bonding & backside RDL
- RRAM in SiGe-BiCMOS
- SG13Gx (based on TARANTO)

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Service Approach → Multi Project Wafer & Prototyping & LVP

Customer A

Customer B

Customer C

200 mm Silicon Wafer

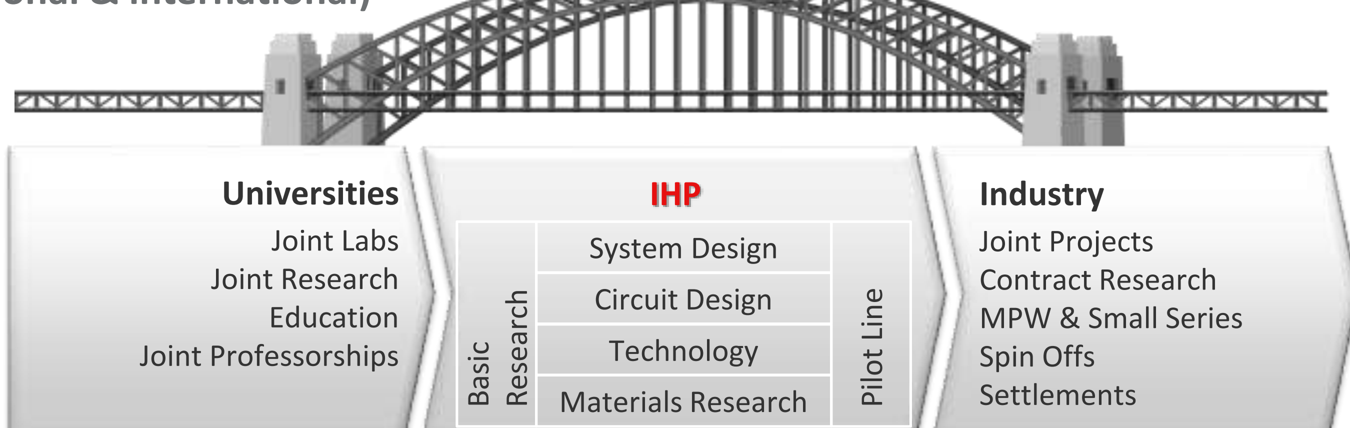
Internal and external customer layouts and structures for technology research (3-5 technologies in one mask set)

IHP as a Bridge between Universities and Industry

Academic cooperation

- Virtual laboratories between universities and IHP for exchanging scientist & know-how
- Enable access to R&D infrastructure
- Currently 9 runnig JointLabs

POZNAN UNIVERSITY OF TECHNOLOGY



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Summary of R&D Activities under Technology Department

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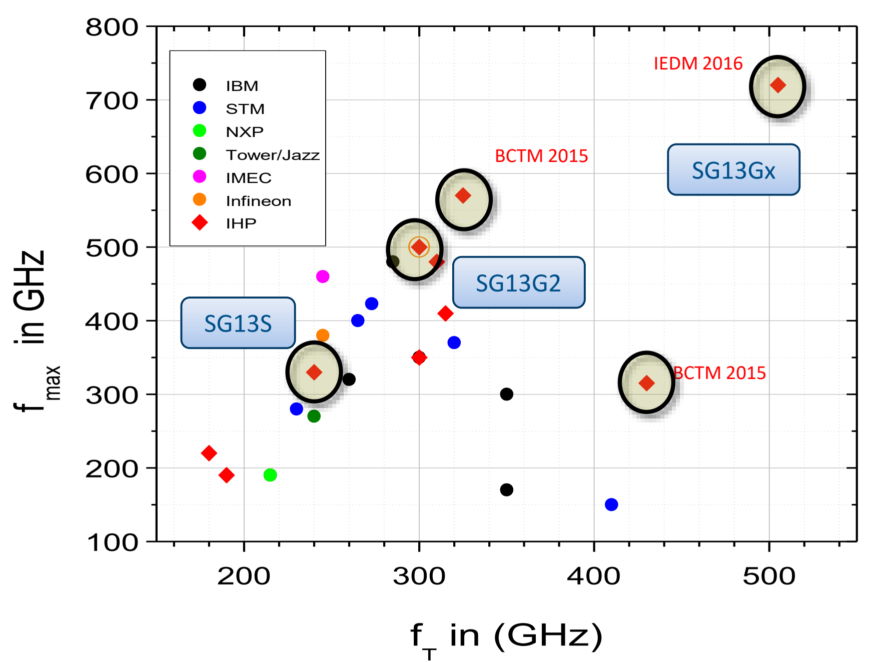
SiGe-HBT & BiCMOS Performance Evolution



DOT5 -> 500GHz Fmax

- **SG13G2 in production today**
- **Pushing the limit designs:**
  - ✓ 240 GHz RF chip-set + package (EuMW ,16)
  - ✓ 240 GHz radar transceiver + package + circular polarization (EuMC ’15)
  - ✓ 550 GHz full Si CT scanner (IRMMW-THz ‘16)

DOT7 -> 700 GHz Fmax

- Discrete HBT with f_T > 505 GHz and f_{max} ≈ 720 GHz (IEDM 2016)

TARANTO -> 600 GHz Fmax BiCMOS

- SG13Gx

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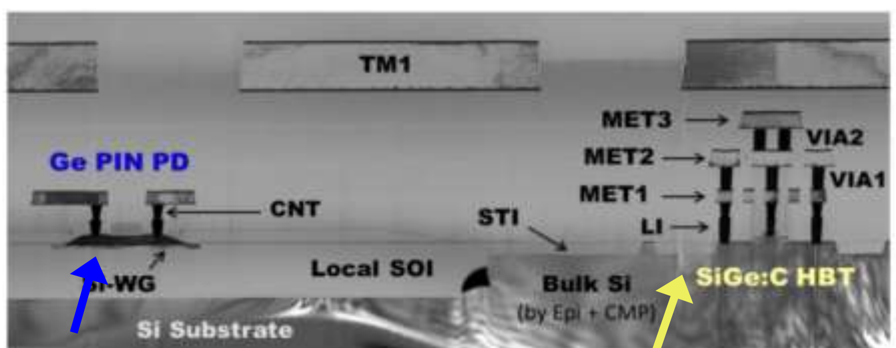
SG25 SiGe BiCMOS + Photonics

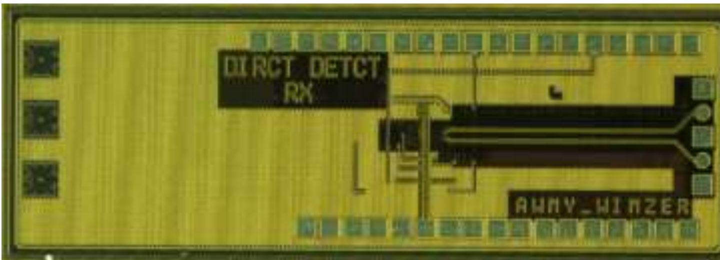


67 GHz Bandwidth Germanium Photo Diode

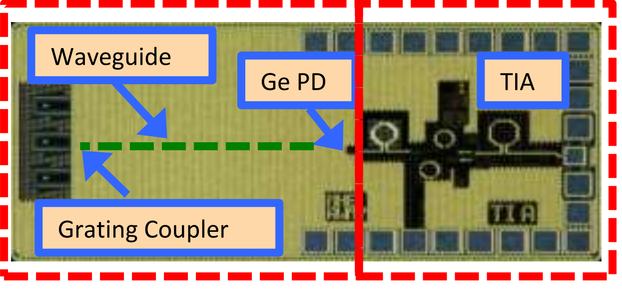
190GHz Ft SiGe NPN

Monolithic Photonic-Electronic

- Same Silicon wafer
  - Localized SOI areas for photonics
  - Bulk like areas for BiCMOS
- Full feature set BiCMOS
- Common BEOL and modular process flow
- Silicon Proven PDKs



56Gbps Data rate receiver for 400Gbit Ethernet
M.Kroh et al. ECOC 2016



54Gb/s silicon photonics receiver, M.H.Eissa et al. ESSCIRC 2016

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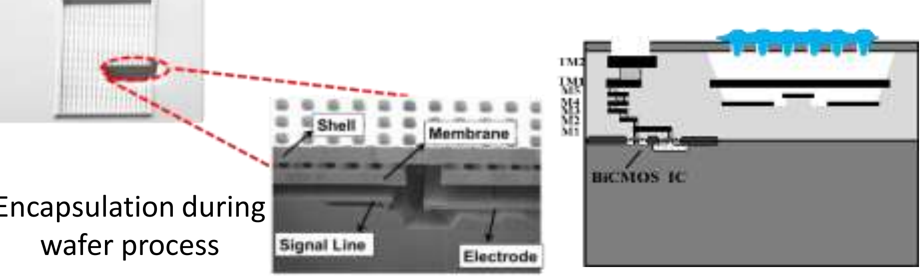
SG13 SiGe BiCMOS + RF-MEMS

- BEOL embedded RF-MEMS technology for mm-wave switches / varactors
- Low insertion loss (~0.7 dB) and high isolation from 30 GHz to above 150 GHz
- RF-MEMS packaging based on wafer-level encapsulation

RF-MEMS Switch Technology



Encapsulation during wafer process

Application Examples

140 GHz Active Imaging

- Tx/Rx Switches
- Phase Shifters
- Tunable Filters
- ....

90 GHz Passive Imaging

30 GHz SatCom

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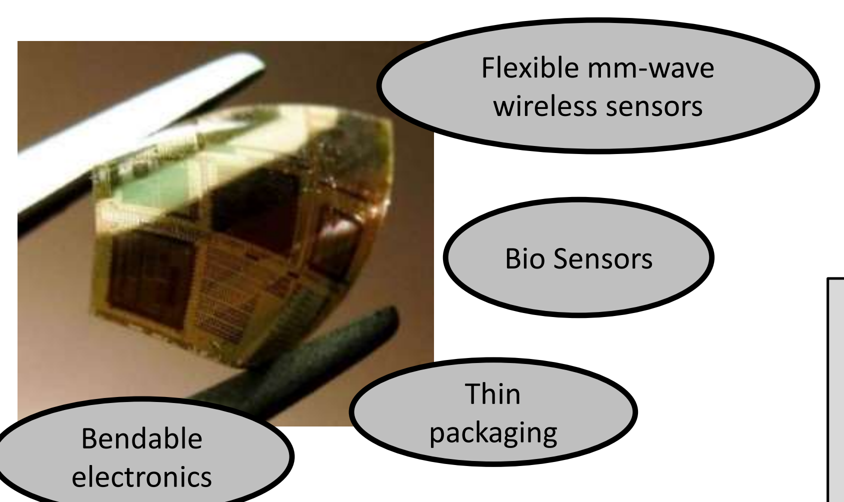
Ultra-Thin Silicon BiCMOS Technology

Fabrication	Standard delivery	Special delivery	Research
(~725 um)	(200 – 300 um)	(down to 100 um)	(down to 20 um)



30 um thickness of BiCMOS wafer

- Wafer thinning + stress release process
- Add. stress compensation layers
- Miniaturization (form factor)
- Shorter interconnections
- Heat dissipation (heatsink)

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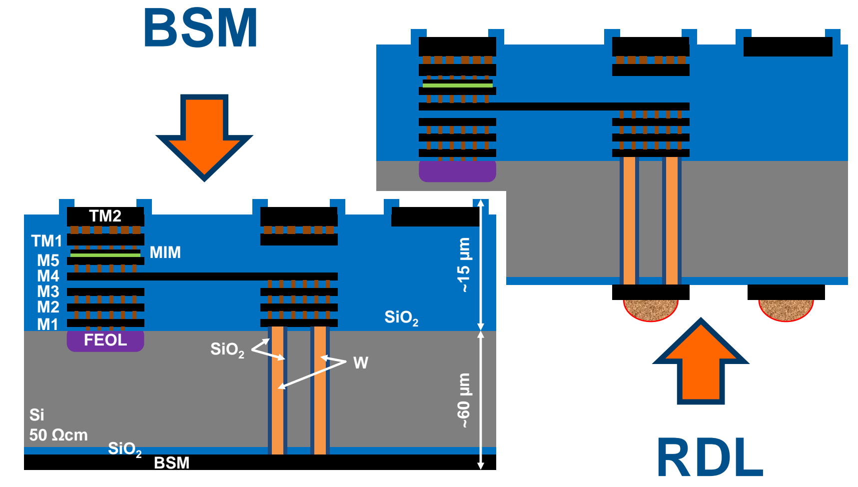
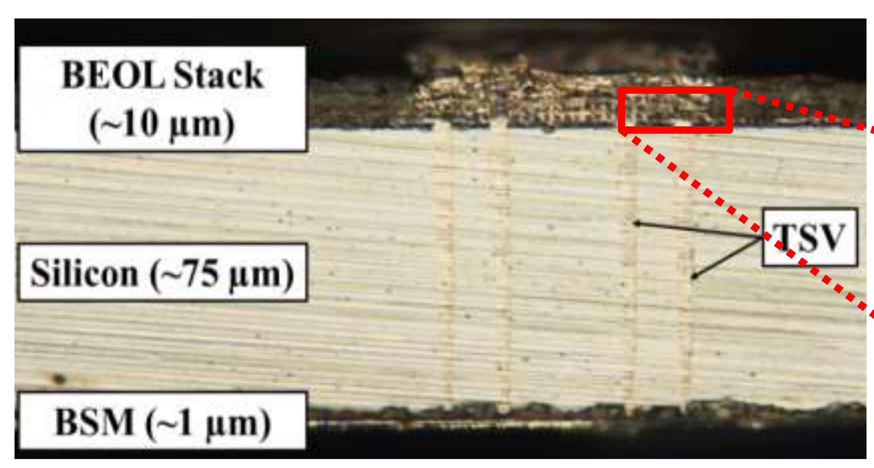
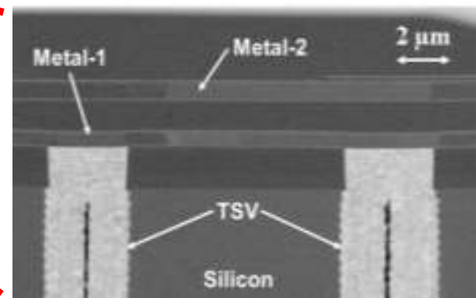
BiCMOS Embedded TSVs

Remove GND bond wires for chip-2-package interface

- Simplify packaging/assembly process
- Minimize parasitic inductance and resistance







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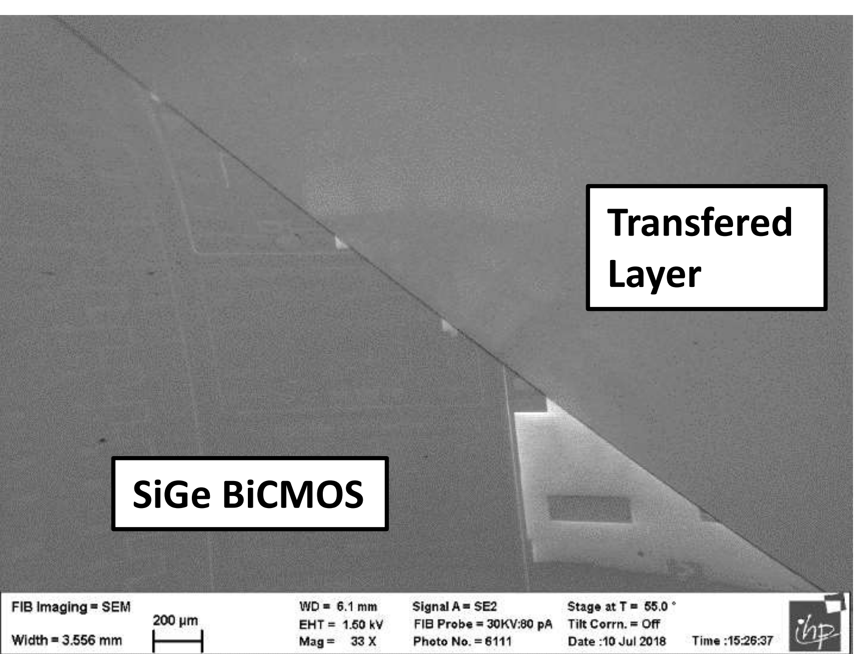
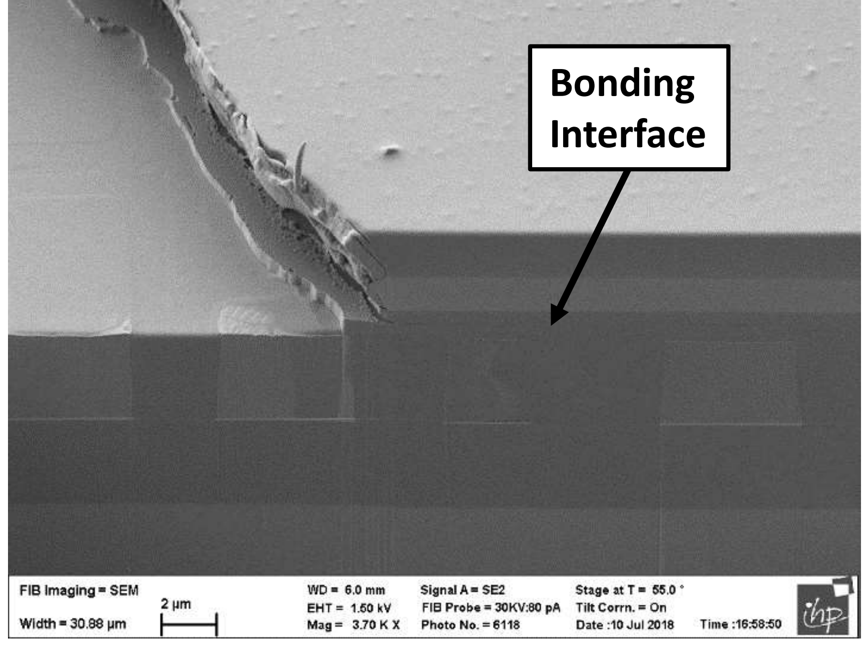
Layer Transfer Technology

- Layer transfer technology based on SiO_2-SiO_2 fusion bonding + backgrinding
- Development of basic process module for different applications (e.g. bolometer)





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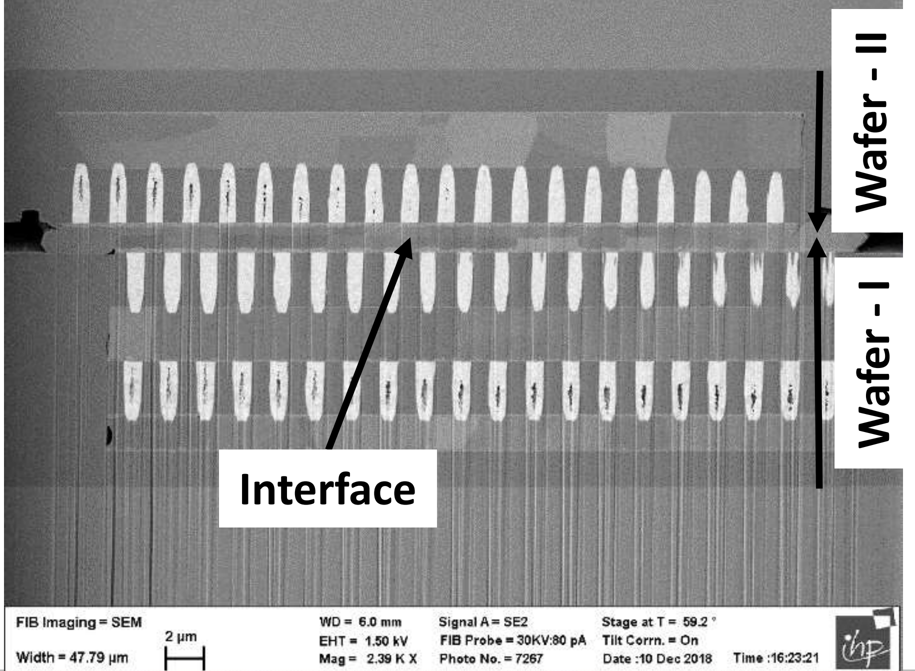
Al-Al Bonding Results - I

- Interconnections between wafers with very low ohmic contacts (specific contact resistance ~1.3e-7 Ohm*cm²)
- Initial process evaluation with yield ~85%



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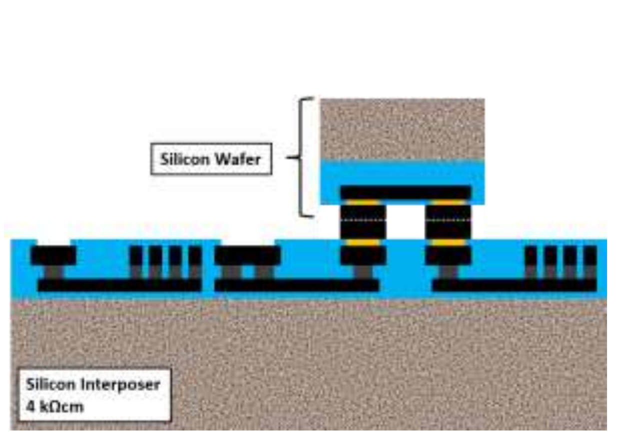
Wafer-Level Packaging Platform

- Fan-out wafer level packaging platform based on Al-Al bonding
  - Fan-out wafer-level packaging & Heterogeneous integration
- General proof of concept already done during Al-Al wafer bonding evaluation



SiGe BiCMOS Chipset

Interposer

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Cooperation Example

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The TT-PET project

A 3-year project started in march 2016 financed by the Swiss National Fund to produce a PET Scanner for small animals **based on silicon detector technology,** insertable in an MRI machine and with **30ps RMS time resolution**.

Participating institutes:

- University of Geneva Sensor ASIC design. Scanner assembly. Image reconstruction.
- University of Bern Read Out design and production. Flex design and production.
- Hôpitaux Universitaires Genève Image reconstruction. Scanner test.

In collaboration with:

- **IHP microelectronics**, INFN of Roma Tor Vergata, CERN - Ideasquare

- **Milestone 1**: A **monolithic** pixel detector with **100 ps** time resolution for MIPs and **large pixel size** to be used for TOF-PET applications.

- **Milestone 2:** A **monolithic** pixel detector with **sub-100 ps** time resolution for MIPs and **fine pixel size** to be used for high-energy and applied physics research.

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Read out geometry

The condition of “parallel plate” read out is fundamental to guarantee the uniformity of the weighting and the electric field.

470 μm

500 μm

D=80 μm

GND

$$I_{ind} = \sum_i q_i \, \vec{v}_{drift,i} \cdot \vec{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

Scalar, saturated

Scalar, uniform

Drawback!

Increase of the pixel capacitance Larger equivalent noise from the amplifier.

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The fast, low noise amplifier

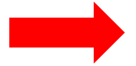
$$ENC^2 \propto \left(2q_e I_C + \frac{4kT}{R_P} + i_{na}^2\right) \cdot \tau + (4kTR_S + e_{na}^2) \cdot \frac{C_{in}^2}{\tau} + 4A_f C_{in}^2$$

Fast integrator

Dominating term: series noise ($\tau < 10\ ns$)

Minimization of series noise

Low input impedance of the transistor

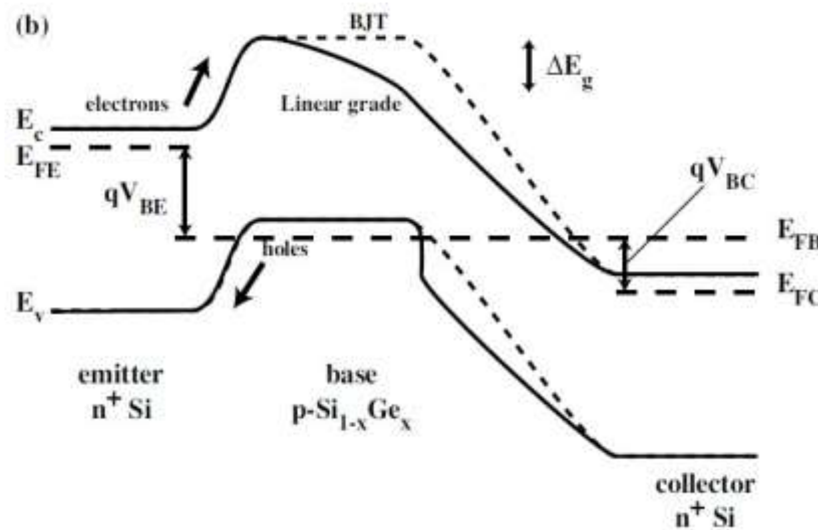


BJT technology

Maximize the current gain (at high frequencies!) while keeping a low base resistance

SiGe technology for low noise, fast amplifiers

A possible approach: **changing the charge transport mechanisms** in the base from diffusion to drift.



Introducing a drift in the base.

SiGe heterojunction bipolar transistor technology.

Our technology choice:

SG13S from IHP microelectronics

$\beta = 900$

$f_t = 250\ GHz$

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Target ASIC specifications

ASIC length	$24\ mm$
ASIC width	$7, 9, 11\ mm$
Pixel Size	$500 \times 500\ \mu m^2$
Pixel Capacitance (comprised routing)	$750\ fF$
Preamplifier power consumption	$< 0.8\ mW/mm^2$
Preamplifier E.N.C.	$600\ e^-\ RMS$
Preamplifier Rise time (10% - 90%)	$800\ ps$
Time resolution for MIPs	$100\ ps\ RMS$
TDC time binning	$20\ ps$
TDC power consumption	$< 1\ mW/ch$

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Sensor design

Simplified architecture for **large pixel size**.

FRONT END AND FAST-OR
PIXEL MATRIX
INSIDE THE GUARD RING
TDC, LOGIC AND I/O
FRONT END AND FAST-OR

- **SG13S technology** from IHP Microelectronics.
- N-on-P pixels.
- Substrate to ground.
- Positive high voltage to pixels.
- Signal routed to the front-end on the chip periphery.

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Sensor design

+ 200 V

+ 200 V

P+

P+

P+

N

N

Depletion depth: 80 µm

$E > 2\ V/\mu m$

P-substrate

$\rho = 1\ k\Omega \cdot cm$

GND

Integrated in standard IHP SG13S technology

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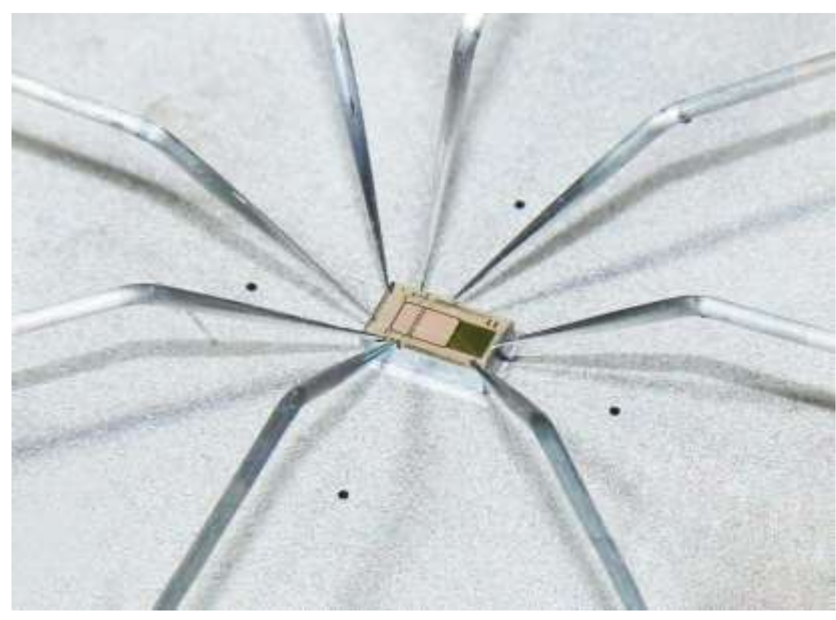
Concept prototype



December 2017

Monolithic chip: sensor + front-end.

- High wafer resistivity ($1\ k\Omega cm$).
- Breakdown voltage: above 160 V.
- Pixel size: $900\ \times\ 900\ \mu m^2$ and $900\ \times 450\ \mu m^2$.
- **No thinning, no backplane metallization.**

Beam Test with MIPs:

- **Time resolution: 200 ps.**
- **Efficiency 99.8%.**
- **Power consumption: 0.8 mW/mm².**

For more information:
L. Paolozzi *et al* 2018 *JINST* **13** P04015
doi: https://doi.org/10.1088/1748-0221/13/04/P04015

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Demonstrator layout

Guard Ring test structures

Front End + Fast OR

TDC

- 3×10 matrix, $500 \times 500\ \mu m^2$ pixels.
- Preamplifier, discriminator, 50 ps binning TDC, logic, serializer integrated in chip.
- Thinned to 100 µm. Depletion depth 80 µm.
- Full backside processing.

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Beam test with MIPs at CERN SPS

For more information:
arXiv:1811.11114

Chip 2
Chip 1
Chip 0

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Efficiency

Chip 1

Y [μm] \ X [μm]	0–500	500–1000	1000–1500	1500–2000	2000–2500	2500–3000	3000–3500	3500–4000	4000–4500	4500–5000
1000–1500	$100.0^{+0}_{-0.1}$	$100.00^{+0}_{-0.05}$	$100.00^{+0}_{-0.03}$	$99.99^{+0.01}_{-0.04}$	$100.00^{+0}_{-0.01}$	$99.99^{+0.01}_{-0.02}$	$100.00^{+0}_{-0.01}$	$100.00^{+0}_{-0.01}$	$99.96^{+0.01}_{-0.02}$	masked
500–1000	$100.0^{+0}_{-0.1}$	$100.00^{+0}_{-0.04}$	$100.00^{+0}_{-0.03}$	$99.99^{+0.01}_{-0.03}$	$99.99^{+0.01}_{-0.03}$	$100.00^{+0}_{-0.01}$	$99.99^{+0.01}_{-0.01}$	$99.99^{+0.01}_{-0.01}$	$99.96^{+0.01}_{-0.02}$	masked
0–500	$100.0^{+0}_{-0.5}$	$100.0^{+0}_{-0.2}$	$100.00^{+0}_{-0.04}$	$99.98^{+0.02}_{-0.05}$	$100.00^{+0}_{-0.03}$	$99.99^{+0.01}_{-0.02}$	$99.99^{+0.01}_{-0.02}$	$99.98^{+0.01}_{-0.02}$	masked	masked

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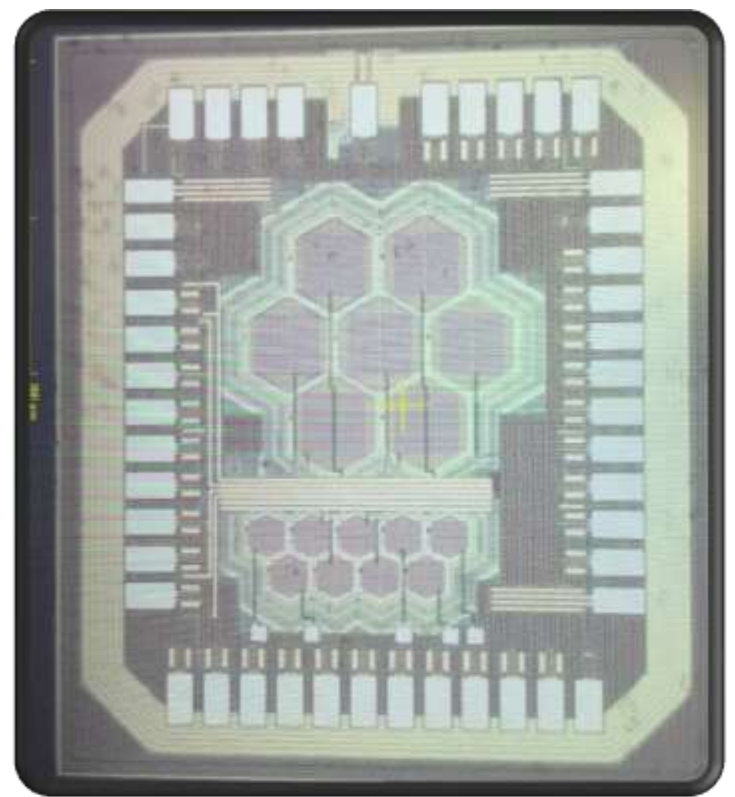
Target: sub-100ps resolution



Test prototype – IHP SG13G2 technology:

- Insulated HBT designed with IHP microelectronics and characterized in foundry.
- High voltage: breakdown at -200 V.
- Electronics fully functional.
- Data taking in progress.

JICG CMOS and JIC LDMOS – A Radiation Hardening by Design ASIC Approach for Applications in Extreme Environments

Outline

- Introduction
- Goals
- JICG CMOS
  - TID Reduction
  - SEU Reduction
  - TID and SEUTest
- Performance Test
- 250 nm JIC LDMOS
- 130 nm JICG CMOS
- Summary and Conclusions

Introduction

- Commercial processor circuits today fabricated in 14-nm technologies
- CMOS technologies for radiation-hard applications are always several generations behind most advanced CMOS technologies
- Advanced SOI FinFET technologies being discussed as most promising candidates for radiation hardness in terms of SEU and TID
  - Very small amount of collected charge after a particle impact improves SEU hardness ,small backside TID effects, high speed, low power, but in aero space applications and high energy physics experiments (HEP) only small volume of devices is required → not affordable for civil applications
- In HEP experiments 250nm bulk CMOS technologies replaced by 130 nm CMOS, 65 nm technologies are currently under evaluation (TID issues !?)
- 130 nm bulk CMOS stays further in the game, mature, robust, low cost

Goals

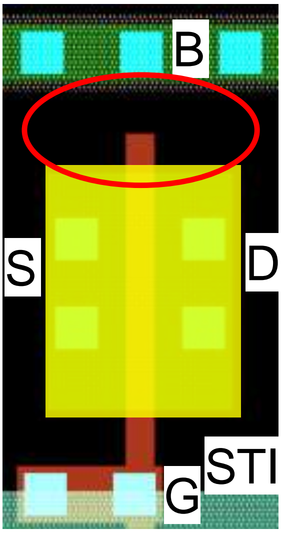
- Improve the radiation tolerance of CMOS transistors in IHP's 250nm and 130nm SiGeC BiCMOS technologies to meet requirements in HEP experiments as a worst case scenario
- Find a radiation hardening by design (RHBD) approach taking into account both total ionizing dose (TID) effects and single event upsets (SEU)
- Evaluation of JICG CMOS and JIC LDMOS test circuits in IHP's 250 nm SiGeC BiCMOS technology
  - Verification of TID and SEU radiation hardness
  - Evaluation of device performance
- Transfer of results into 130nm technology
  - Evaluation of extra effort for forming of S/D extension and halo implants and slicide blocked areas

JICG CMOS

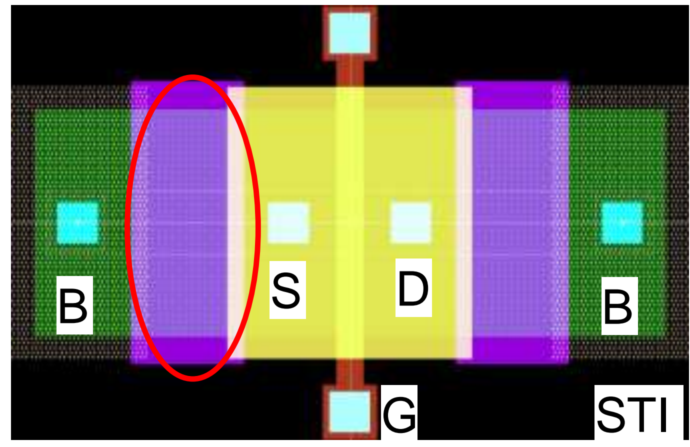
- Suppress TID induced source drain leakage by junction isolated (JI) of source drain regions, form silicide blocked well regions
- Avoid SEU induced malfunctions of digital cells suppressed by a redundancy on transistor level, each MOS transistor is replaced by a stack of two locally separated single transistors which share a common gate (CG)

JICG CMOS - TID Reduction

- **Efficient draw off of majority excess charge carriers to the body contact**
  - Well sheet resistance near and in source region determines turn on behavior of parasitic bipolar transistor



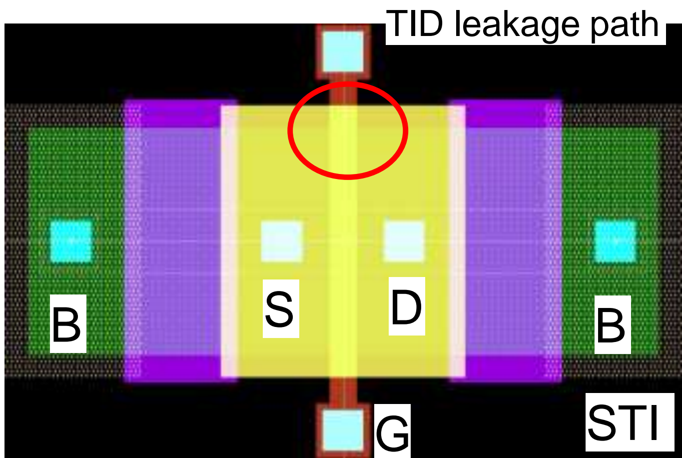
Source/drain-body isolation from body via STI, well sheet resistance high



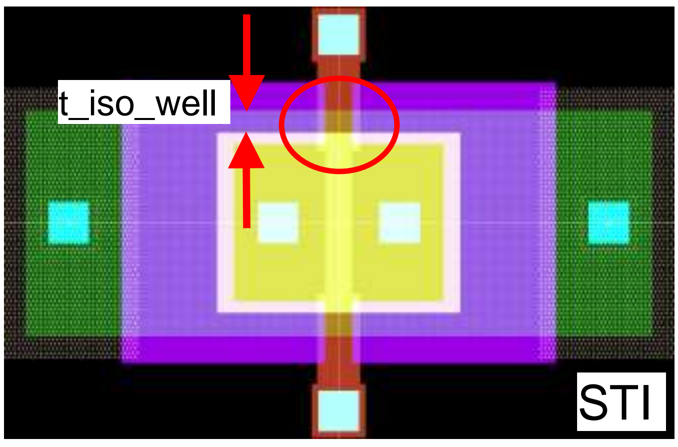
Source/drain-body isolation from body via silicide blocked region in ACTVE, well sheet resistance low

JICG CMOS - TID Reduction

- **TID: Complete junction isolation of source/drain regions**



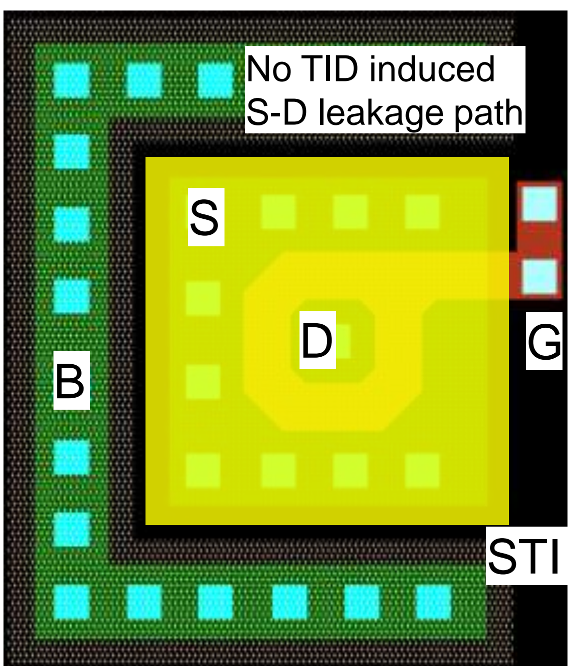
TID related source drain leakage due to positive fixed charges generated in the STI region of the MOS inversion channel



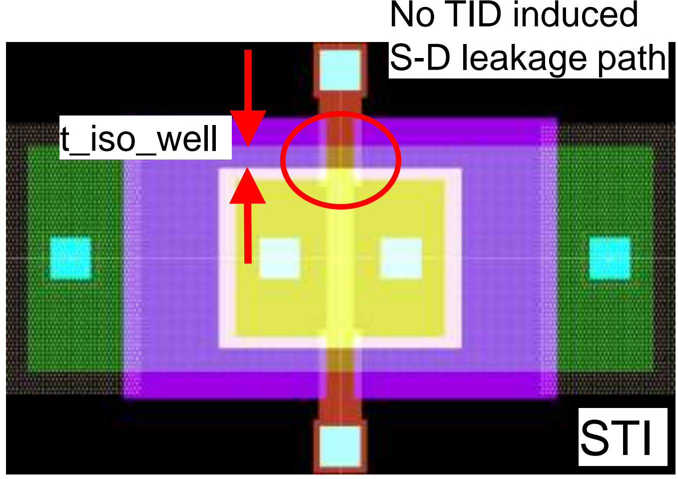
Additional lateral junction prevents TID related source drain leakage due to positive fixed charges generated in the STI region of the MOS inversion channel

JICG CMOS - TID Reduction

- **TID: JI MOS transistor vs enclosed layout transistor (ELT)**



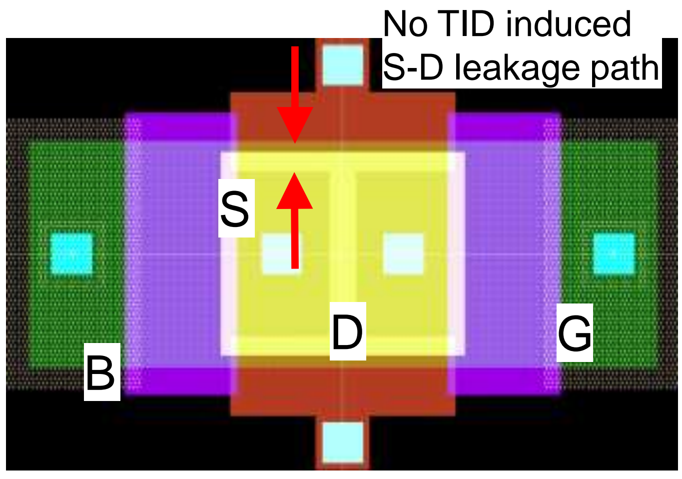
Commonly used ELT to suppress TID related source drain leakage

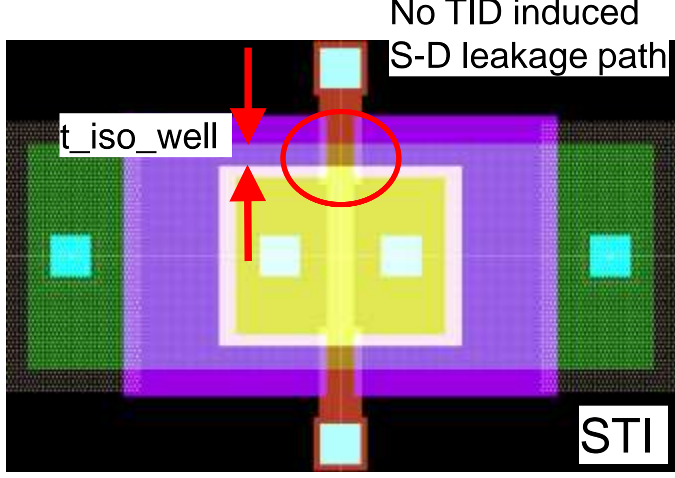


JI MOS as a symmetrical device enabling a minimum gate width. But also with additional gate body capacitance.

JICG CMOS - TID Reduction

- **TID: JI MOS transistor vs MOS transistor with dog bone gate**



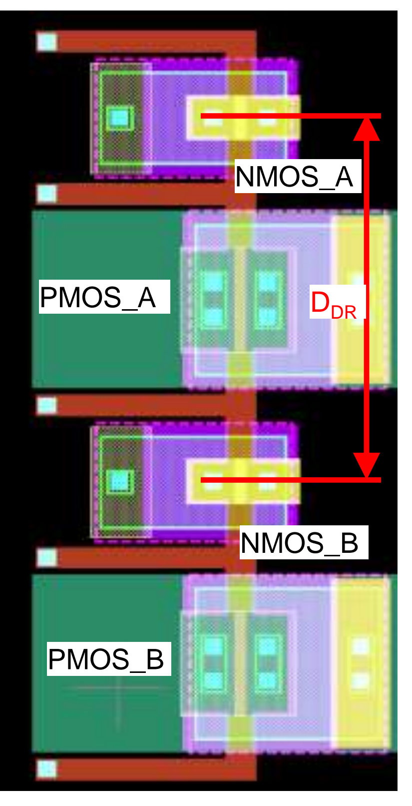


Dog bone gate MOS transistor with a large additional gate body capacitance drastically reduces CMOS switching speed.

JI MOS transistor also with additional gate body capacitance. Challenge for SALBLOCK litho !

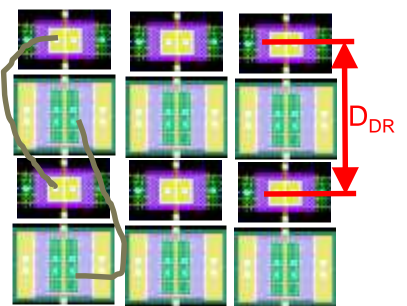
JICG CMOS - SEE Reduction

- **SEU: Avoiding SEUs by redundancy on transistor level**



- Stack of two locally separated MOS transistors A and B which share a common gate maintain the blocking capability of any NMOS and PMOS branch in a CMOS circuit after an impact of a high energetic particle
- Critical design value in the layout is the geometrical distance of the drain regions of the two MOS transistors D_{DR},
- D_{DR} must be great enough so that the generated electron hole pairs along the impact trajectory in one transistor does not affect the blocking capability of the second transistor
- Alternating arrangement of NMOS_A/PMOS_A/NMOS_B/PMOS_B in vertical direction gives a sufficiently great distance D_{DR} between the stacked transistor pairs.

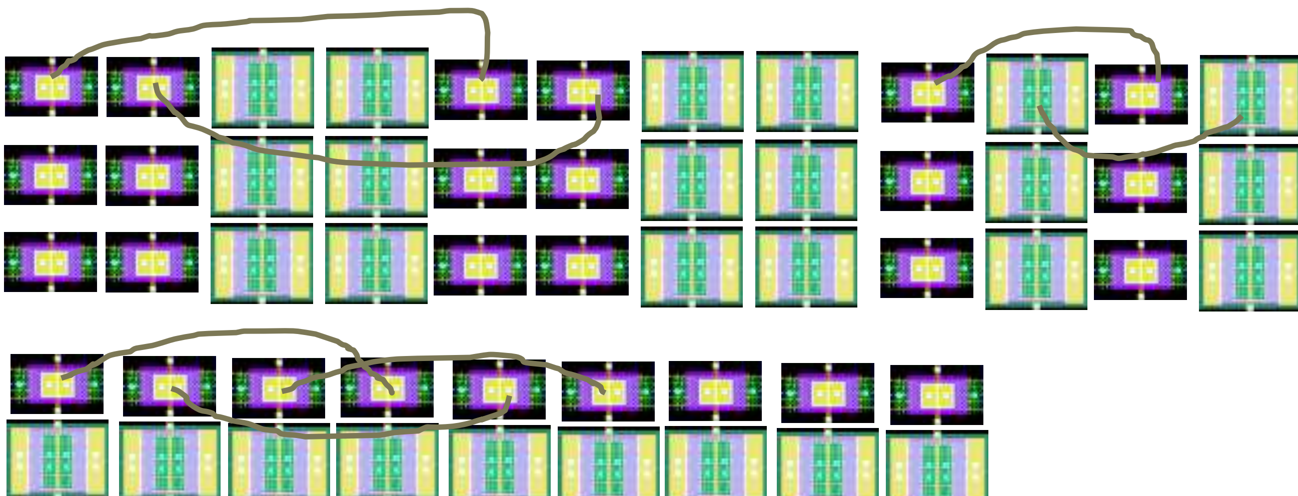
JICG CMOS - SEE Reduction



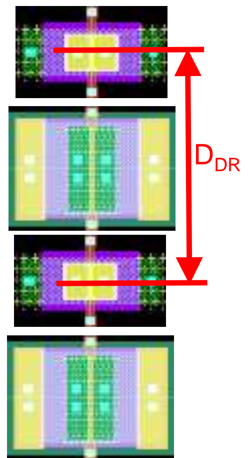
- **SEU hardening challenges at arrangement of MOS transistor pairs with common gates**
  - Requirements for the layout :

  Minimum area consumption for arrangement of transistors and their wiring

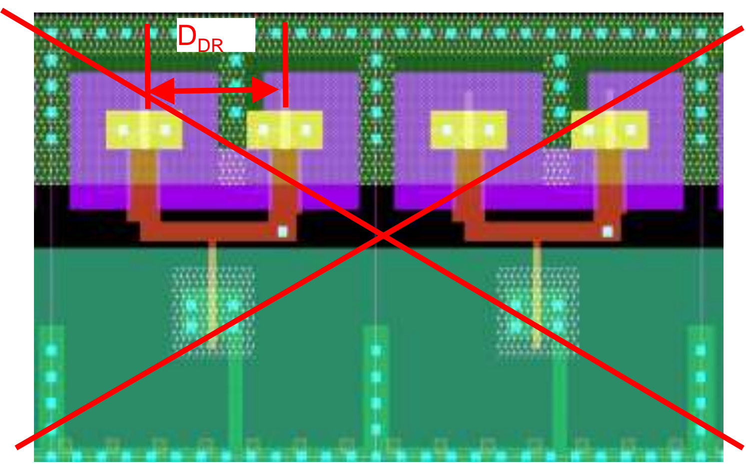
  Ensure sufficient minimum distance d_{DR}



JICG CMOS - SEE Reduction



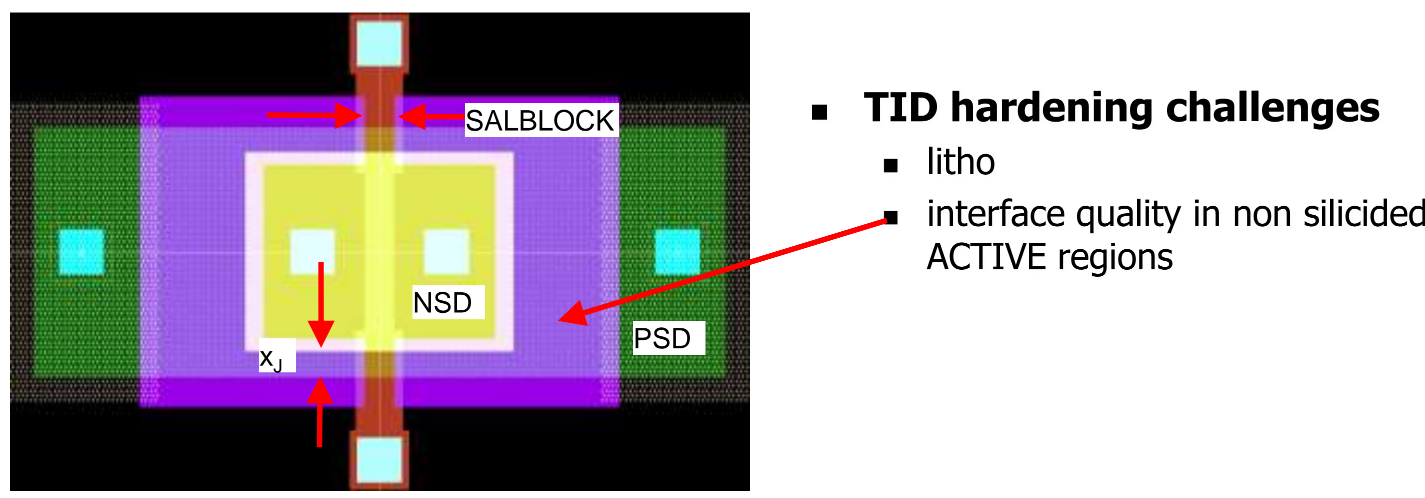
No events detected for
LET> 120 MeV cm2/mg



Events detected @
LET< 62 MeV cm2/mg

Ensure sufficient minimum distance of source drain regions D_{DR}

JICG CMOS -TID Reduction



- Challenging overlay and CD requirements for NSD, PSD and SAL masks
- For 0.13µm and below, special effort for halo and LDD mask sequence
- TID hardening approach via silicide blocker mask verified in IHP’s 0.13µm SG13S technology, feasible up to 65 nm technology node
- But there are new radiation damage issues in 65 nm technologies with trapped charges in spacers which cause depletion of LDD regions …

JICG CMOS - TID and SEU Test

Long inverter chain with 720 single inverters as simple test device for TID, SEU and performance tests

- NMOS transistor gate width 1 μm, PMOS gate width 2.3 μm

- **TID testing**
  - devices were irradiated using a Co-60 source for all inverters V_{DD} = 2.5V was applied, inverter chain input was set to 0V → the gates of one half of all inverters are biased with 0 V, where the gates of the other half are biased with V_{DD}=2.5V (gives maximum of trapped positive charge at STI/silicon interface).

JICG CMOS – TID and SEU Test

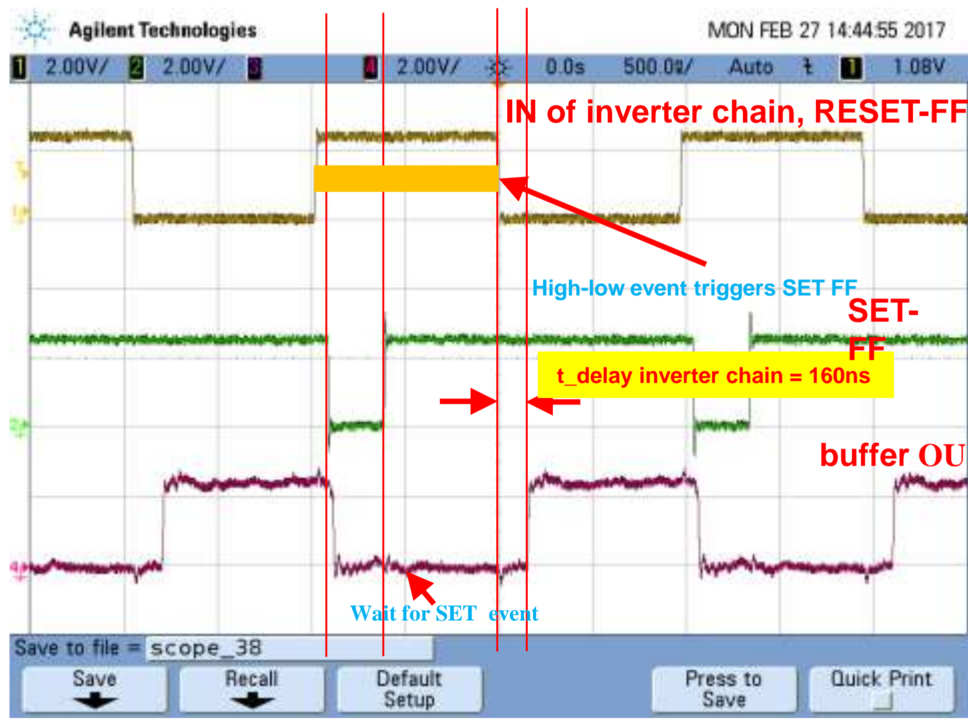
Long inverter chain with 720 single inverters as simple test device for TID, SEU and performance tests

- NMOS transistor gate width 1 µm, PMOS gate width 2.3 µm

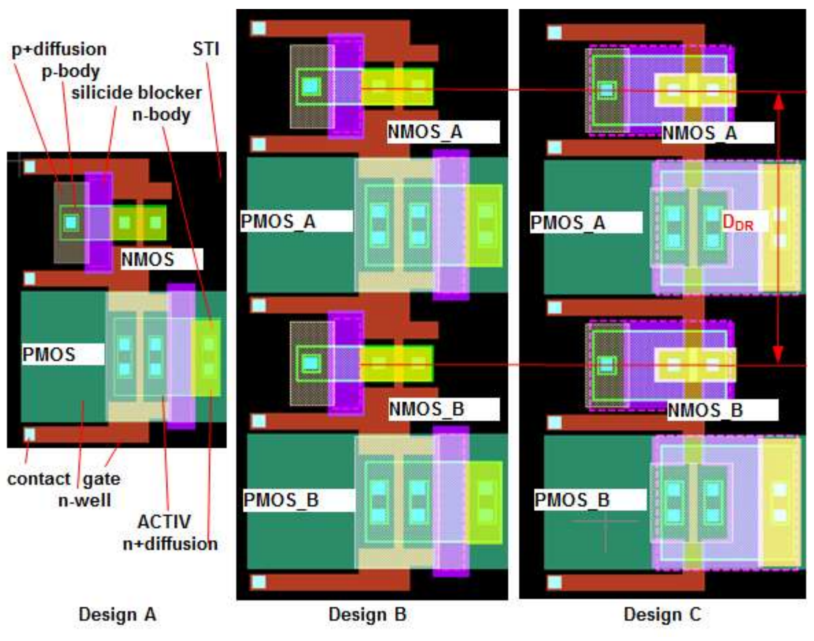
- **SEU testing**
  - last stage of inverter chain is connected to the RESET input of a RS latch
  - output of the RS latch drives an output buffer to drive a 50 Ohm output impedance
  - RS latch catches any propagated SET event during the irradiation with high energetic particles
  - Convenient counting of events in separated counter
  - Once one event is detected the test setup sets again the RS latch, so the setup is ready for counting the next propagated SET event

JICG CMOS– Switching Performance

- **Switching performance test**
  - Determination of gate RC delay and dynamic power loss



JICG CMOS - Designs



3 inverter designs for testing of

- **TID induced S/D leakage**
- **Propagated SEU events**
- **Switching performance**

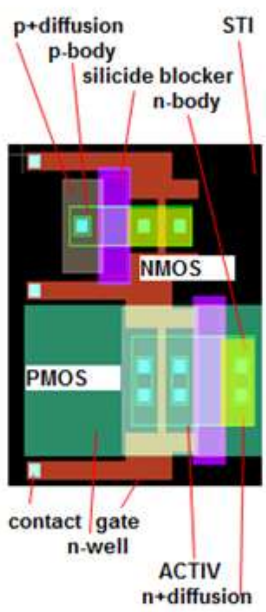
Design A:standard CMOS inverter without improved radiation hardness

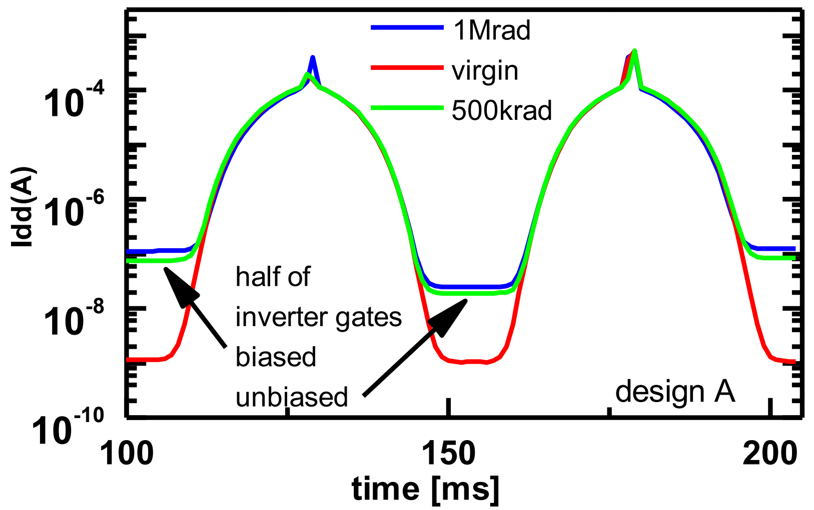
Design B:standard CMOS inverter with improved SEU radiation hardness by redundancy on transistor level.

Design C:improved TID and SEU radiation hardness by junction isolated NMOS and PMOS transistors and redundancy on transistor level.

JICG CMOS - TID Test

- Standard CMOS Inverter as reference
  - Different bias for each half of inverters

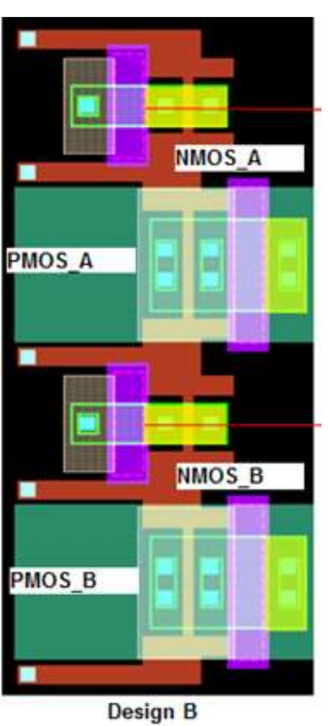


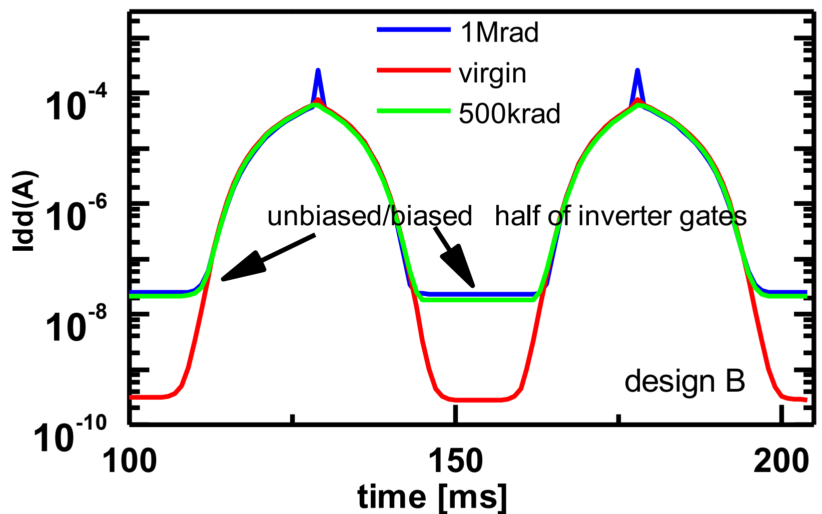


$1.1x10^{-7}$ A total leakage current after 1Mrad TID
360+24+2 =386 inverter stages with high at output
→**2.8x10-10 A leakage current per inverter**

JICG CMOS - TID Test

- Inverter with SEU protection elements only





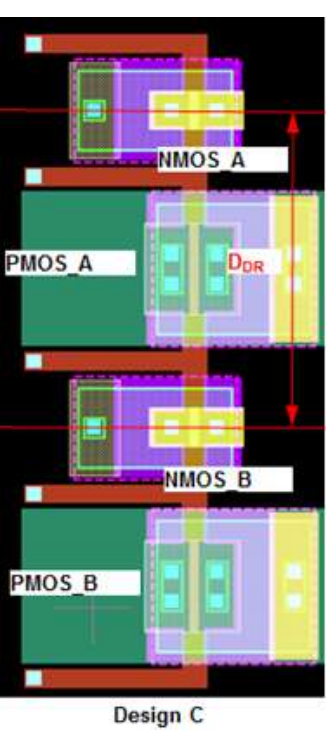
2.5×10^{-8} A total leakage current after 1Mrad TID

360+24+2 =386 inverter stages with high at output

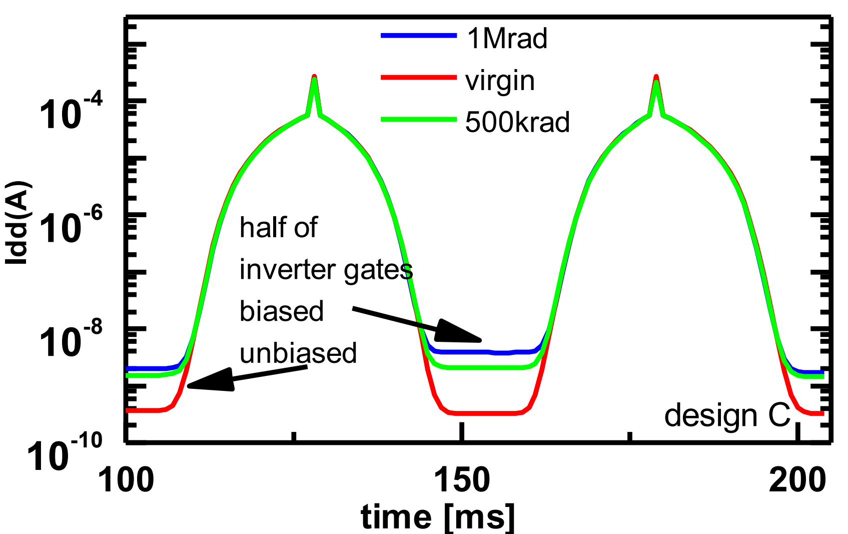
→6.5×10^{-11} A leakage current per inverter

JICG CMOS - TID Test

- Inverter with TID and SEU protection construction elements



Design C

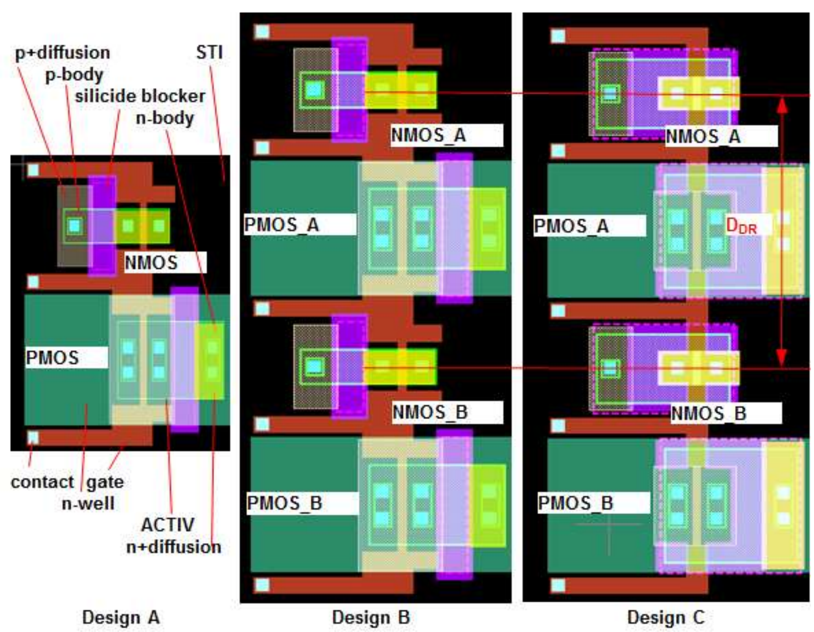


$4x10^{-9}$ A total leakage current after 1Mrad TID

360+24+2 =386 inverter stages

→**$1x10^{-11}$ A leakage current per inverter**

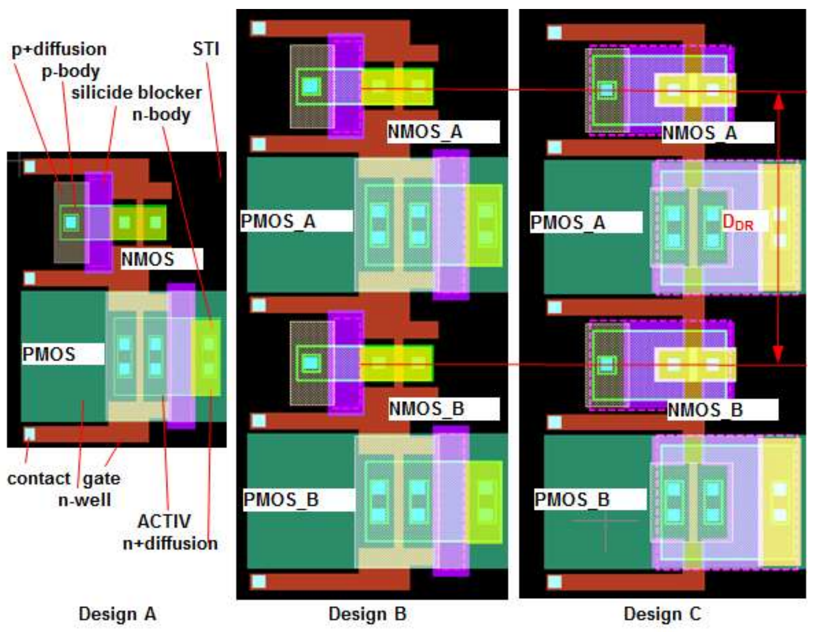
JICG CMOS - SEU Test



- SEU tests with high energy heavy ions 124Xe35+ ions (E=995MeV)
- three tilt angles 0°, 45° and 60° corresponding to LET values of 62.5, 88.3 and 125 MeV cm^2 mg^{-1}
- particle fluence 6.4 10^{6}cm-2.

- Standard inverter design A,
  - 13 events at LET=62.6 MeV cm2 mg-1
  - 40 events at LET=88.3 MeV cm2 mg-1
  - 65 events at LET=125 MeV cm2 mg-1
- Designs B and C
  - no events at all up to the maximum available LET value of 125 MeV cm^2 mg^{-1}
- no SEL events for all designs A,B and C

JICG CMOS Performance



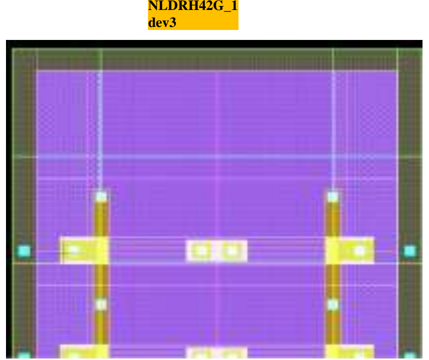
SEU testing of JICG shift registers in March 2019

- Gate delay time per inverter | dynamic power loss
  - design A: 82 ps | 149 µW/MHz
  - design B: 180 ps | 186 µW/MHz
  - design C : 220 ps | 221 µW/MHz

JIC LDMOS

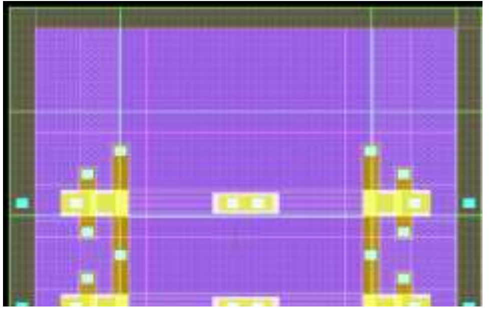
- **Supression of TID induced leakage**

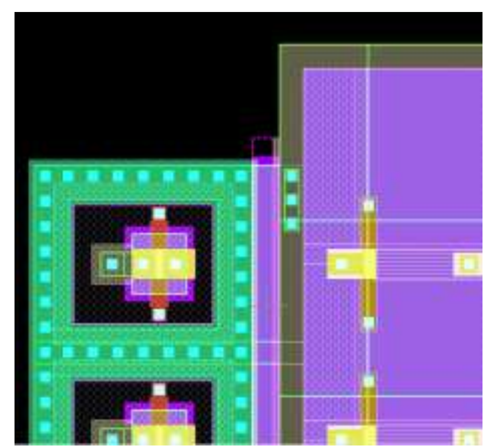
NLDRH42G_1
dev3



- **Supression of TID induced leakage and SEB**

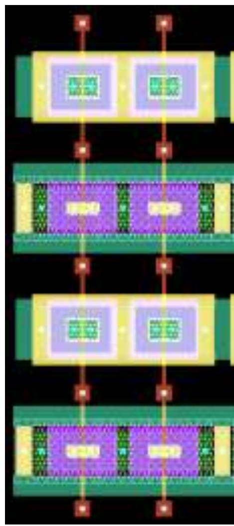
MNLDRH42G
dev1

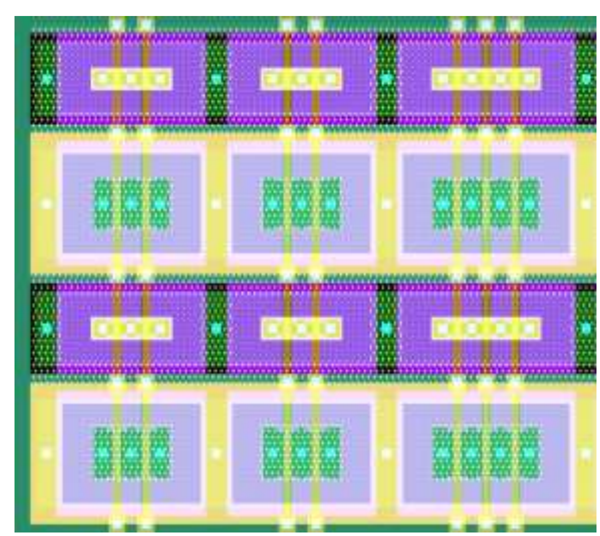




- Additional lateral junction prevents TID related source drain leakage due to positive fixed charges generated in the STI region of the MOS inversion channel
- Cascode arrangement (MOS/NLDMOS or IMOS/NLDMOS) effectively increases SEB onset volatage from 14 V to 4 V
- Common gate arrangement shows significant decrease of RF performance in terms of f_t and f_{max}

130 nm JICG CMOS



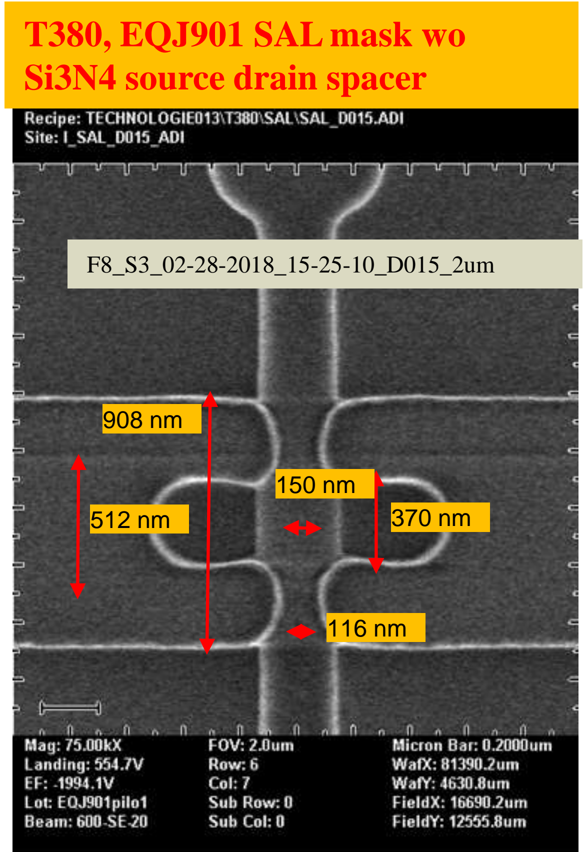


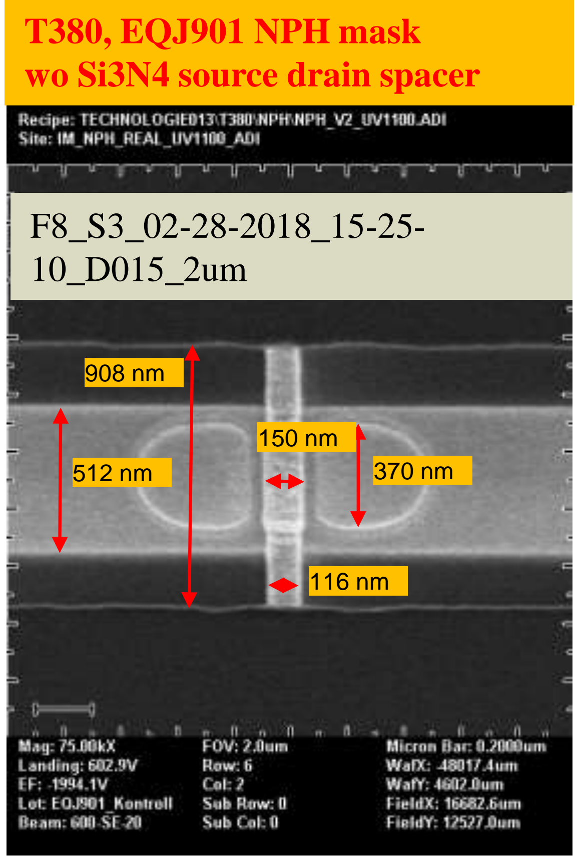
- 130 nm JICG Inverter chain SEU test shows no events for LET > 120 MeV cm2/mg
- 130 nm JICG Shift register for SEU testing currently in preparation

Supression of TID induced leakage and SEU

- Redundancy on transistor level, stack of two locally separated MOS transistors which share a common gate maintain the blocking capability of any NMOS and PMOS branch in a CMOS circuit after an impact of a high energetic particle
- Alternating arrangement of isolated NMOS and PMOS transistors in vertical direction gives a sufficiently great distance between the stacked transistor pairs
- Each transistor with dedicated guard ring
- Highly effective conduction of well currents to body contacts inhibits turn on of parasitic bipolar transistors

130nm JICG CMOS – SAL





Summary & Conclusions

- A novel RHBD design approach suitable for applications in harsh radiation environment based on bulk CMOS technologies has been verified in 250 nm technology node
- JICG CMOS inverter test circuits fabricated in a 0.25µm SiGeC BiCMOS technology show excellent radiation hardness in terms of TID and SEU
- The new bulk CMOS RHBD approach is capable to significantly suppress TID and SEU induced malfunctions for combinational and sequential digital circuits
- In comparison with standard CMOS inverters JICG CMOS inverters require a doubled chip area and show a decrease of switching speed by a factor of 0.37 and an increase of dynamic power loss by a factor of 1.48
- Extra litho effort for TID hardness in 130 nm CMOS technology
- SG13RE technology module of SG13S technology will include JICG CMOS and JIC LDMOS devices
- JICG SRAM in preparation

Thank you for your attention!

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