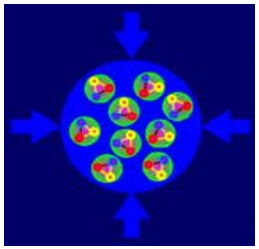
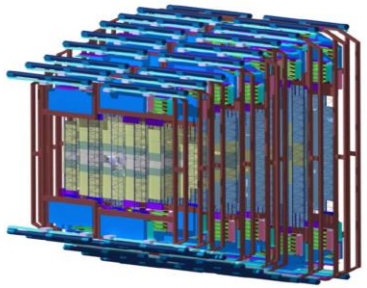


CBM

STS



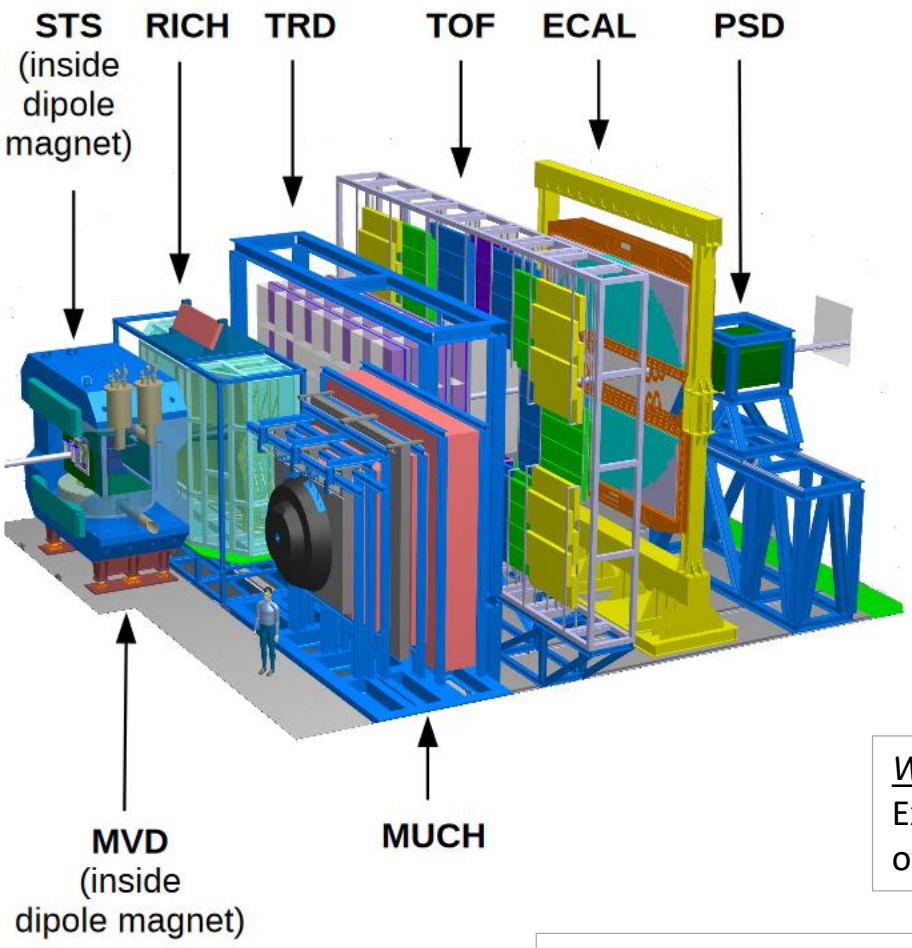
Quality Assurance Tests of The STS Read-out Electronics for The CBM Experiment

Merve Dogan, Adrian Rodrigues Rodriguez, Christian J. Schmidt

5th Matter and Technology Meeting, Jena 2019

FAIR

GSI



- **Dipol Magnet:**bending charged particles trajectories
- **Silicon Tracking System:**charged particle tracking
- **Micro-Vertex Detector:**secondary vertex reconstruction
- **Ring Imaging Cherenkov:** pion identification
- **Transition Radiation Detector:**electron identification
- **Time of Flight Detector:**hadron identification
- **MUon Chambers:**muon identification
- **Electromagnetic CALorimeter:** electron/photon identification
- **Projectile Spectator Detector:** collision centrality and reaction plane determination

What will be obtained

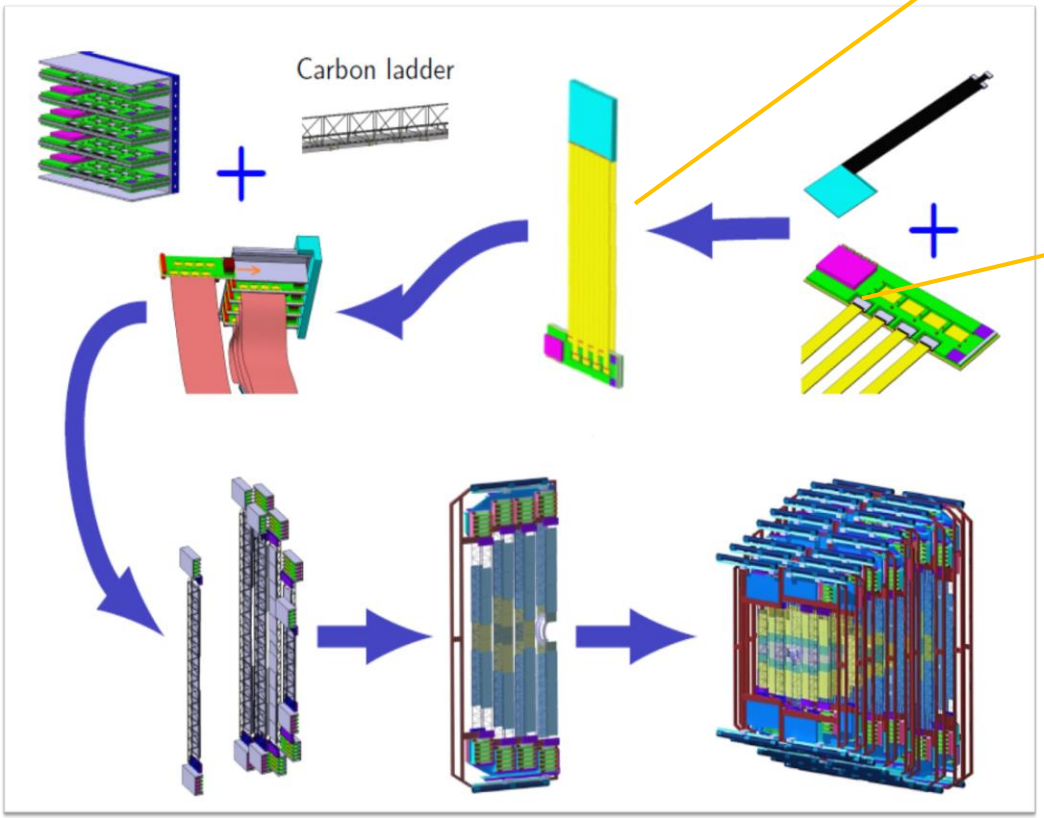
Exploration of the QCD phase diagram in the region of very high baryon densities

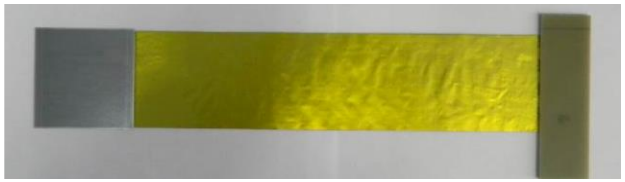
Requirements

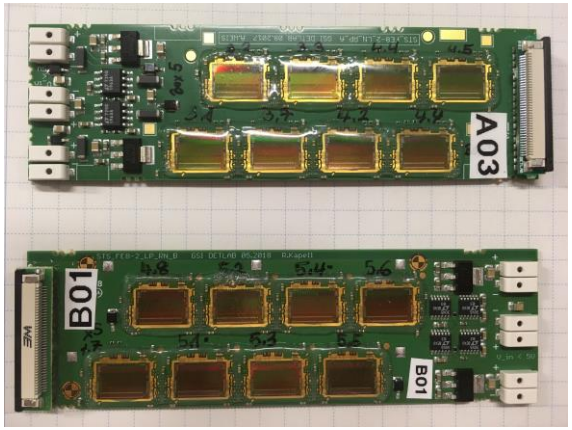
- High event rates: up to 10 MHz Au+Au reactions/seconds
- Self-triggering front-end electronic
- high-speed data processing
- Radiation hard detectors and front-end Electronics

Silicon Tracking System

- 896 modules
  Totally 106 ladders and 8-10 modules per ladder



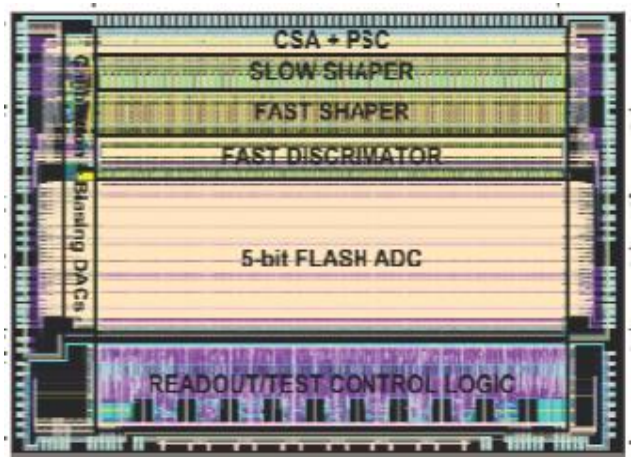




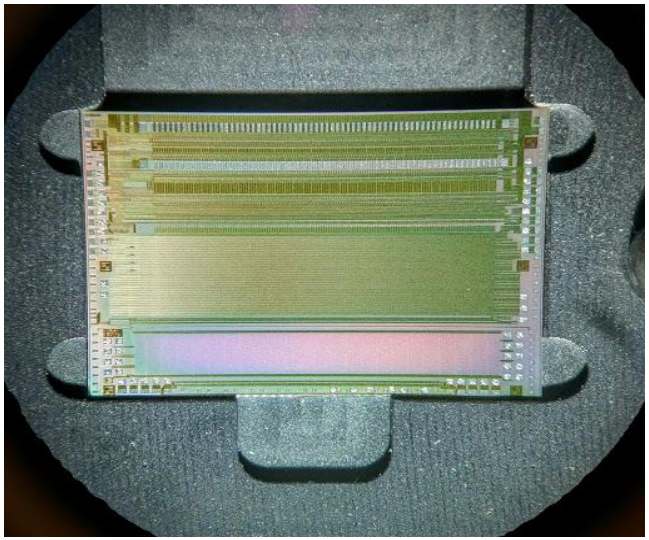
- 8 tracking station between the angle $2.5° \leq \Theta \leq 25°$
- Self-triggering electronics
- double-sided silicon microstrip sensors
- hit spatial resolution $\approx 25\ \mu m$
- $\Delta p/p \approx 1.8\%$
- Inside 1 Tm dipole magnet
- hit reconstruction eciency > 98%

Read-Out Electronics

STS-XYTERv2.0 (STS X,Y coordinate + Time and Energy Resolution)



STS-XYTER version 2.1 is now available and under test

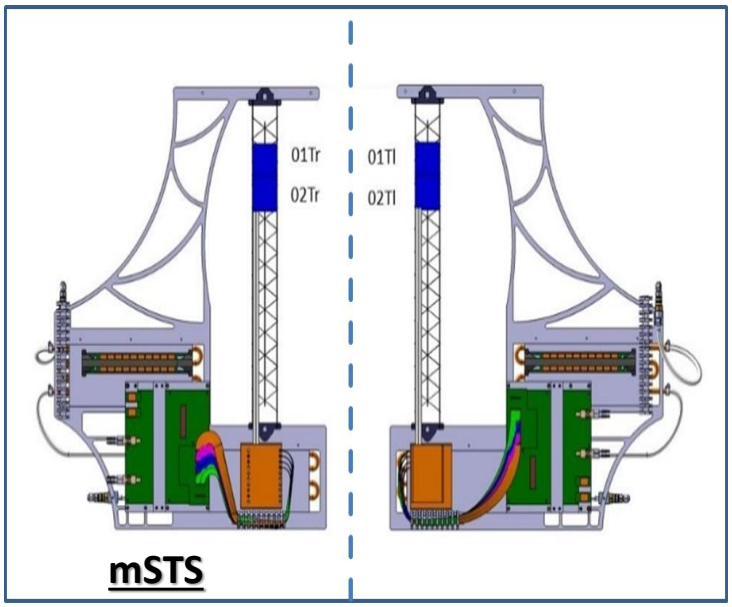


- 128 channels+2 test channels
- Chip size: approximately 10 mm x 6.7 mm
- Radiation-hardened design
- Energy and time measurement
- Time resolution < 5ns
- 5 bit flash ADC/channel dynamic range: 14fC
- Digital back-end compatible with the CERN-GBTx data concentrator

MOTIVATION:

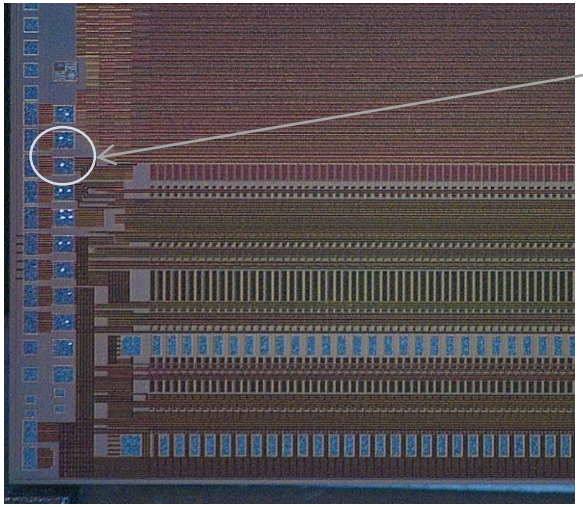
Test and QA of STS-XYTER v2 and prototype FEBB for module production and FEB assembly

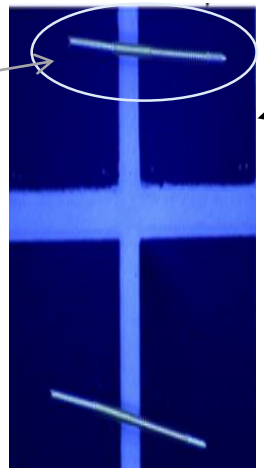
FAIR Phase 0: mCBM and mSTS

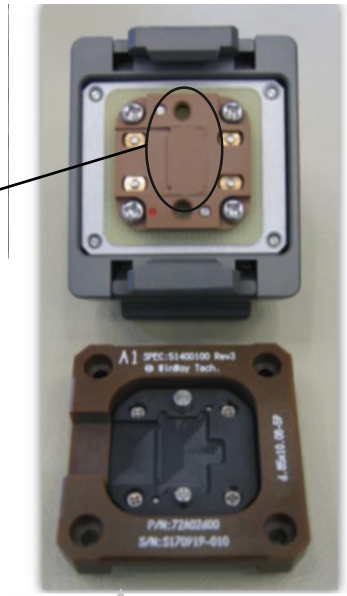


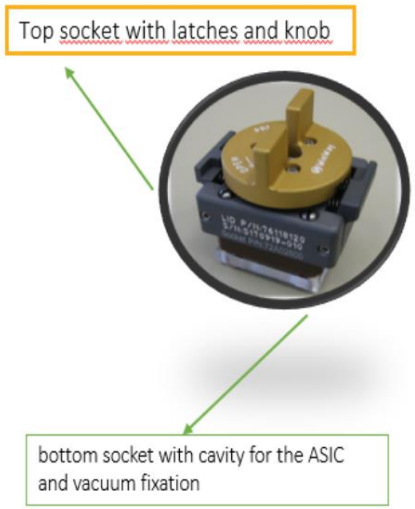
- mCBM: A CBM full system test-setup for high-rate nucleus-nucleus collisions at GSI/FAIR
- mSTS: demonstrator of STS intergration and operation aspects
- Two mechanical half-units for the first of total two mSTS tracking stations
- It will allow to test the detector and electronics components developed for the CBM experiment
- Module installation has finished
- First run was on December 2018, upcoming run in 2019

Test System@GSI









Hardware:

- Pogo pin station designed at GSI with close collaboration from Cracow team.
- The pogo- socket has 53 pogo needles, each one has a diameter of ~100 µm.

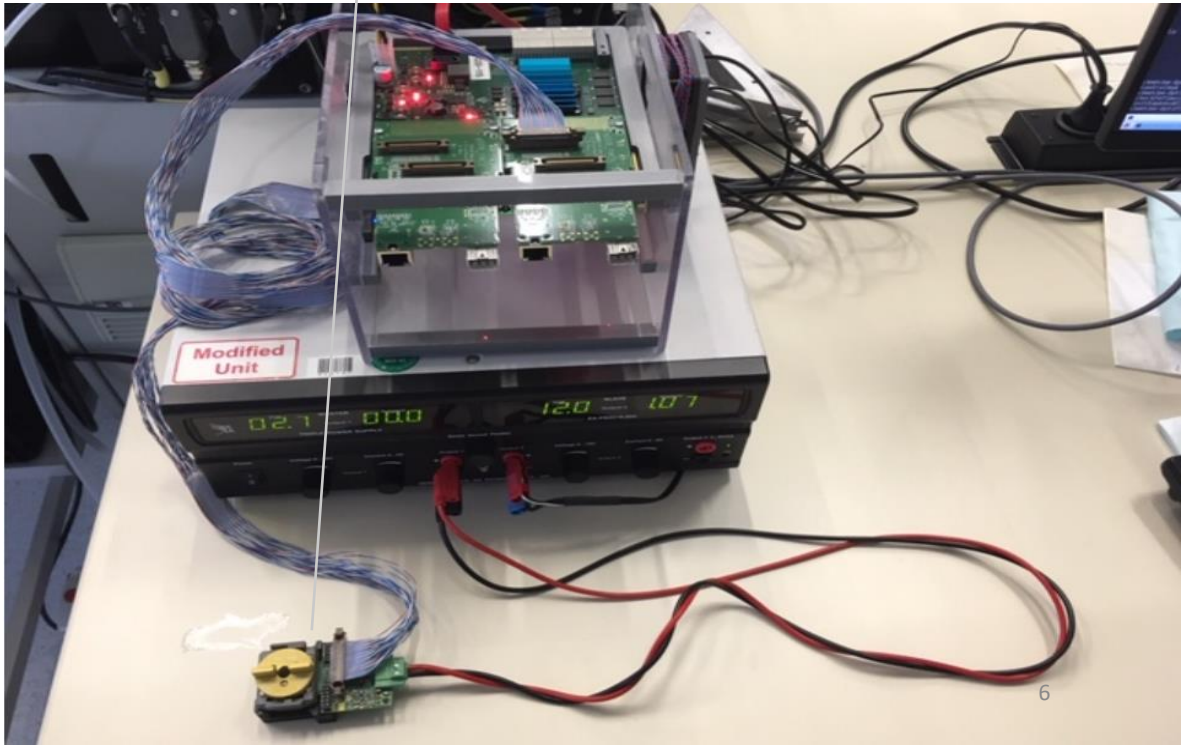
- Pogo station
- AFCK board with STS-XYTER tester firmware.
- gDPB_FMC interface card.

software basen on python

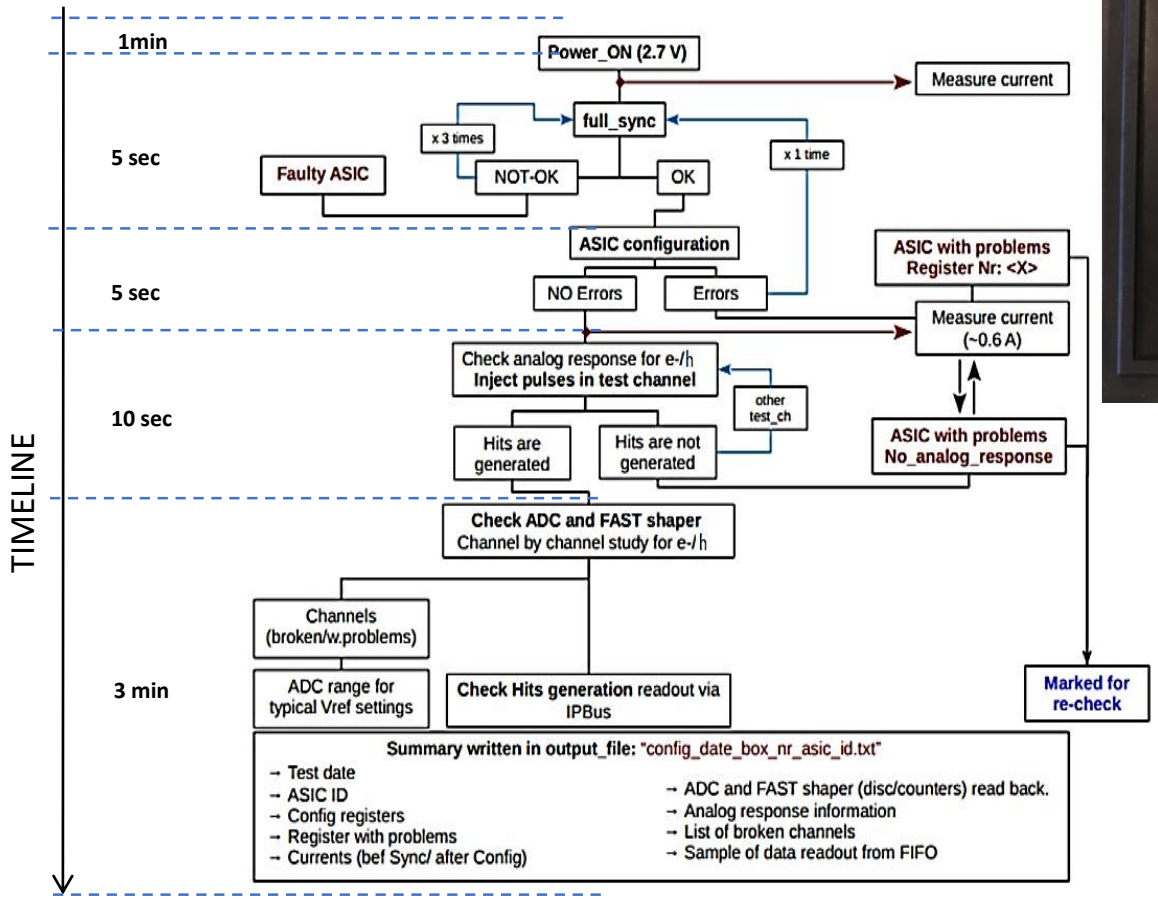
Which values are tested?

Current values, reference voltages values, analog responses, the dynamic range for the electrons and holes before calibration

@GSI Clean Room



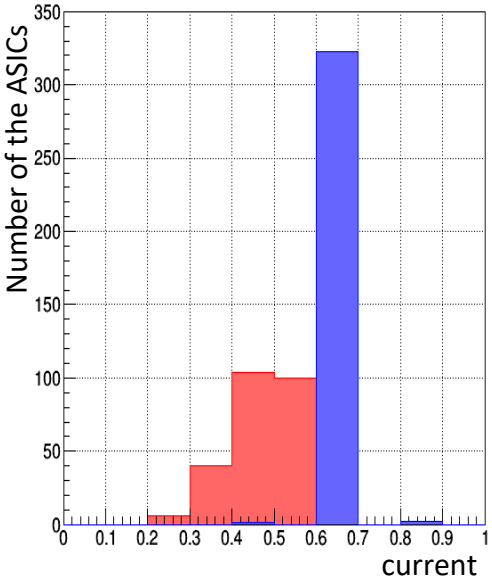
Basic protocol for ASIC testing

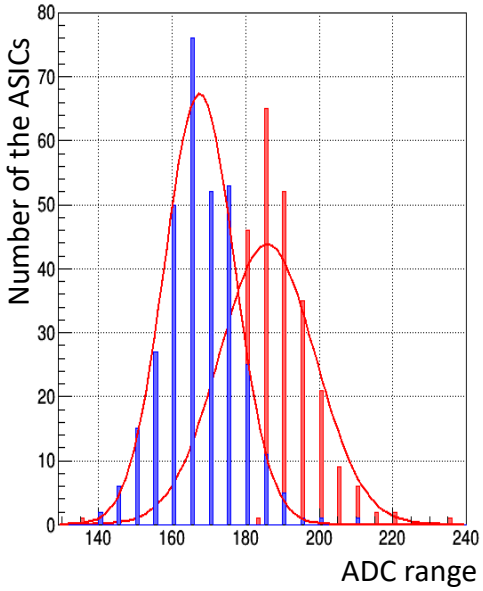


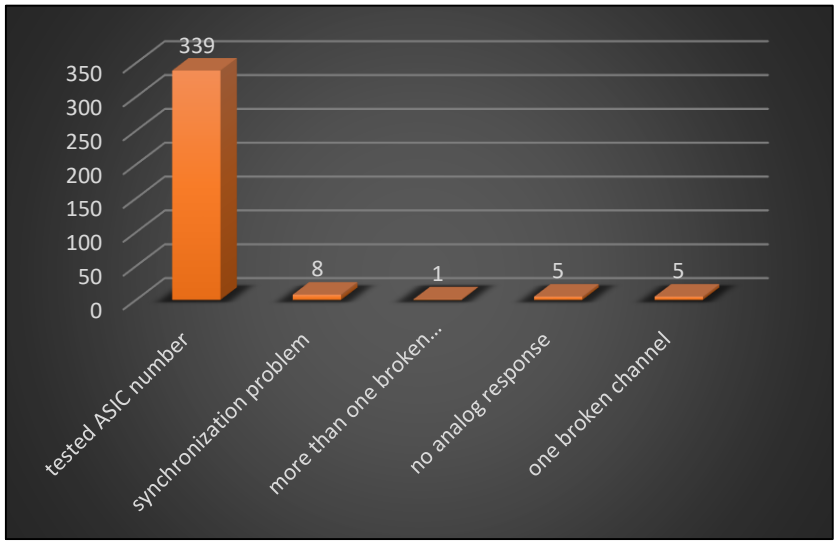
Box with ASICs

-In the version 2.1, possible to fuse a uniq ID in the chip at the pogo-pin test level
-this information can be requisted later on as a way to track the full test of the chip from basic tests until the final system

ASIC acceptance results







Before synchronization

After Configuration

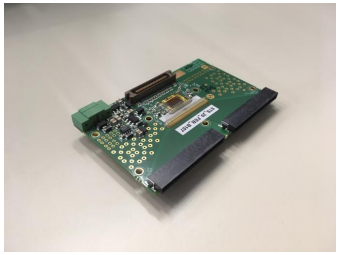
Hole

electron

Total Amount of tested ASICs: 339
Problematic ASIC number: 20
yield is 94 %

	Electrons	Holes
ADC Range (Register Value Units)	185	167
ADC Range (mV)	92.5	83.5
Amplifier Gain (ADC units/mV)	0.33	0.37

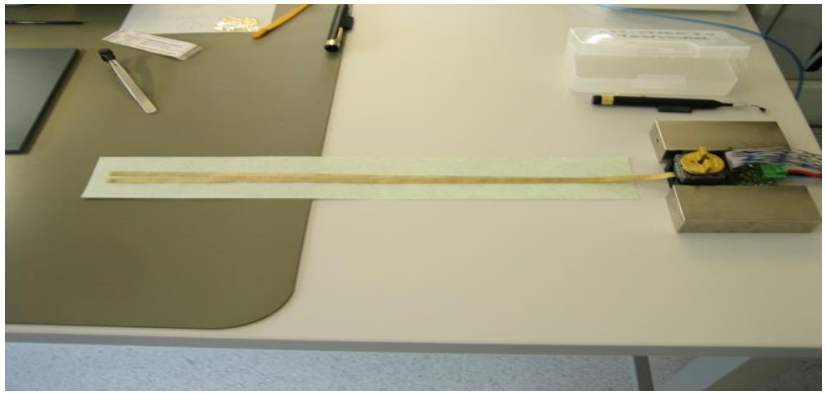
FEBB Tests



Total Number of Tested FEBs	146
Number of FEB with problematic performance	8
- Very high current	2
- No analog response	1
- No fast discriminator response	1
- One or more individual broken channel	4

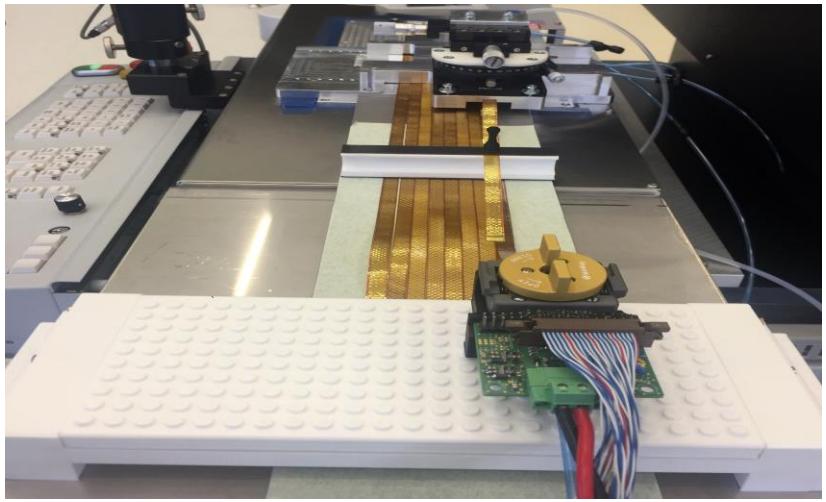
Functional tests during assembly

TEST 2: ASIC+Microcable



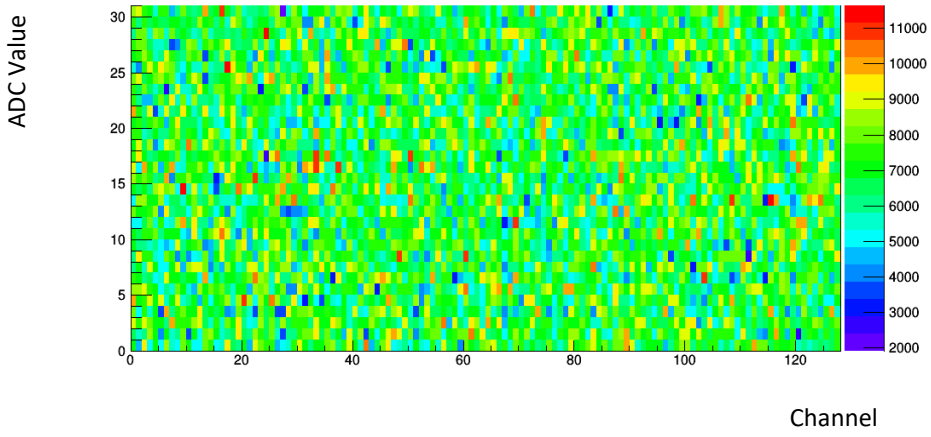
- The goal is to check electrical connectivity between microcable and ASIC (tab-bonding quality)
- Measure the noise level and see the connection of channels
- Possible to re-bond the microcable again on ASIC side

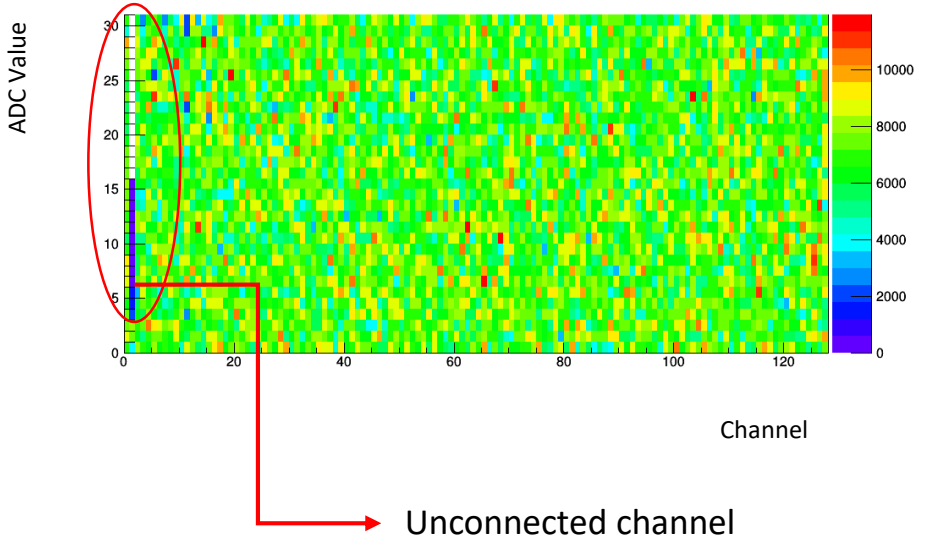
TEST 3: ASIC+Microcable+Sensor

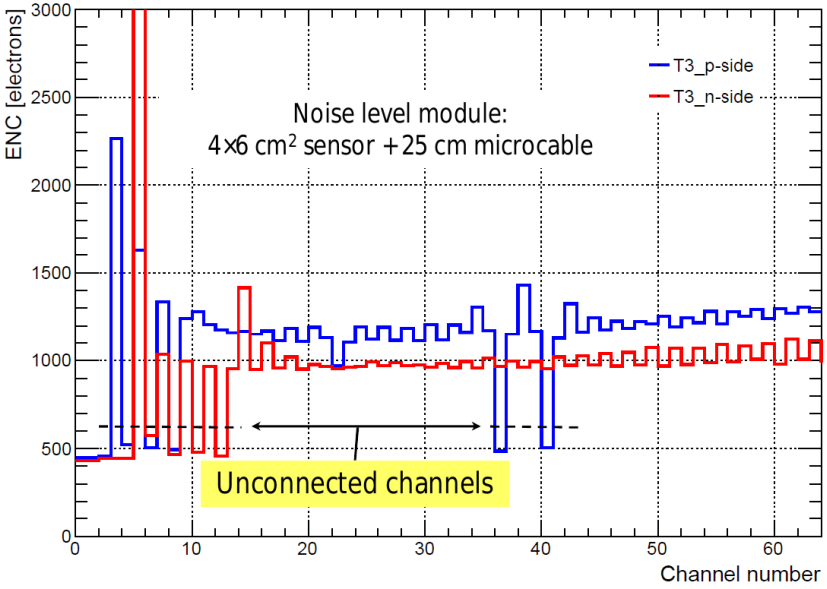


- The goal is to check electrical connectivity between microcable, Sensor and ASIC (tab-bonding quality)
- Measure the noise level and see the connection of channels
- Possible to re-bond the microcable again on the sensor side

Channel hit maps reveal unconnected channels



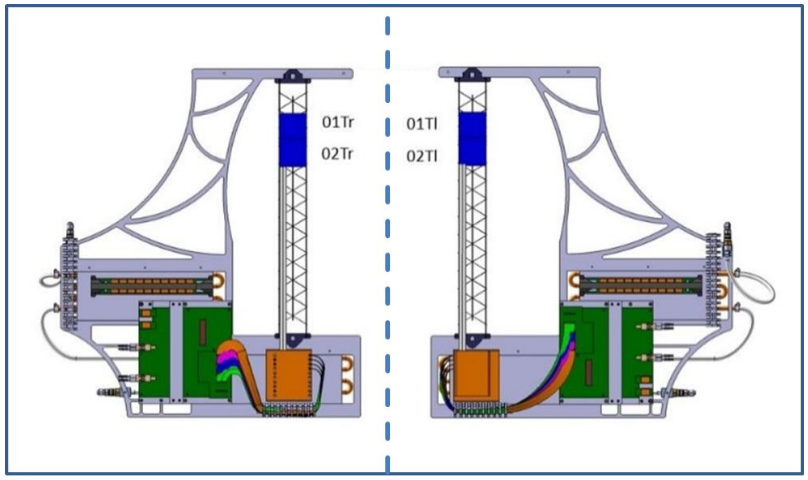




Electrical connectivity tests

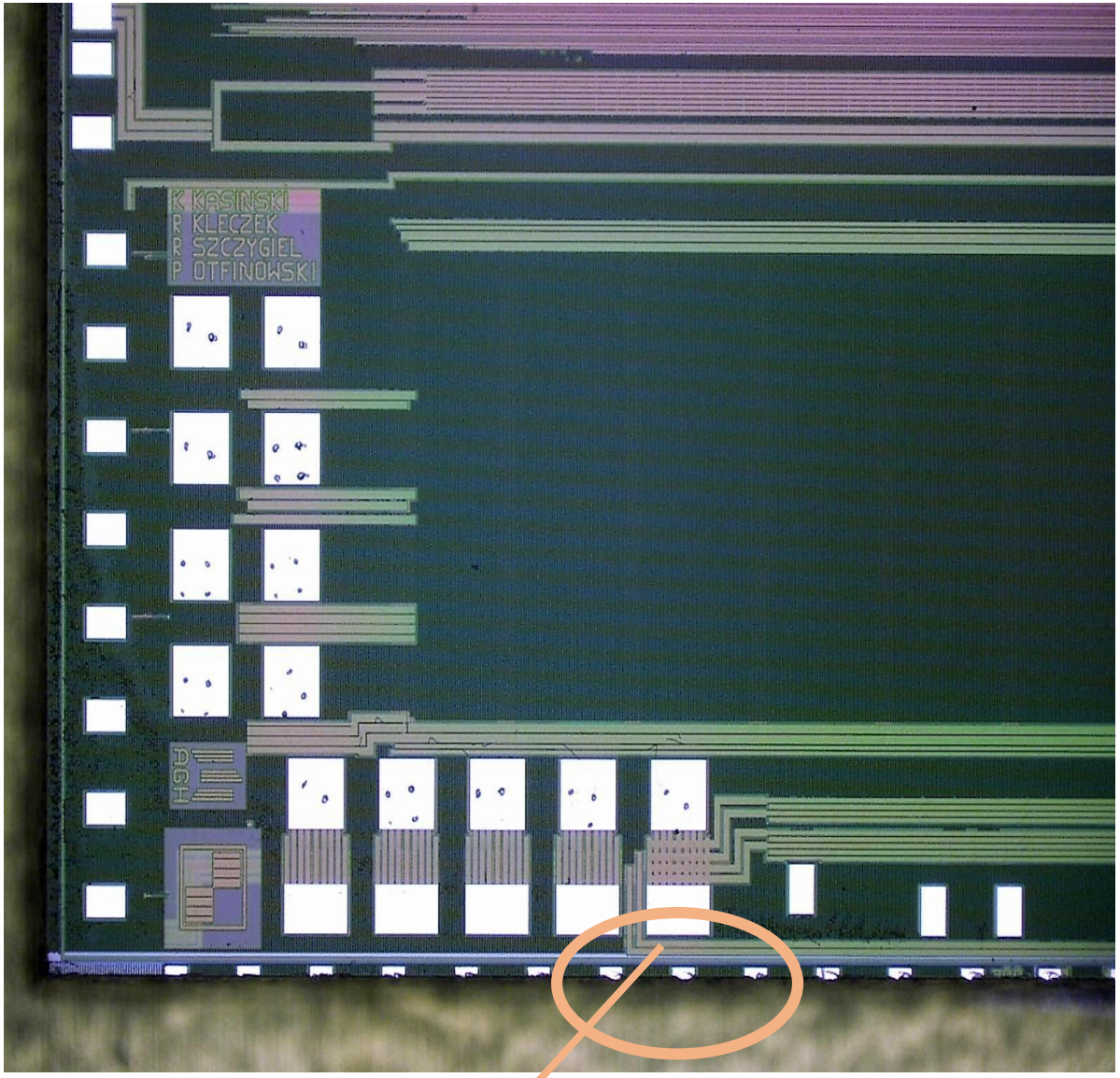
i. Histograms in root
ii. Read noise hit distribution

mCBM Module Assembly Status



ASSEMBLY STAGE	Number of tested Asics	SETUP REQUIREMENT	TEST PURPOSE	TIME/per ASIC	Number of Bad ASICs	Unconnected Channels
ASIC test	98	Pogo pin station	Fully calibration & test	12 min	10	
Module 01T-r	16	Pogo pin station	Check electrical connections	5 min		3
Module 01T-l	8 (p-side)	Pogo pin station	Check electrical connections	5 min		-
Module 02T-r	16 (only test with microcable)	Pogo pin station	Check electrical connections	5 min		2
Module 02T-l	16	Pogo pin station	Check electrical connections	5 min		-

STS-XYTER2.0—critical design detail



Critical lines for wire bonding

- ASICs showed different behaviours during the module test after assembly
- forthcoming module productions will be done with one ASIC test stage only.

Many thanks to my colleagues…

THANK YOU!