High-speed digitizing in MicroTCA with the DFMC-DS800 board

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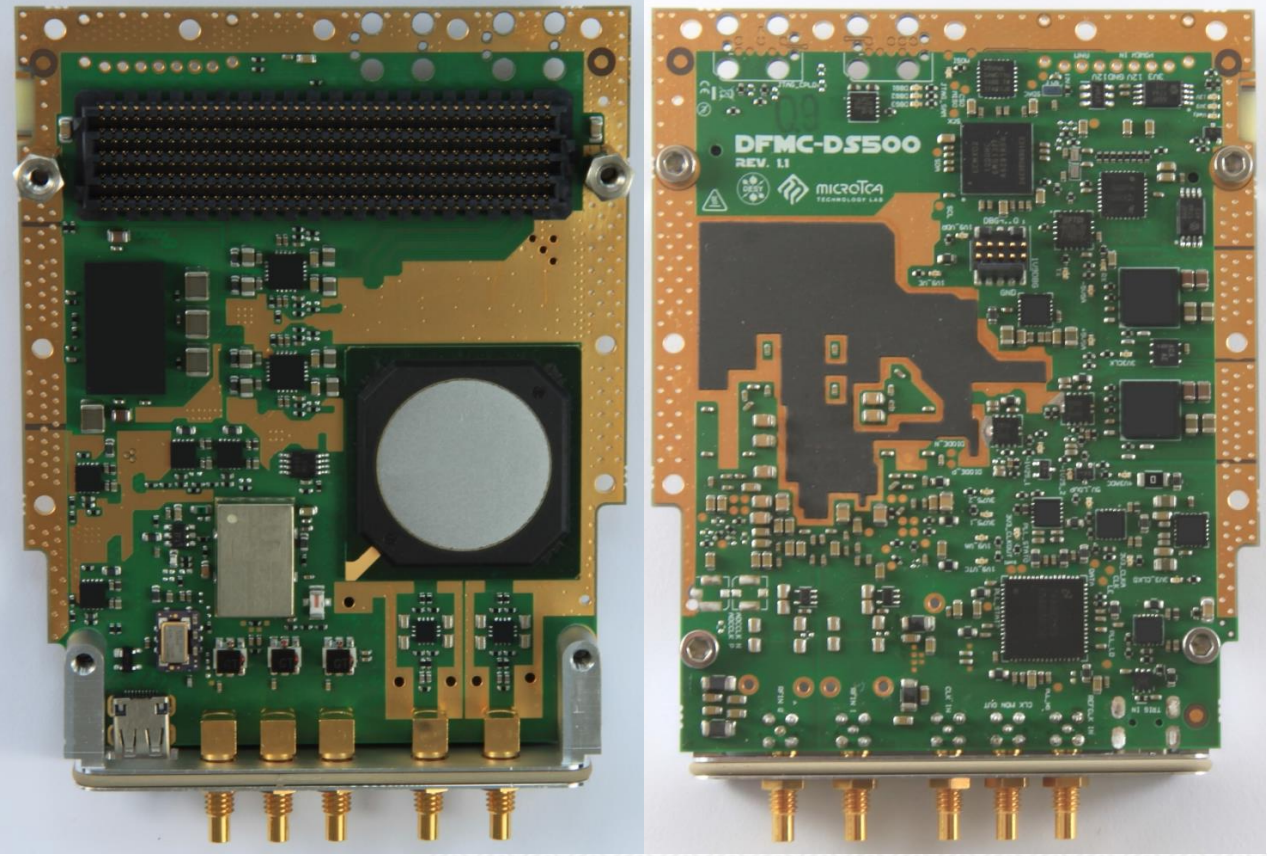
DESY.

AGENDA

1. DFMC-DS800 Digitizer Board
2. DAQ-System (Firmware / Software)
3. Applications in accelerator diagnostics
4. Demo

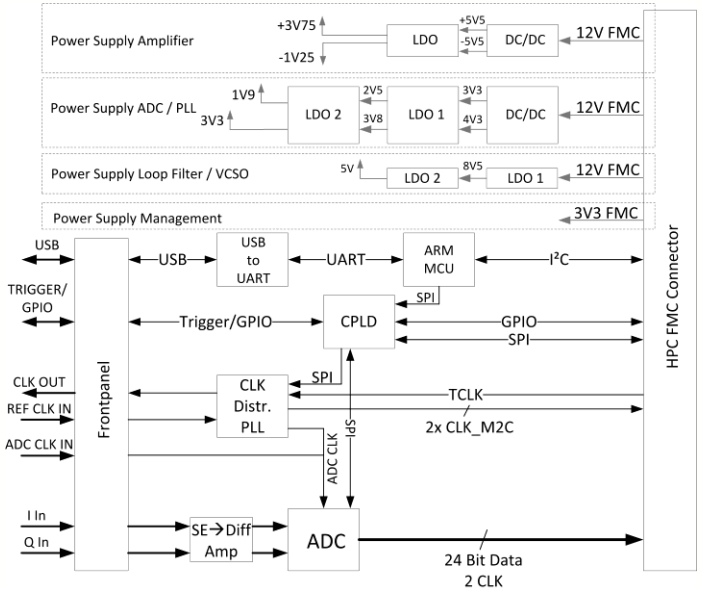
DFMC-DS800 Overview

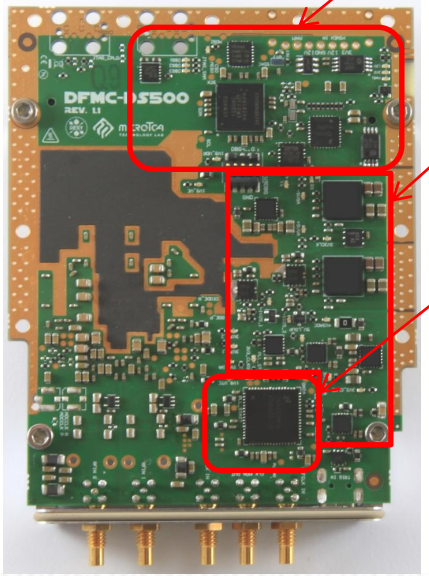


- single width FMC according to ANSI/VITA 57.1 standard
- 8.5 mm stacking height
- air cooled, shielding cage + heatsink planned
- front panel: 5 RF SSMC + 1 HDMI Type D (micro) connectors
- 12-Bit, 500/800 MSP/s Dual Ch., 1/1.6 GSP/s Single Ch.

DFMC-DS800 Overview

- ADC input bandwidth: 2.7 GHz
- fully diff. amplifier [4,5] LS bandwidth: 4.8 GHz
- no anti-aliasing filter present
- variants with up to 3.2 GSP/s





Management

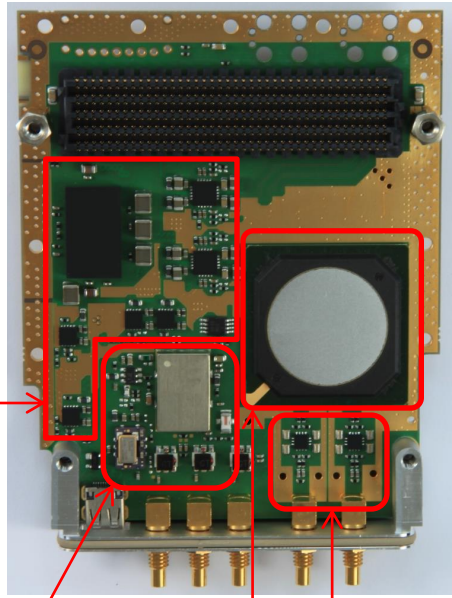
Power Supply

PLL

Oscillators/Loop Filters

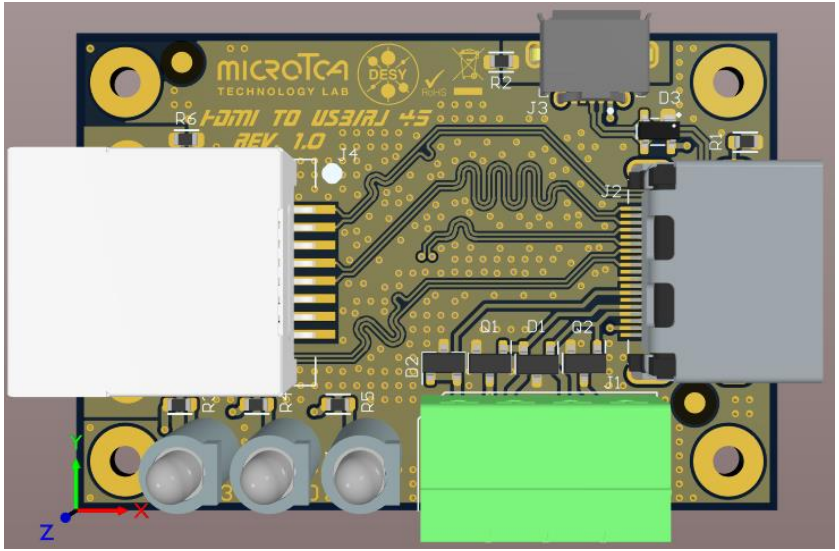
ADC

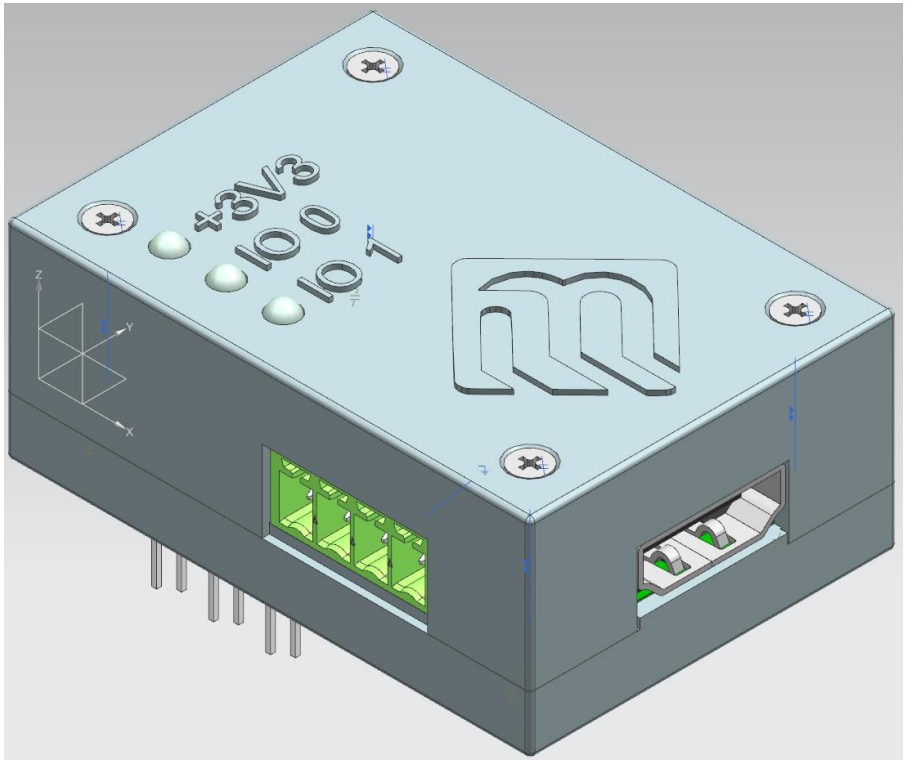
SE → DIFF Amplifiers



Break-Out board

- 4 LVDS (differential) pairs → can act as input or output (trigger/control signals, 100 MHz)
- 2 single-ended bits input / ouput
- serial interface (debugging and testing)



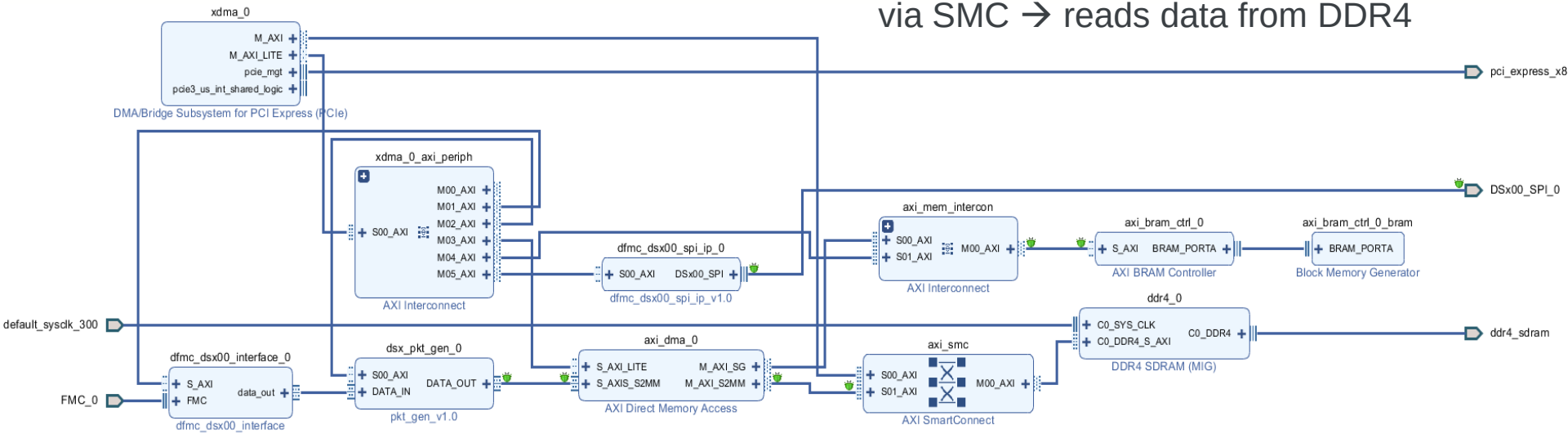


DAQ-FPGA

- DFMC-DSX00-INTERFACE connected to LVDS data lanes → delay calibration
- DSX_PKT_GEN generates AXI stream pakets readable by AXI DMA core

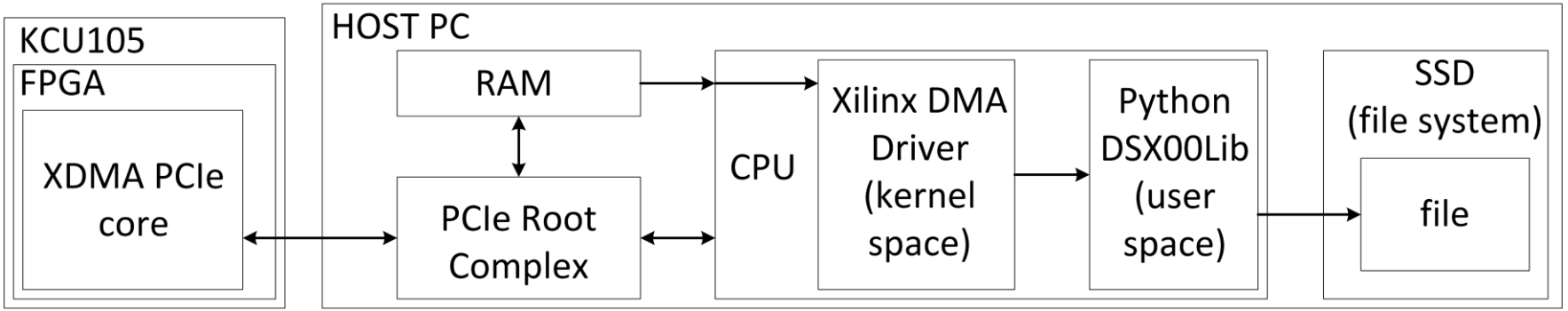
(see also THOA01, IBIC 2018, J.Marjanovic for data post-processing)

- AXI_DMA dumps data into DDR4 via AXI SmartConnect
- XDMA PCIe core controls cores via AXI Lite
- XDMA has full AXI connection to DDR4 via SMC → reads data from DDR4

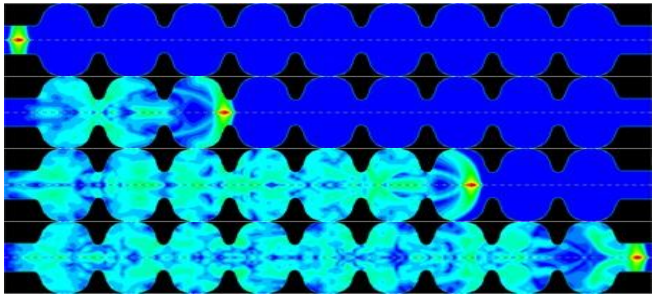


DAQ-Software

- straight forward solution for DAQ
- XDMA transfers sample data from DDR4 (KCU105) into host PC‘s RAM via PCIe root complex (DMA controller)
- Xilinx DMA driver (kernel space) provides pointer for DMA transfers into RAM
- Python library DSX00Lib can access transfered data in kernel space
- data can be dumped into file on SSD/HDD
- over 1 Mio. samples per channel can be stored on KCU105 (2GB DDR4)
- 8k samples can be stored on DAMC-FMC25 (256 MB DDR2)



Diagnostic Applications



bunch passing a cavity, H.Padamsee

Klystron melt-down after arc, TV transmitter

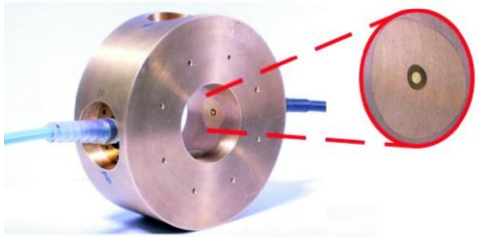
High-Order Modes

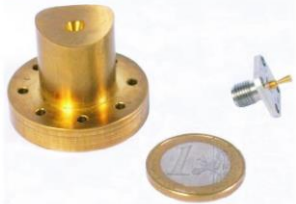
- Electron bunch excites HOM in cavity, signals from HOM couplers can provide informations about:
- beam position, beam charge, cavity alignment
  - „Electronics for High-Order Modes Detection“, Uros Mavric et al.

Klystron Lifetime Management

- Detection of dangerous Klystron states:
- gun arcs, loss of beam, loss of HF signal
  - Model Based Fast Protection System For High Power RF Tube Amplifiers Used At European XFEL Accelerator, Lukasz Butkowski

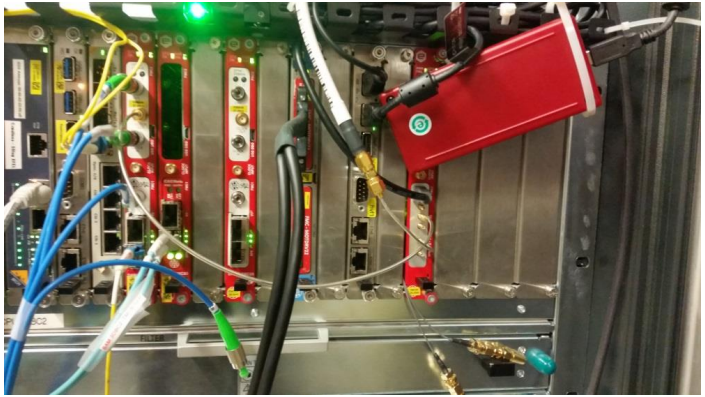
Diagnostic Applications

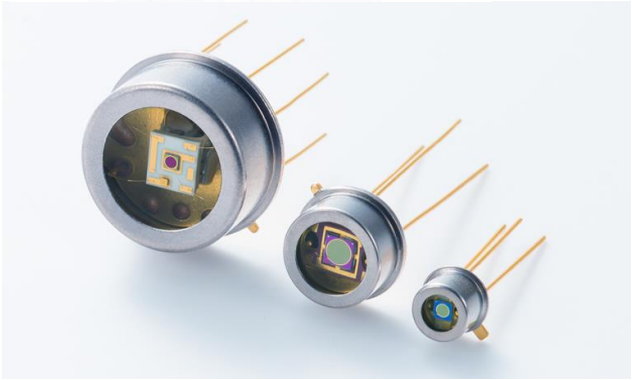




Bunch Arrival Time Monitor

- direct sampling of pick-up [6] signals
- reduction of bandwidth from 40 GHz to 2.4 GHz
- roughly estimate bunch arrival time
- adjust electro-optical BAM



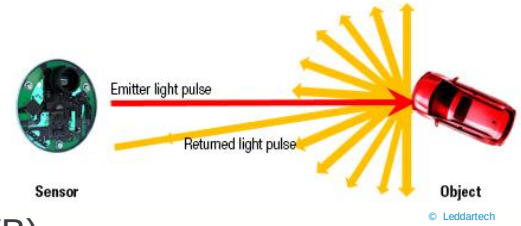


Photodiode / PSD

- fast photo diode and PSD readout (front end needed)
- beam position measurments
- light intensity measurements

Summary and Outlook

- RADAR / LiDAR
- Signal Intelligence
- RF sampling SDR
- Consumer RF (DAB, DVB)
- 3G/4G Basestations



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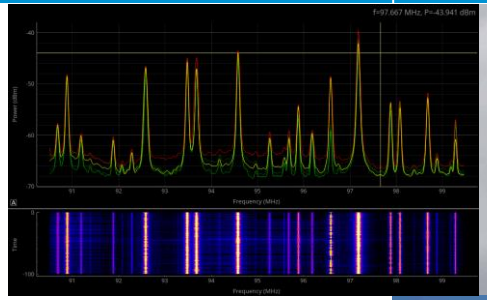

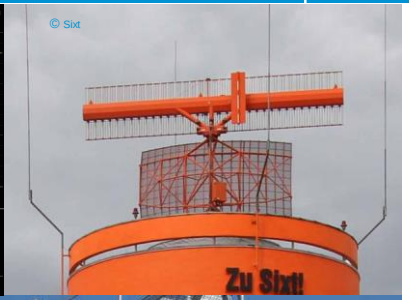

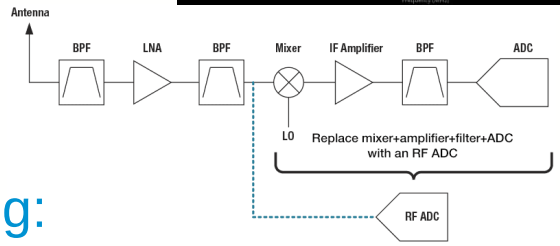

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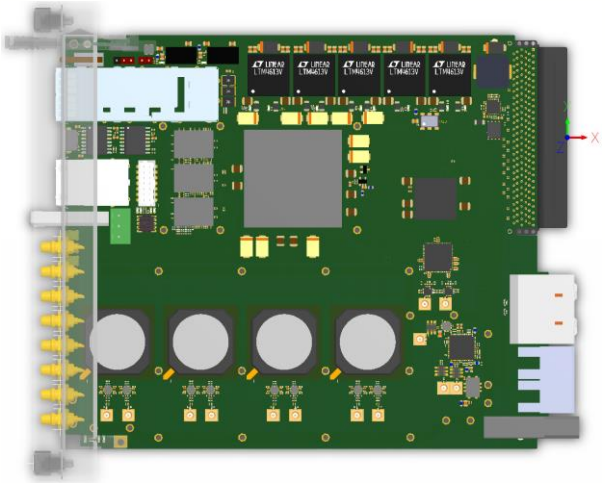


Upcoming:

- DFMC-DS800 final revision available end of 1st quarter 2019
- DAMC-DS800 → 8 channel digitizer AMC, same ADCs as DFMC-DS800
- 10/12-Bit variants with up to 3.2 GSP/s available

ACKNOWLEDGEMENTS

M. K. Czwalinna, M. Fenner, S. Jablonski, J. Marjanovic, H. Schlarb

Thank you for your attention.

DEMO

References

[1] Prototype of the Improved Electro-Optical Unit for the Bunch Arrival Time Monitors at FLASH and European XFEL, H. Dinter et al., Proceedings of FEL, 2015

[2] The Bunch Arrival Time Monitor at FLASH and European XFEL, M. Viti et al., Proceedings of ICALEPCS, 2017

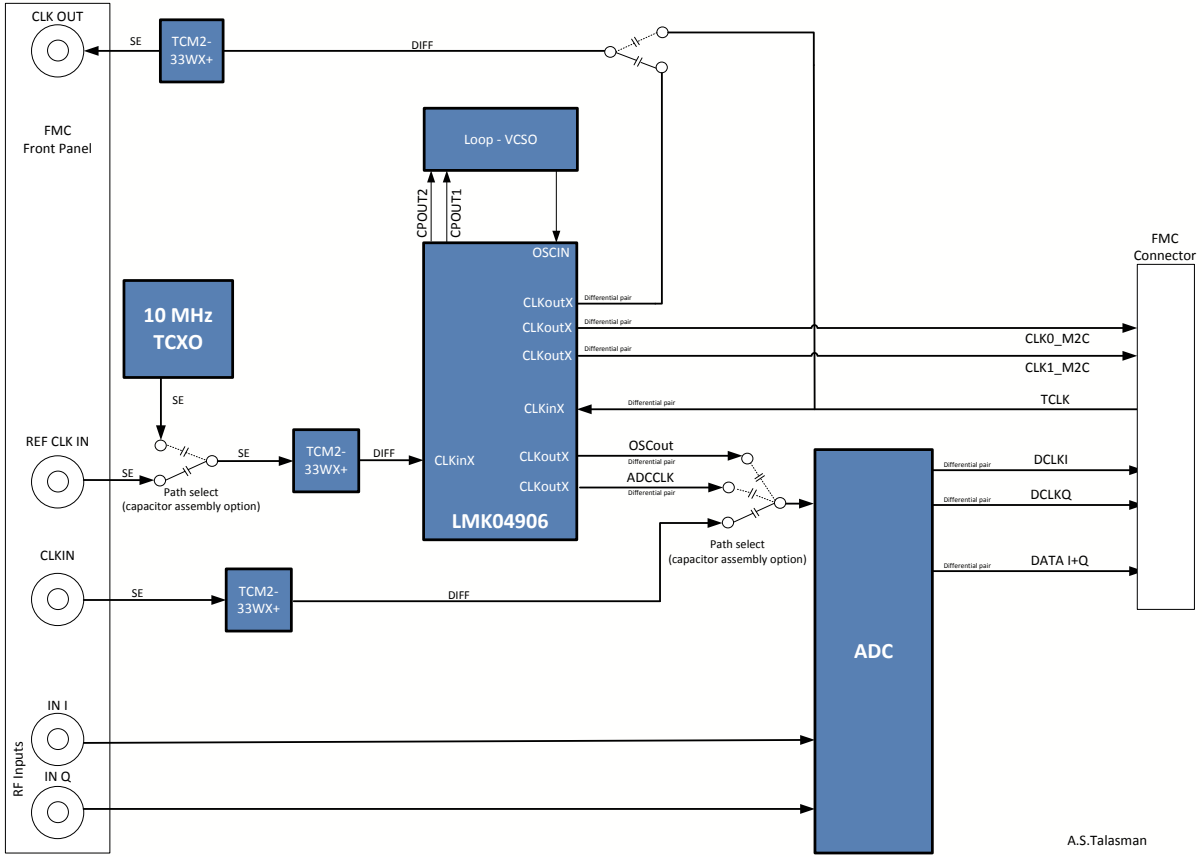
[3] High bandwidth pickup design for bunch arrival-time monitors for free-electron laser, A. Angelovski et al., PHYSICAL REVIEW SPECIAL TOPICS - ACCELERATORS AND BEAMS, 2012

[4] Driving the GSPS ADCs in Single-Channel or Dual-Channel Mode for High Bandwidth Applications, M. Plisch, J. Brinkhurst, TIDU175 Texas Instruments Incorporated, July 2012

[5] Stabilizing Differential Amplifiers as Attenuators, L. Siebert, TIDA00522 Reference Guide, Texas Instruments Incorporated, August 2016

[6] High Bandwidth Pickup Design for Bunch Arrival-Time Monitors for Free-Electron Laser, A.Angelovski et al.,Physical Review Special Topics – Accelerator and Beams, 2012

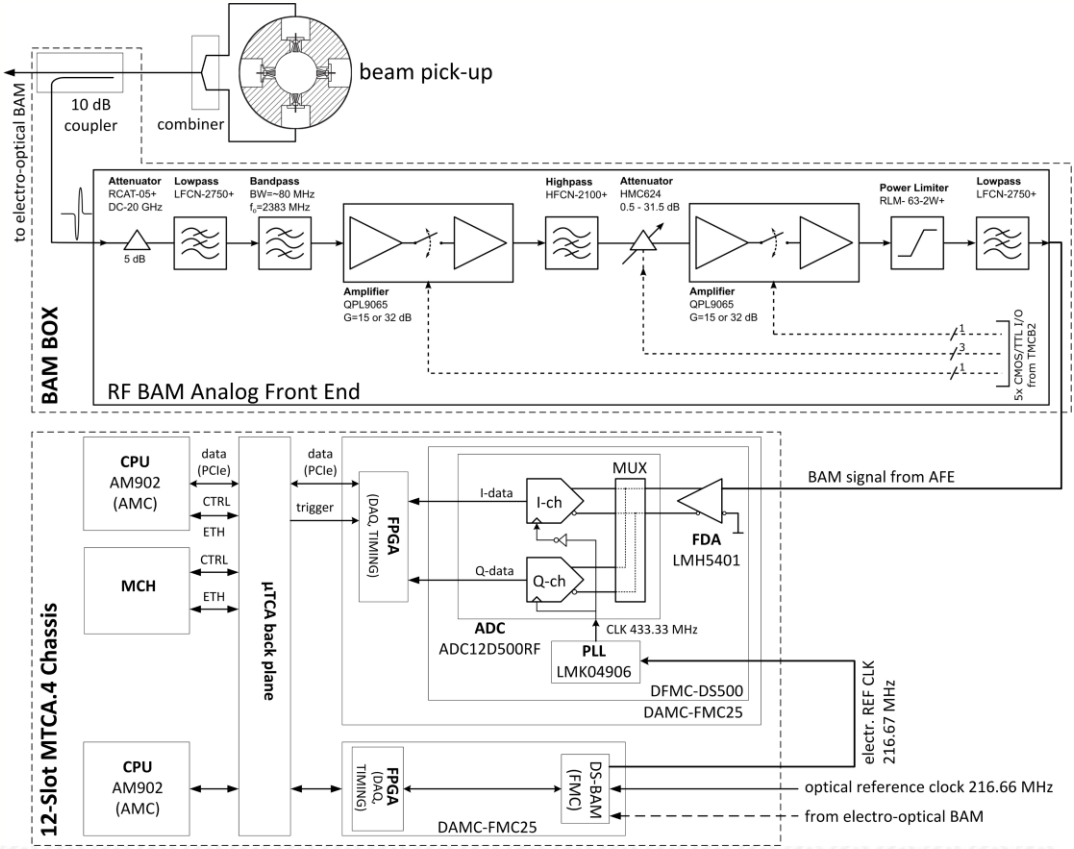
Clock Tree



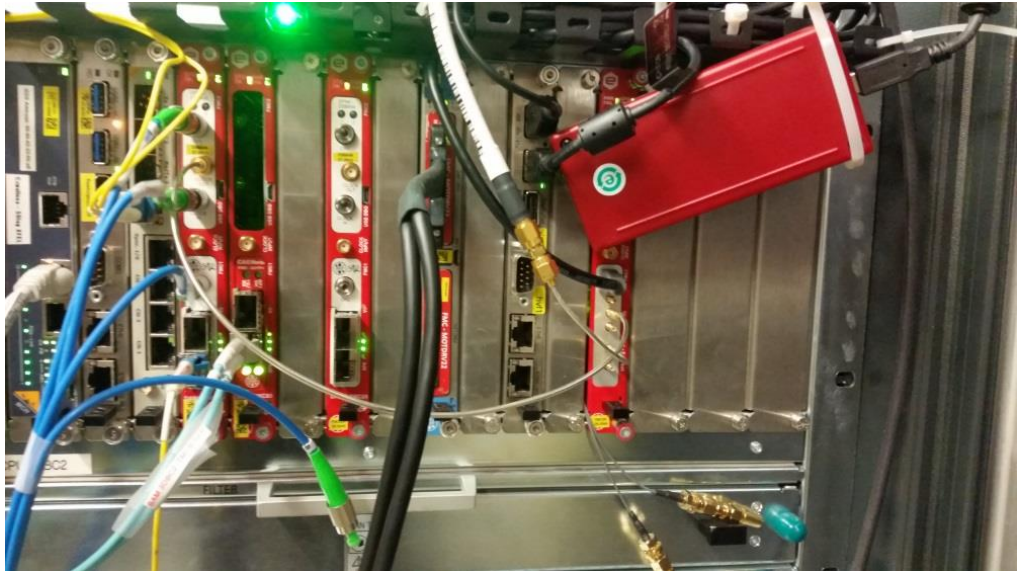
- direct clock feed to ADC
- local 10 MHz oscillator
- PLL which can lock:
  - 10 MHz clock
  - front panel clock
  - TCLK (MTCA BP)
- local VCSO 800 MHz
- external loop filter
- clock output (debug)
- two clock paths to carrier

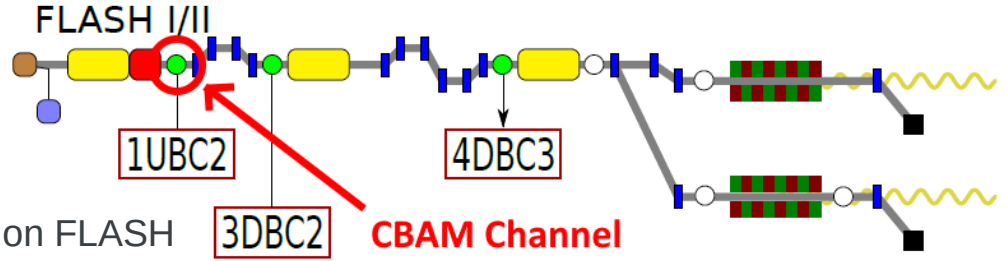
Coarse BAM Channel

- coarse BAM Channel planned in FLASH
- coarse BAM channel in addition to electro-optical BAM [1,2] → automatically adjust optical delay lines
- uses same combined high-bandwidth pick up [3] signals (40 GHz)
- analog front end bandpass filters the pick up signal
- bunch charges can vary from 20 pC up to 1 nC, which requires a dynamic range of about 34 dB
- sampling (DFMC-DS500/DAMC-FMC25) and processing in MTCA.4 crate



CBAM Channel in FLASH



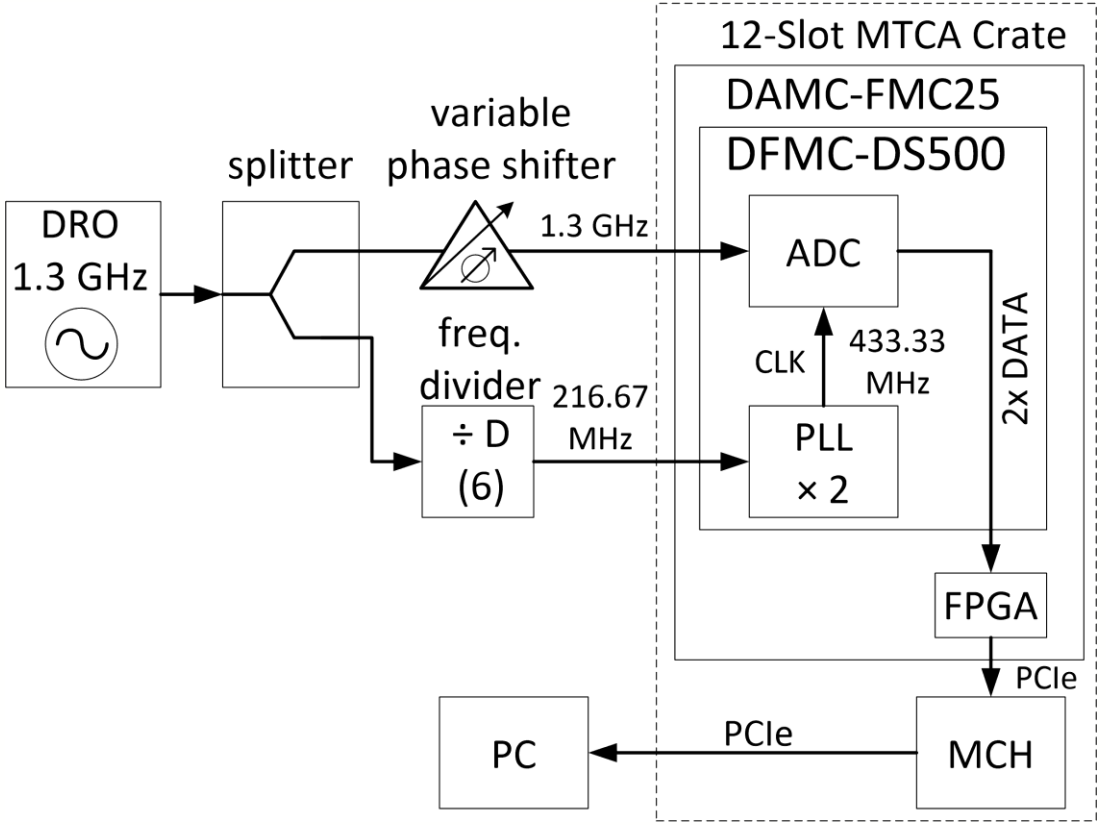


MOOB03, IBIC 2018, N. Baboi et al. for more details on FLASH

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

CBAM DS500 Test Setup

- complex high-bandwidth pick up signal
- testing ADC performance under ideal conditions with reduced signal bandwidth
- undersampling 1.3 GHz carrier with phase synchronous ADC clock → produces DC signal
- timing error converts into amplitude error
- roughly estimate the timing accuracy



Results

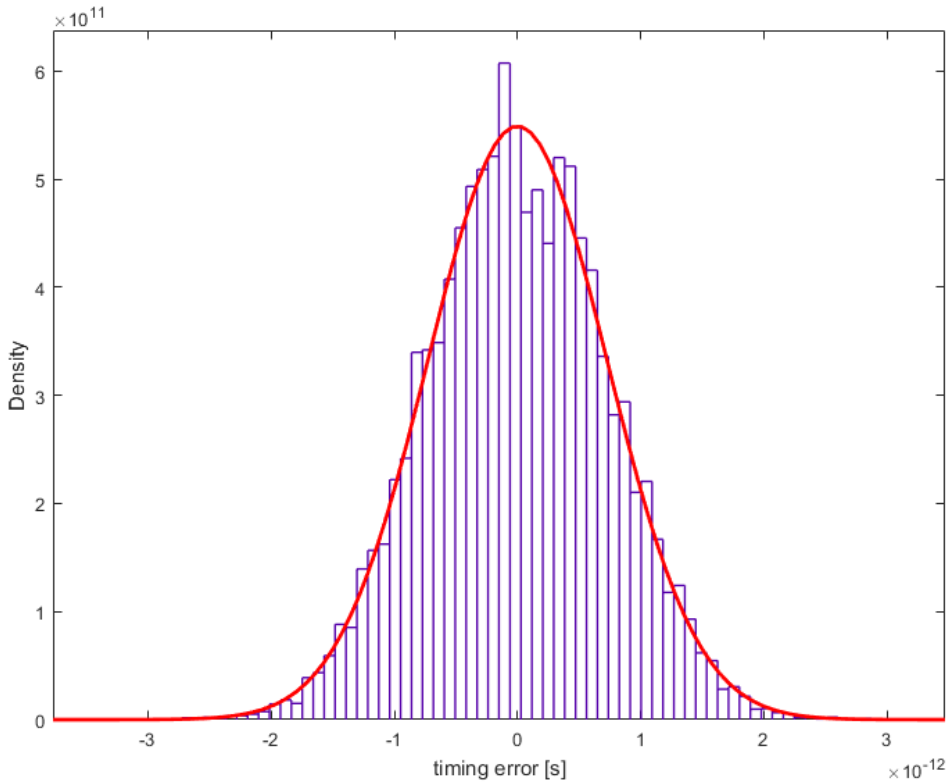
- recorded 1.6M samples
- fitting normal distribution with:

  μ = -2.93117e-21s

  σ = 726.36 fs

- timing error (p2p): 7 ps
- timing error (rms): 726 fs

- results are not outstanding but also not bad
- meet the requirements of ~1 ps



Summary & Outlook

- results of test measurements look promising
- meet the requirements of ~ 1 ps timing error
- operation in FLASH will show wether the accuracy will actually be achieved

- further improvements of the DFMC-DS500 have to be done → second revision
- PLL is not running with full performance (reduction of phase noise and jitter)

EOBAM System

BAM System's Units & Periphery