# Camera Read-Out with MicroTCA

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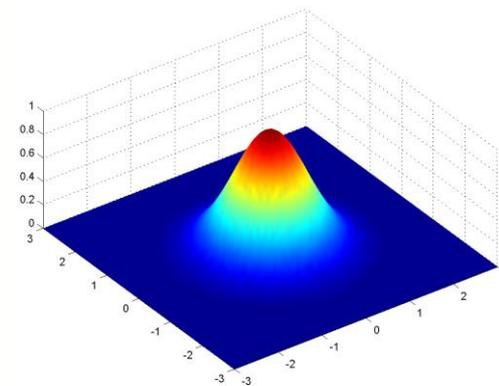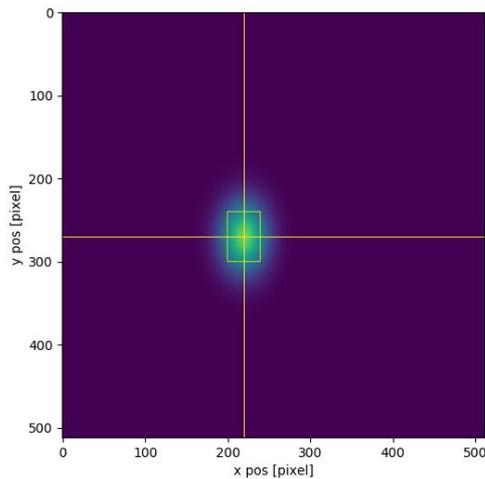
# AGENDA

1. Motivation - GigE Vision for Beamline Scientists

2. Overview about the standard

3. GigE Vision IP Core

4. Usage with MicroTCA Hardware

5. Live Demo

- Possibility to outload image processing to FPGA

- Algorithms can run in parallel

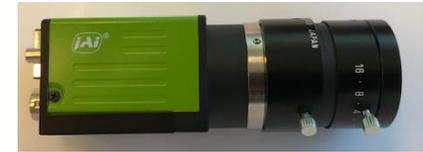- Flexibility of software, power of hardware

Beam Diagnostics

- Calculation of centroid standard deviation

- Gaussian fitting

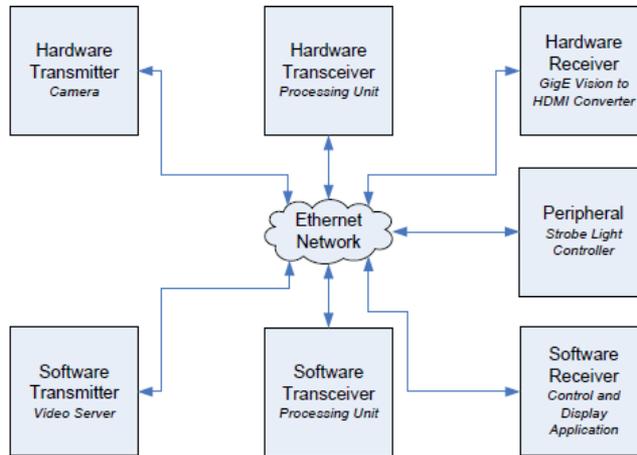- Target protecting system (shutdown if beam runs out of focus)

# GigE Vision Standard

- UDP/IP based protocol

- Gigabit – Ethernet

- Several additional features
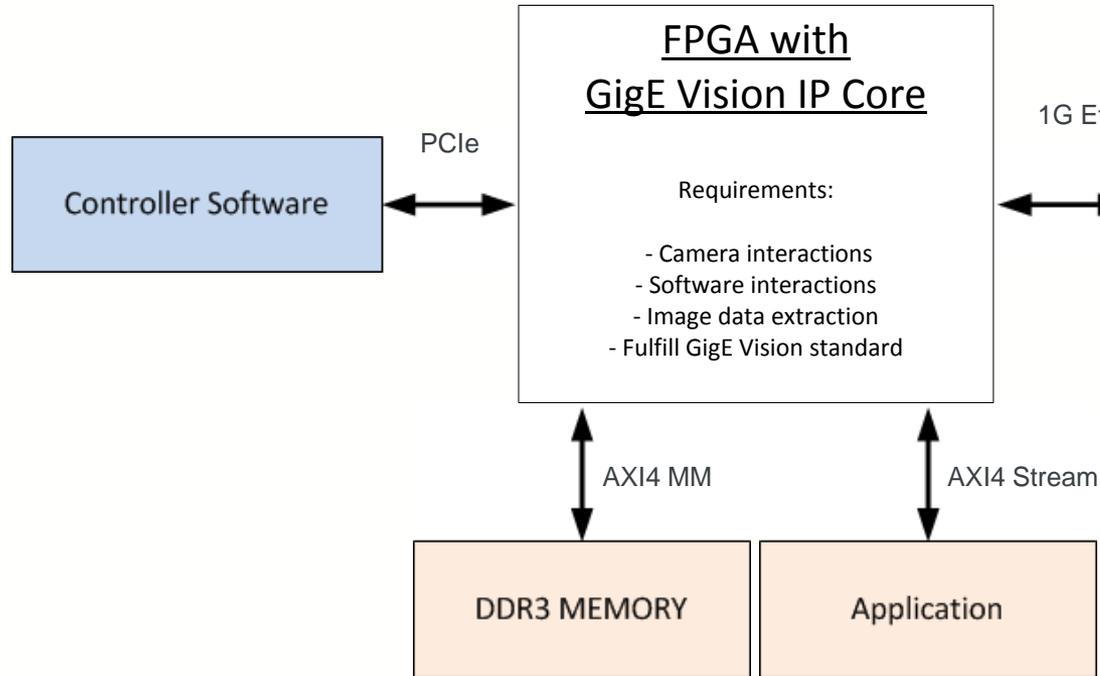


Allied Vision Mako G-030



JAI – GO 2400 PGM



*from GigE Vision Standard version 2.0*

Advantages:

- simple cabling (up to 100 m, PoE)

- faster transfer rate than IEEE 1394

- lower cost compared to parallel and Camera Link standards
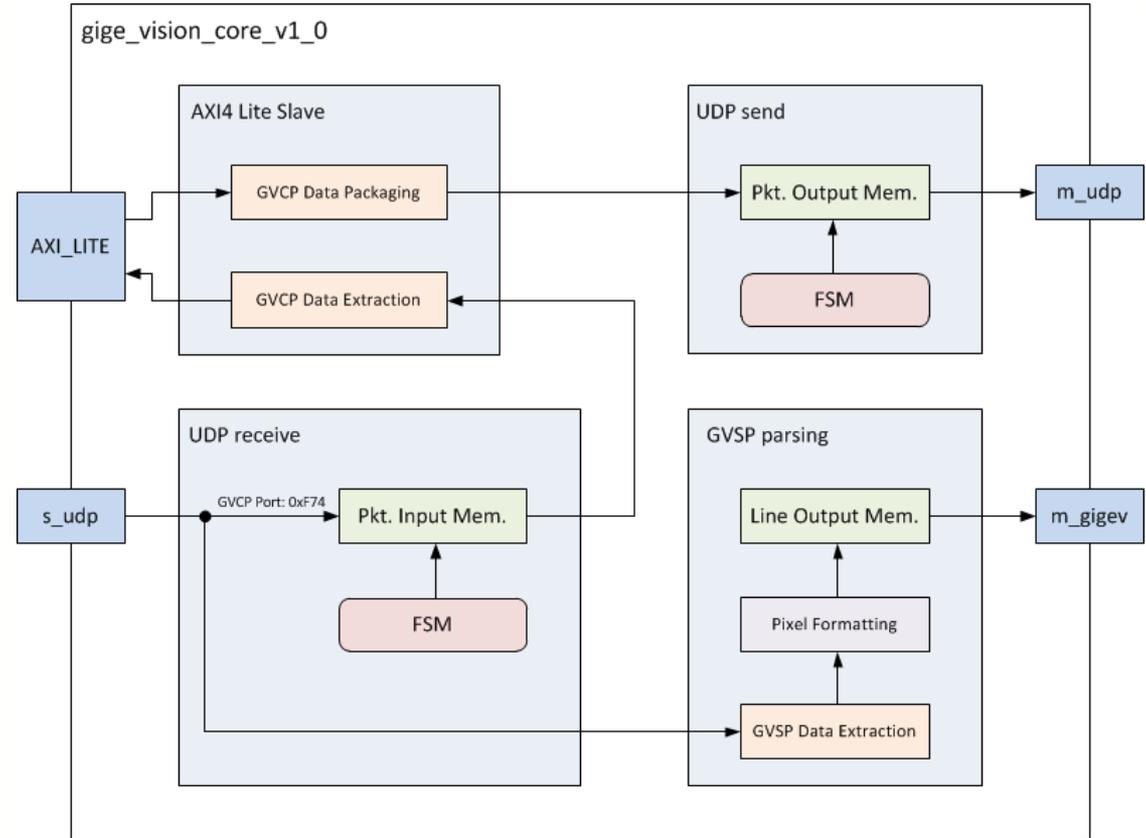
- device precision time protocol

**FPGA with GigE Vision IP Core**

Requirements:

- Camera interactions
- Software interactions
- Image data extraction
- Fulfill GigE Vision standard

Controller Software

PCIe

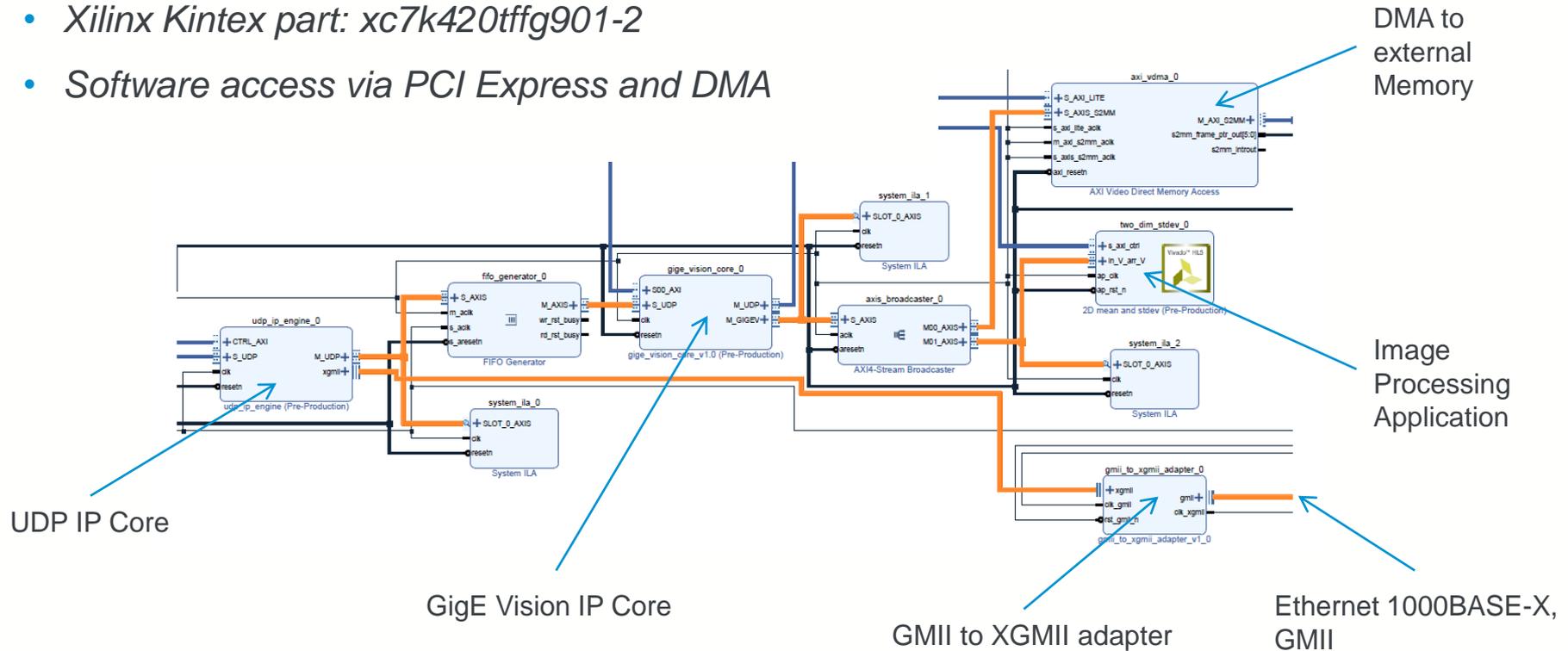1G Ethernet

CAMERA

AXI4 MM

AXI4 Stream

DDR3 MEMORY

Application

General Concepts:

- GigE Vision Control Protocol
- GigE Vision Stream Protocol
- Discovery Mechanism
- XML description file

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DESY.

# GigE Vision IP Core

General Features:

- Software interface

- Send GVCP packets

- Receive GVCP/GVSP packets

- Pixel formatting

- Send image data stream

# GigE Vision FPGA Design

- *Xilinx Kintex part: xc7k420tffg901-2*

- *Software access via PCI Express and DMA*

DMA to external Memory

Image Processing Application

UDP IP Core

GigE Vision IP Core

GMII to XGMII adapter

Ethernet 1000BASE-X, GMII

PCI Express data exchange via backplane

DAMC-TCK7

- Kintex7 FPGA with GigE Vision firmware

MTCA CPU

- GigE Vision controller software

External Monitor

- Image Output (Live, FullHD)

- Format is adjustable in software

JAI GO 2400 PGE

- 8-bit, 12-bit, 10-bit monochrome

- 48.8 fps with full resolution



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- 8 bit per pixel (Mono8)
- Python Controller Software
- Plotting with OpenCV
- Counter in FPGA
- Timer in Software
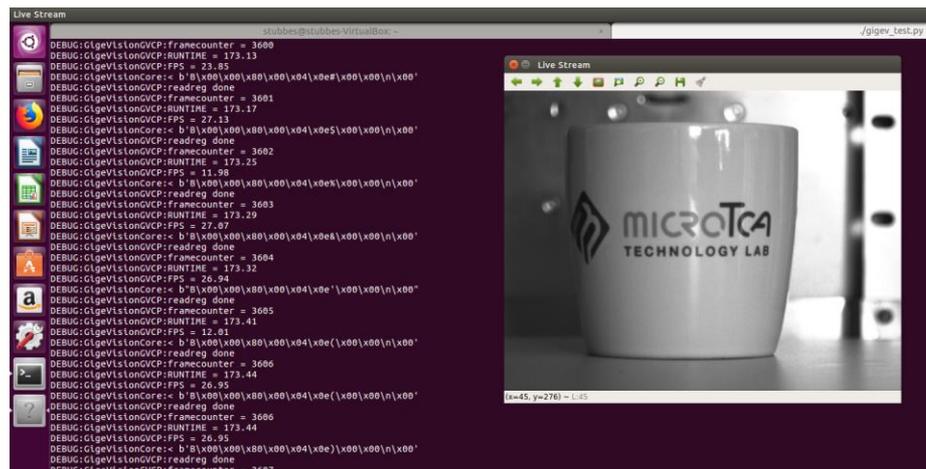


| Resolution | Frame Size | Max. Framerate 1GB Eth. | Framerate FPGA | Framerate Software |
|---|---|---|---|---|
| 640 x 480 px | 2.46 Mbit | 406 fps | 53 fps | 24 fps |
| 1920 x 1080 px | 16.59 Mbit | 60 fps | 50 fps | 20 fps |
| 1936 x 1216 px | 18.83 Mbit | 53 fps | 48 fps | 18 fps |

*Bottleneck:*

*Data Read Out from DDR3*

Live Demonstration

1. FullHD resolution live image with 20 fps in average
2. Two dimensional mean calculation with Vivado HLS IP Core