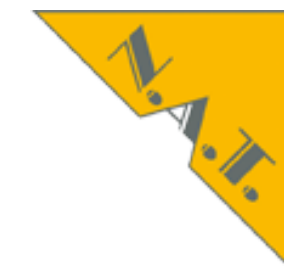
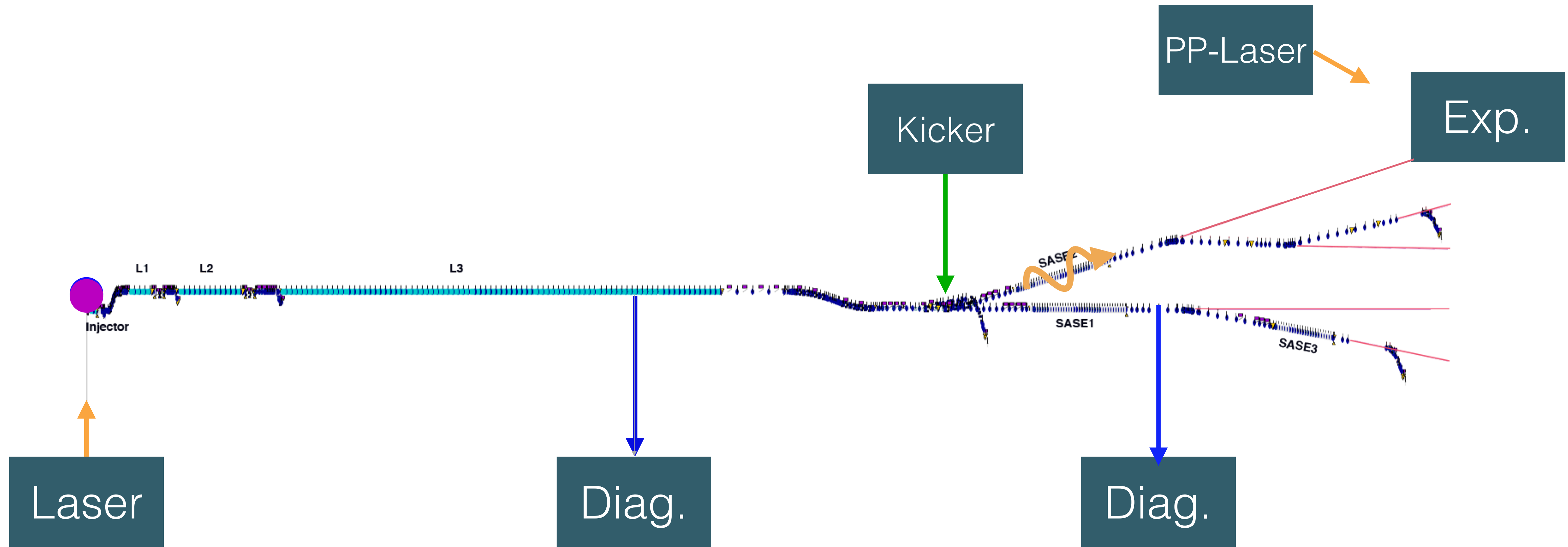


The XFEL Timing System

Kay Rehlich, DESY MCS4 & TechLab

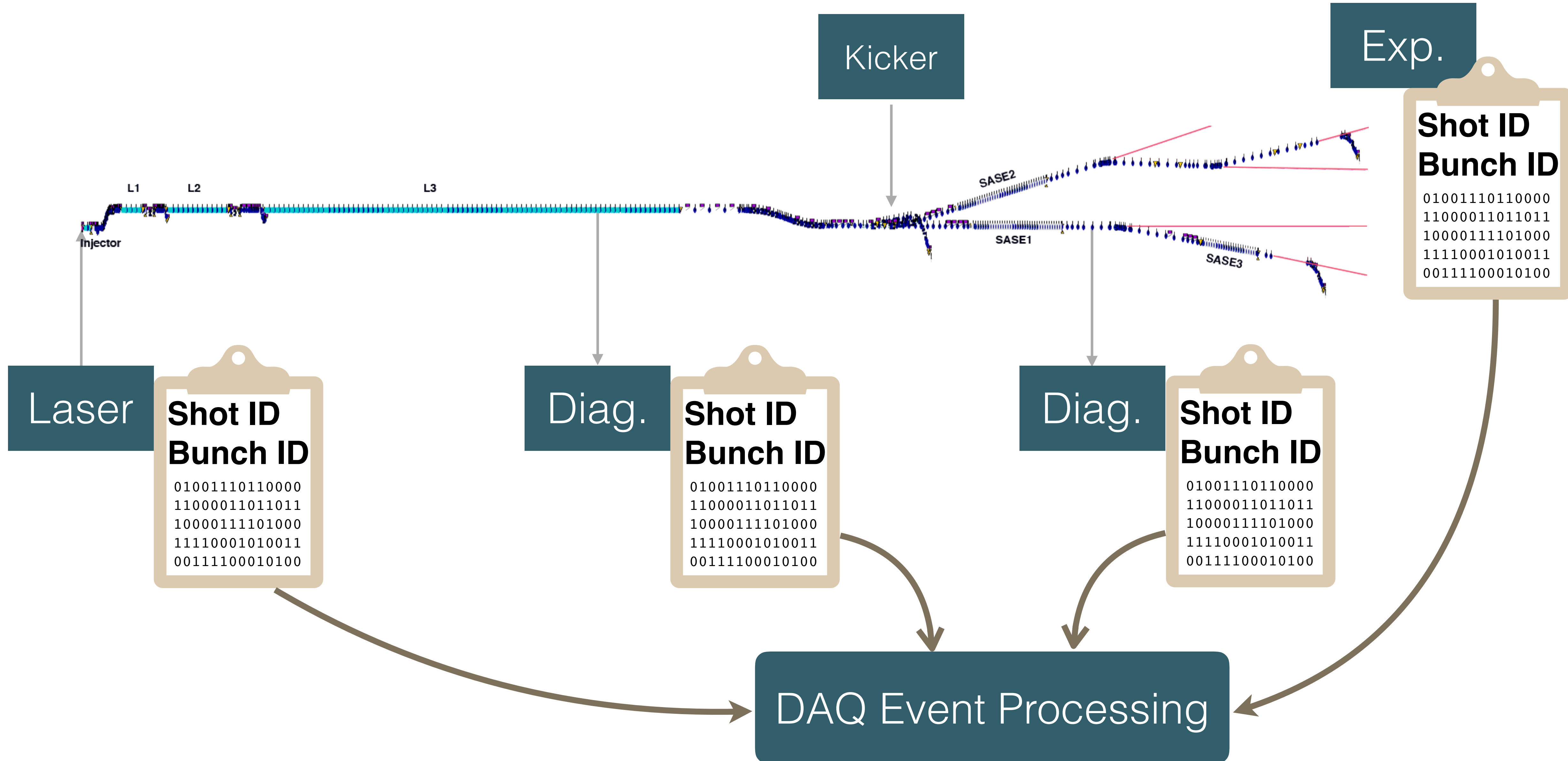


Introduction - Clocks & Triggers

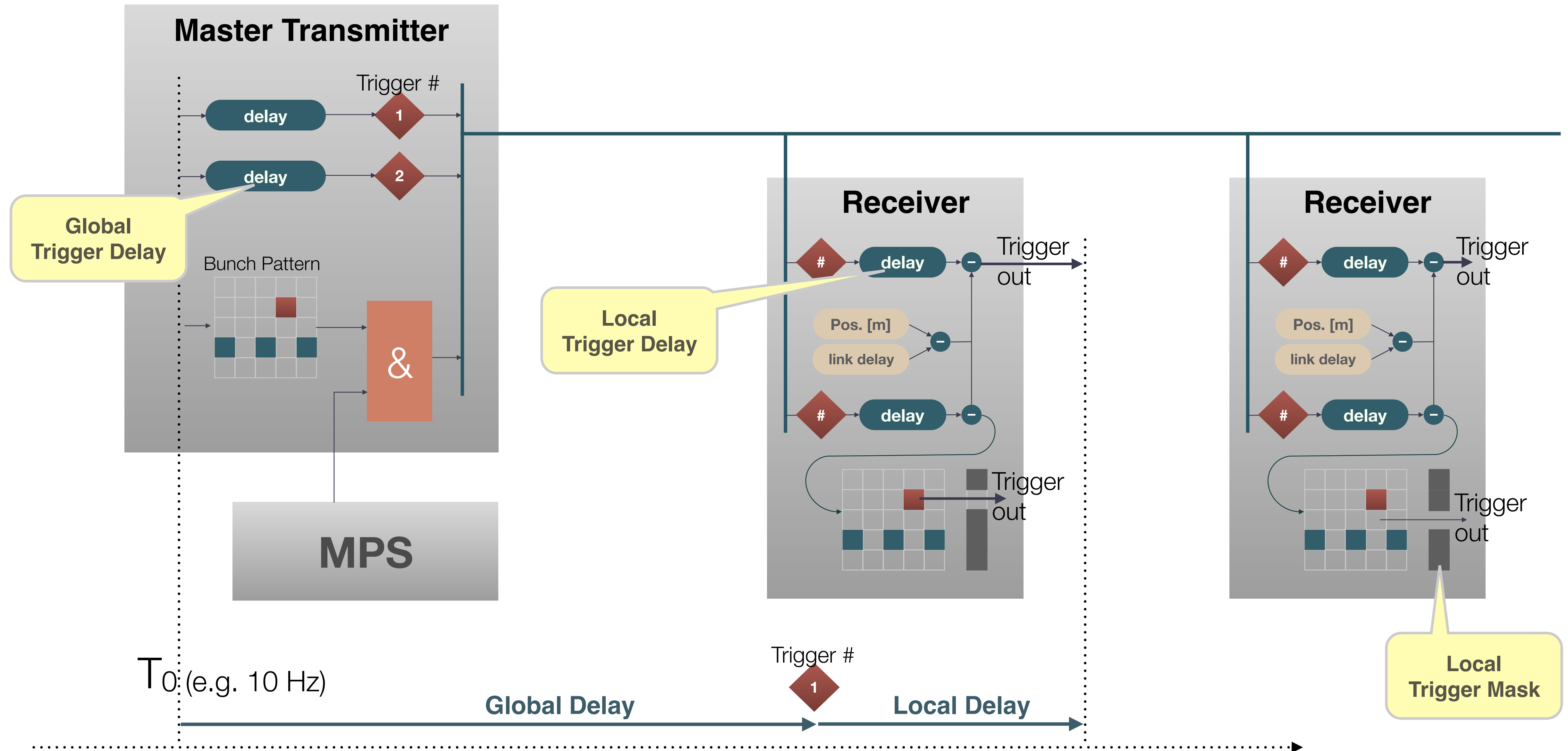


- Define the source and destination of bunches (XFEL: 27000 / sec.)
- Trigger and clocks for diagnostics and actuators depending on location

Introduction - Data Tags for Software



Trigger and Bunch Pattern Distribution





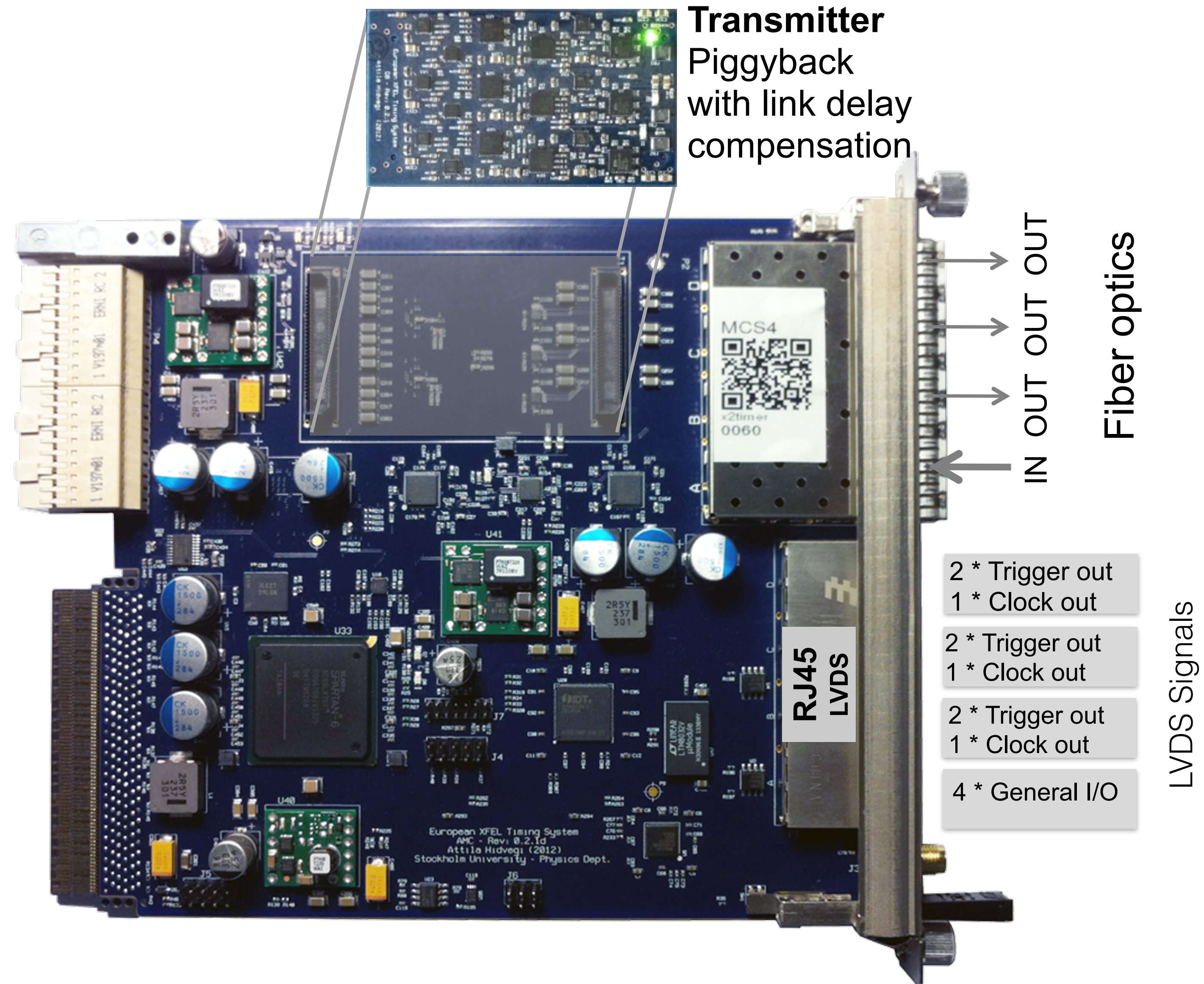
MicroTCA.4 Timing Receiver / Transmitter

Can be used as a timing **receiver** or **transmitter**

Optional **RTM**:
9 transmitters,
Further triggers or
clocks

MicroTCA Backplane:

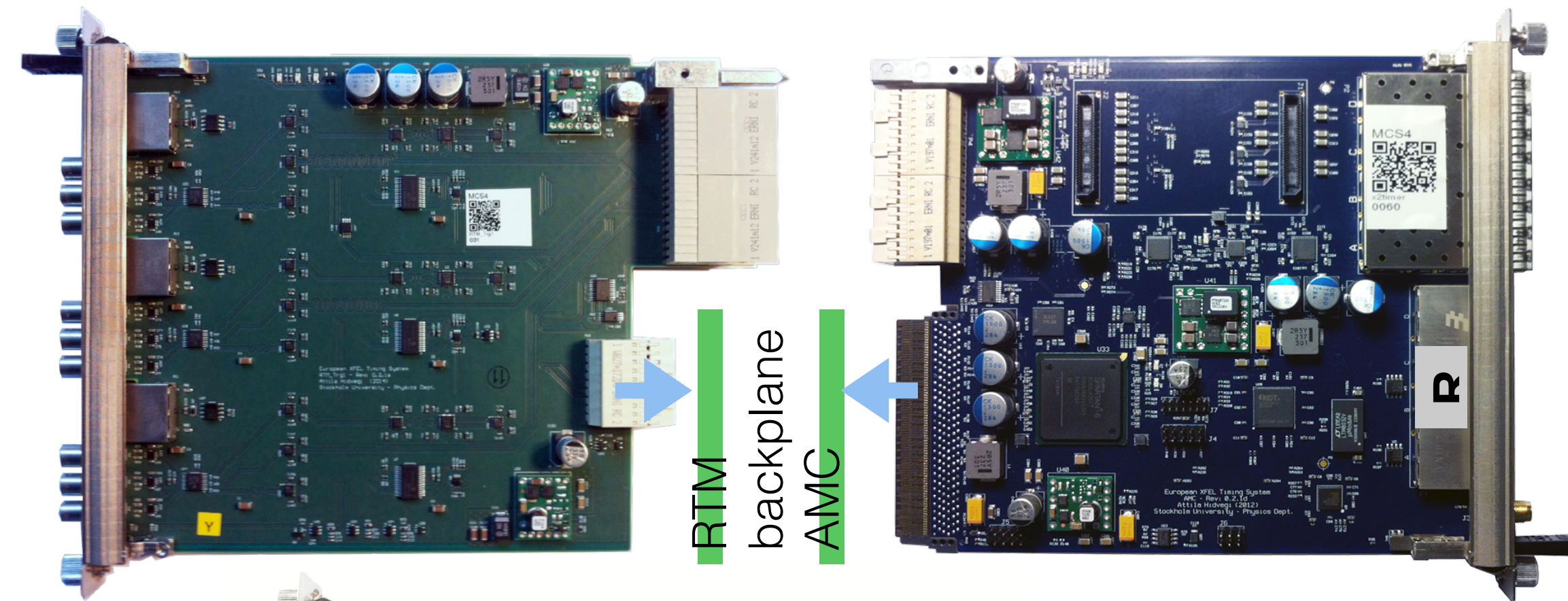
Clocks: TCLKA and TCLKB
Triggers: 8 * M-LVDS



RTM Timing Extension Modules

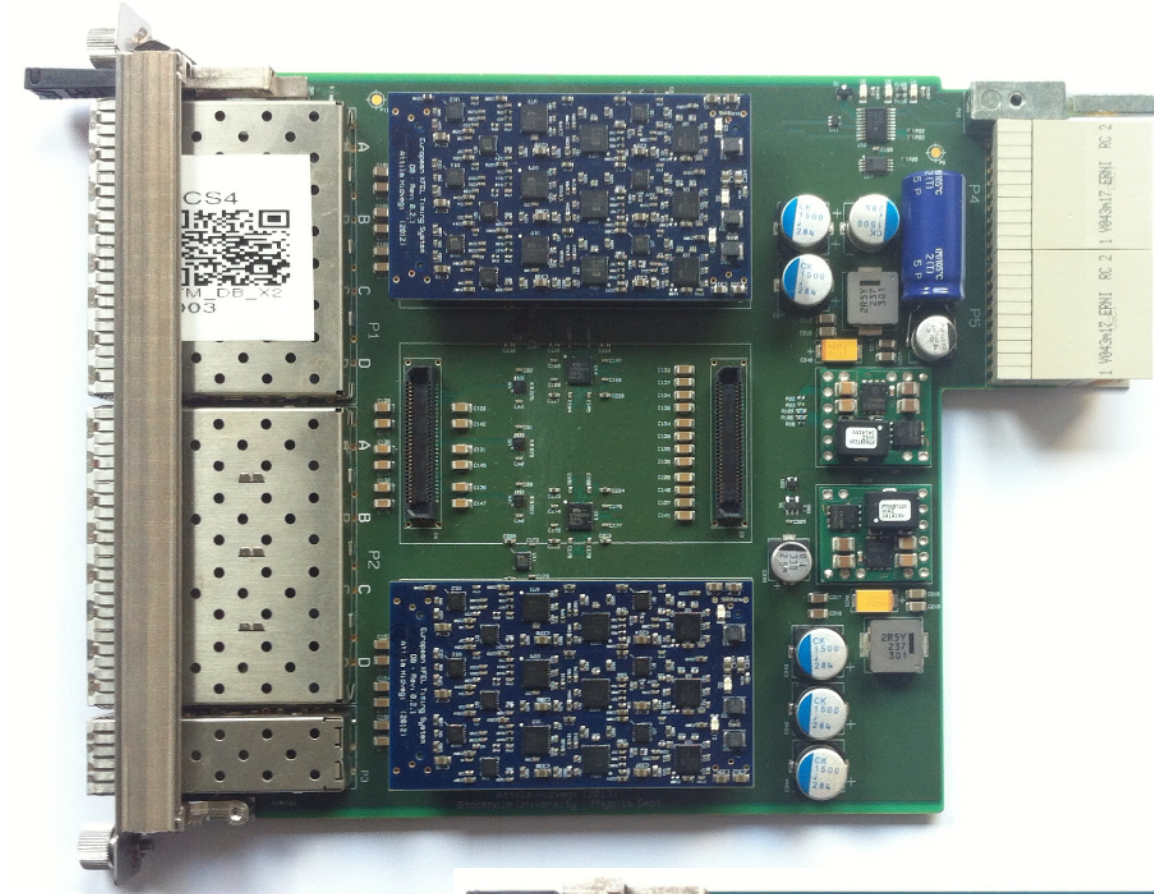
9 Lemo outputs (50 Ohm):

- Triggers, Clocks, Data
- 3 channels with 5ps resolution



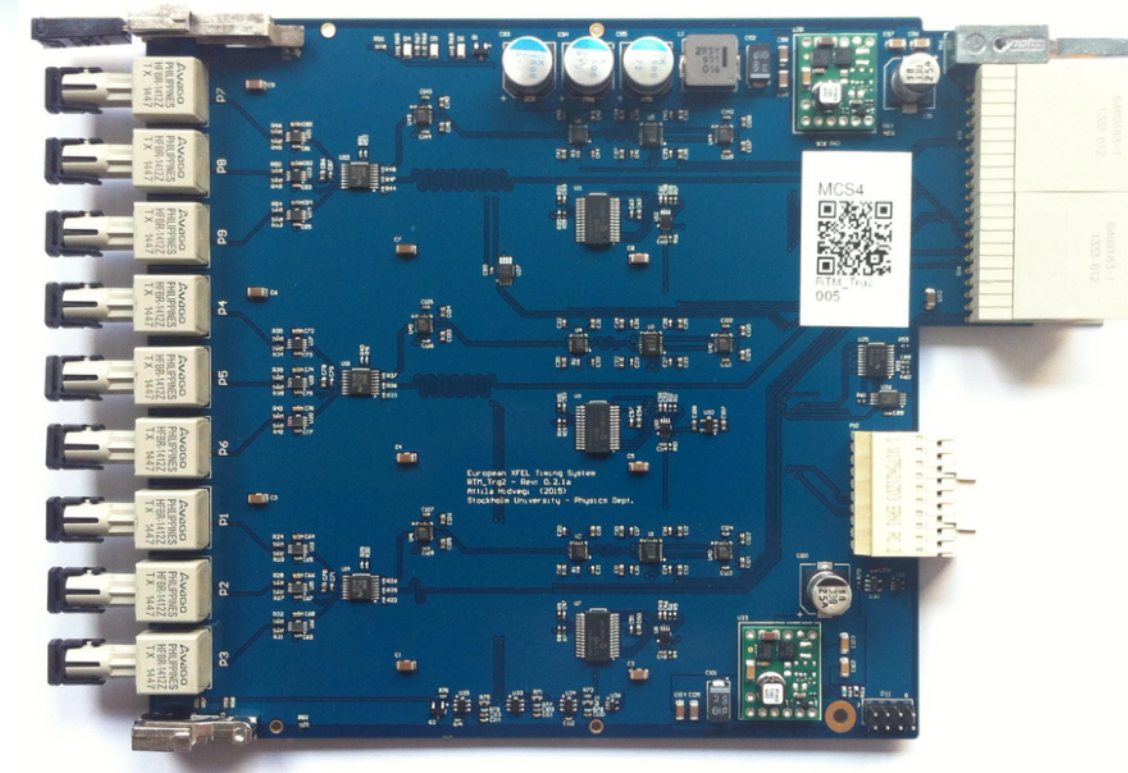
9 SFP outputs:

- length compensated fiber links

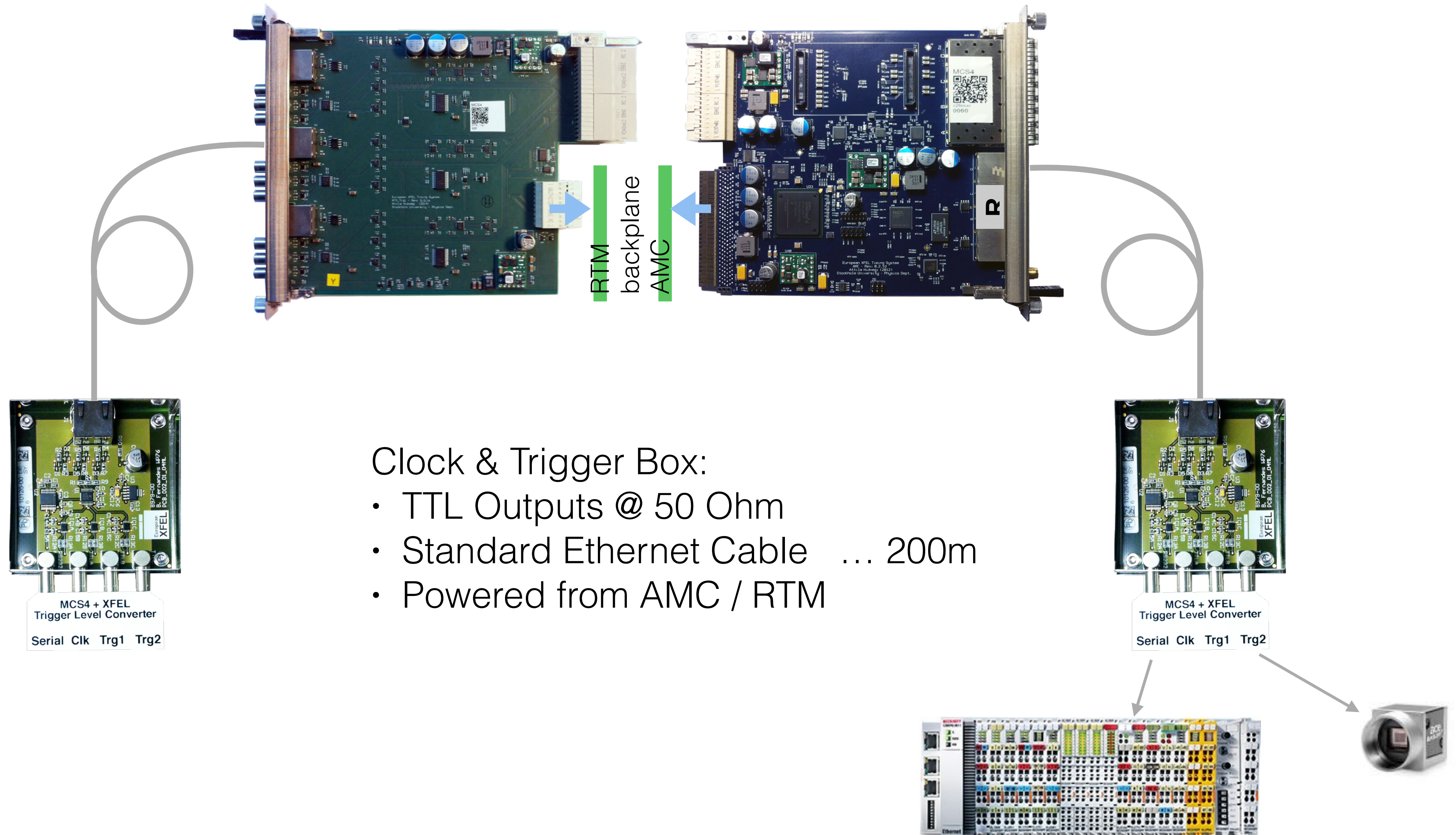


9 Fiber outputs (ST):

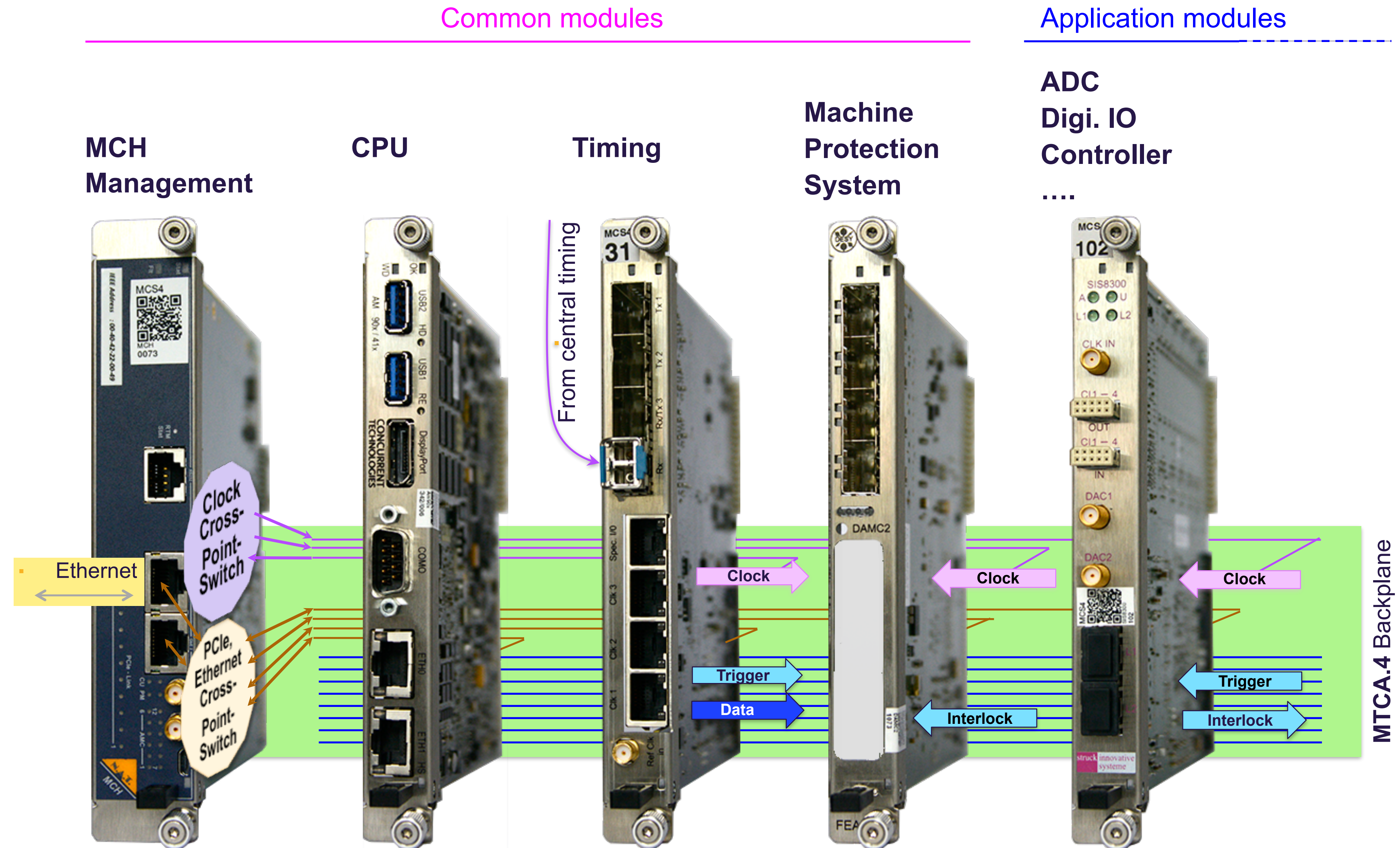
- Triggers, Clocks, Data
- used for modulators



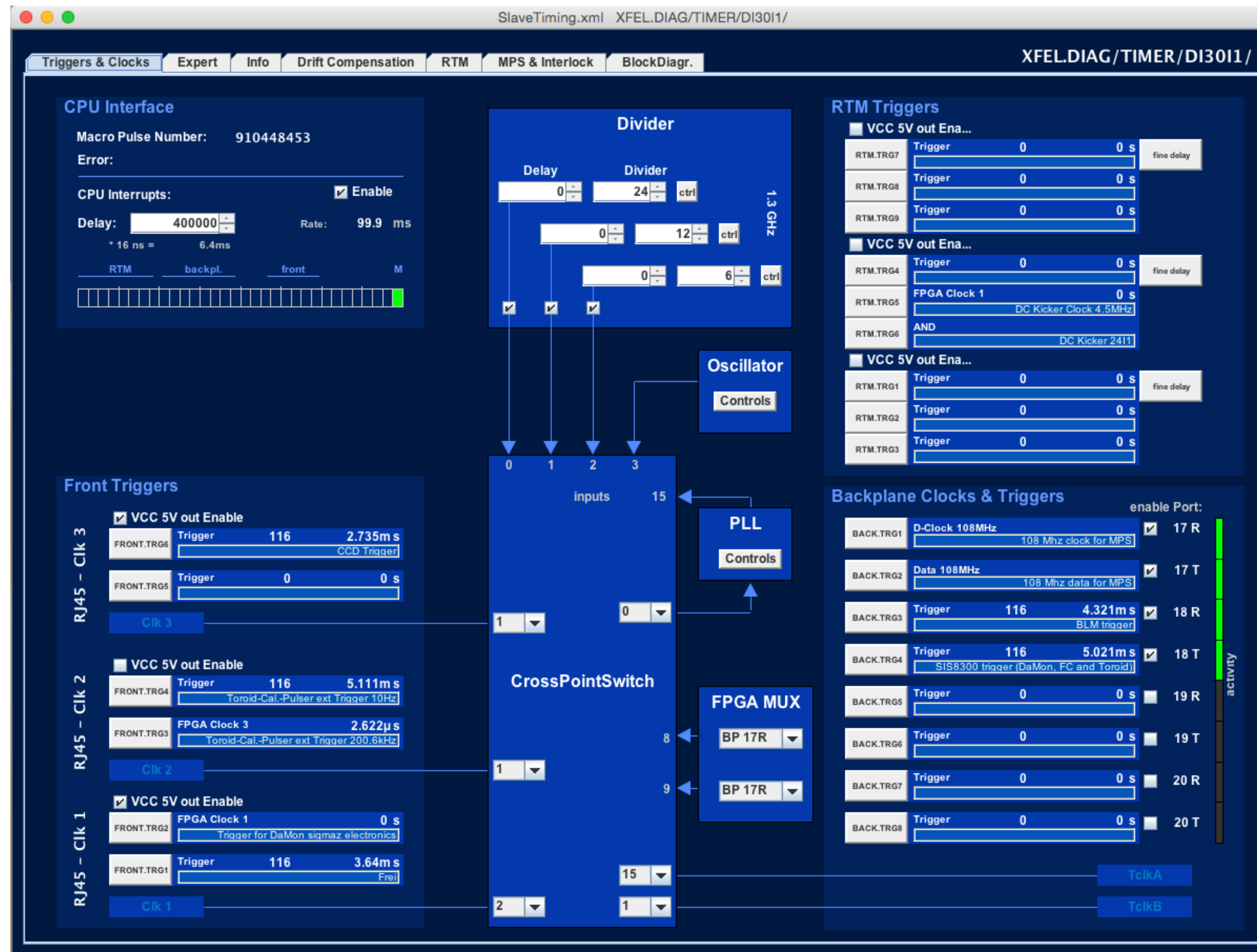
RTM Timing Extension Modules



Timing in a MicroTCA.4 Crate



Timing Main Controls - DOOCS Panel with jddd



Front
Outputs

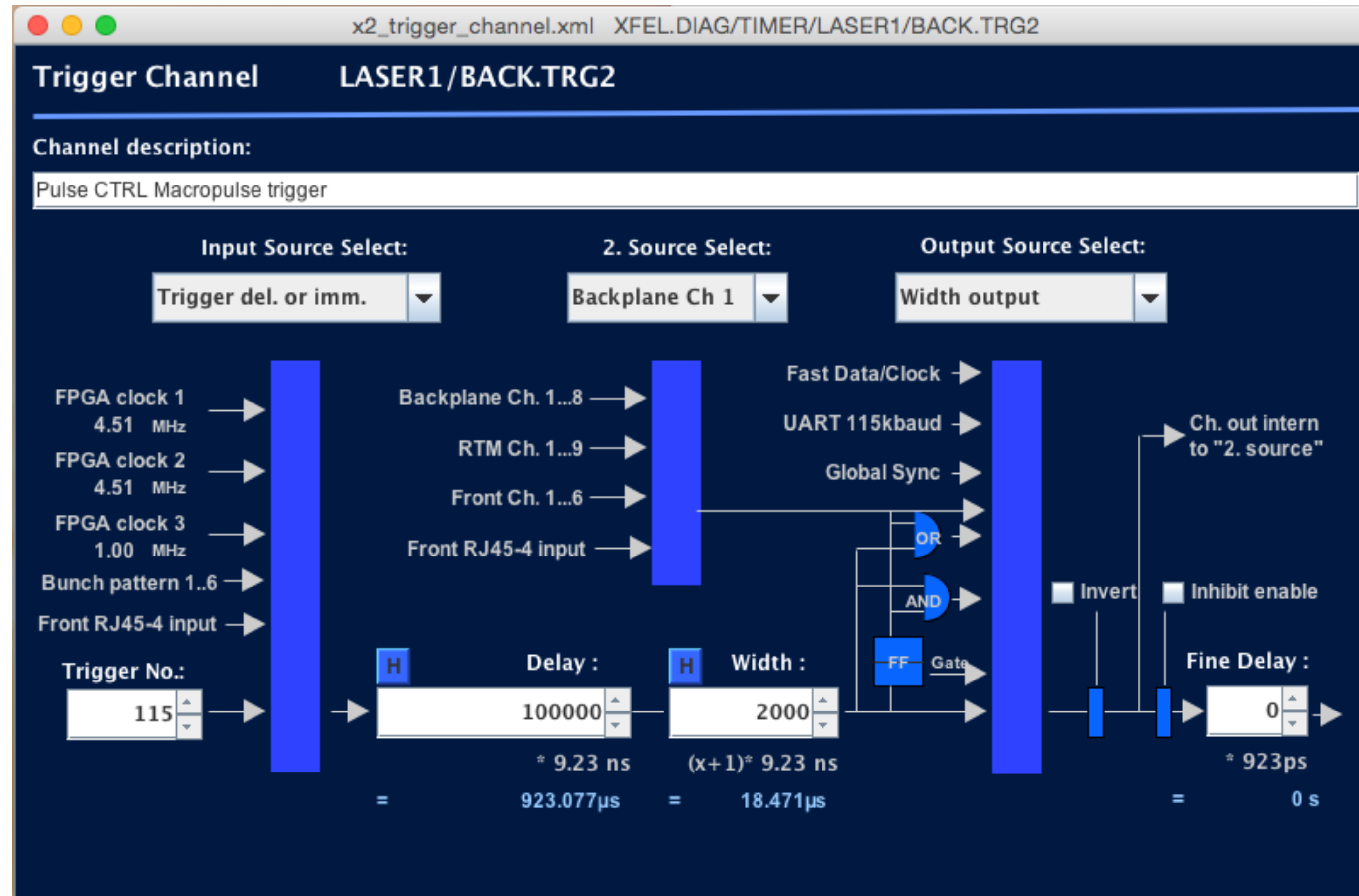
RTM
Outputs

23 Channels:
trigger/clock/data

5 Channels:
precision clocks

Backplane
Outputs

One Trigger/Clock/Data Channel Configuration out of 23



Selection of:

- Trigger # (0 ... 255)
- Bunch Pattern
- Clock from FPGA
- Front Input

Delay and Width:

- up to 150ms
- in 9.23ns steps

Combination w/ second channel:

- Gates (start
- Bursts of clocks
- Combine with 2nd channel

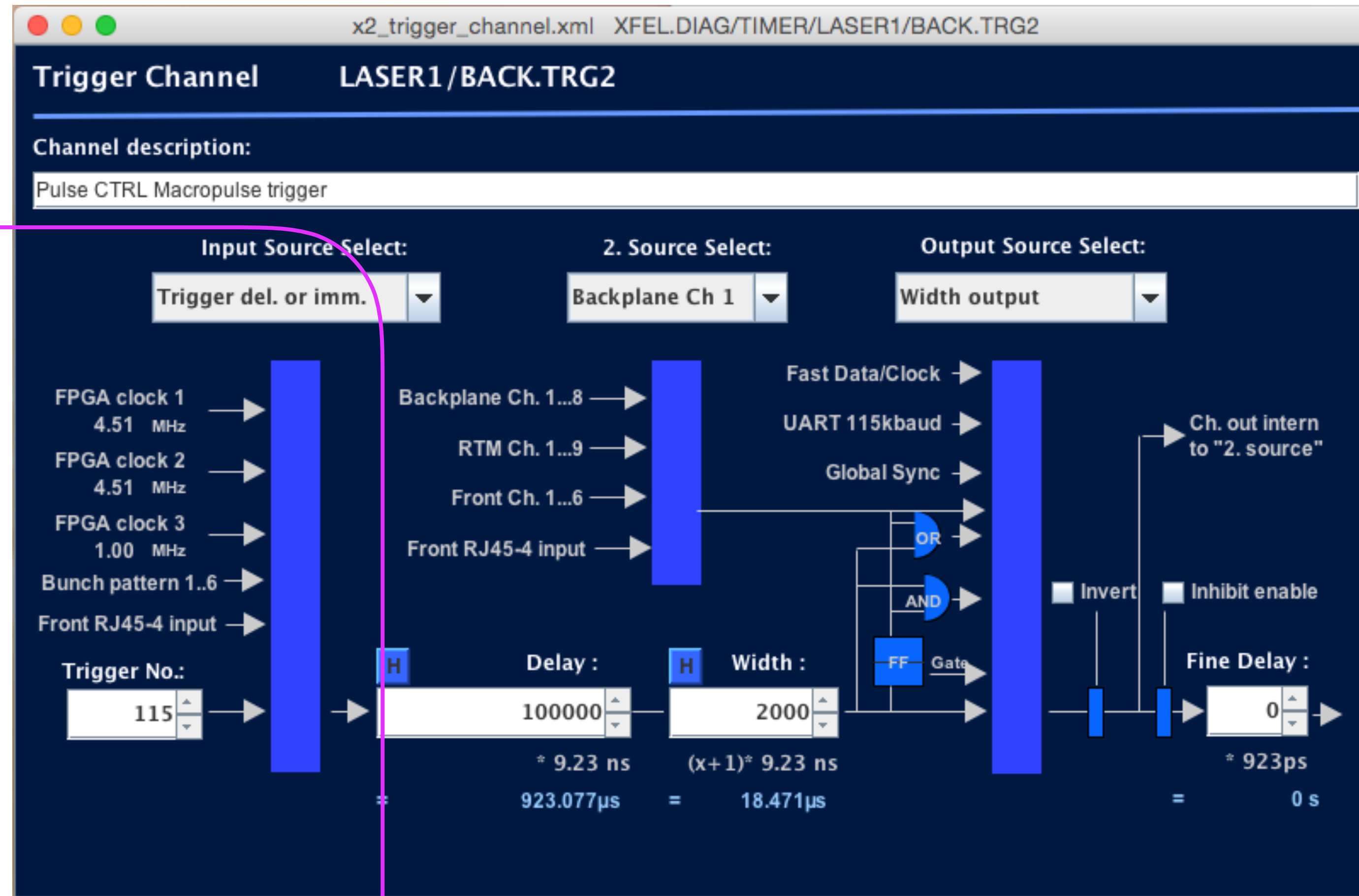
Select source:

- Single delayed & width
- Combination w/ 2nd Ch.: AND, OR, FlipFlop
- Serial data

Output can be:

- Inverted
- Inhibited
- Fine Delay: .92 ns steps

One Trigger/Clock/Data Channel Configuration out of 23



Selection of:

- **Trigger # (0 ... 255)**
- **Bunch Pattern**
- **Clock from FPGA**
- **Front Input**

Delay and Width:

- up to 150ms
- in 9.23ns steps

Combination w/ second channel:

- Gates (start
- Bursts of clocks
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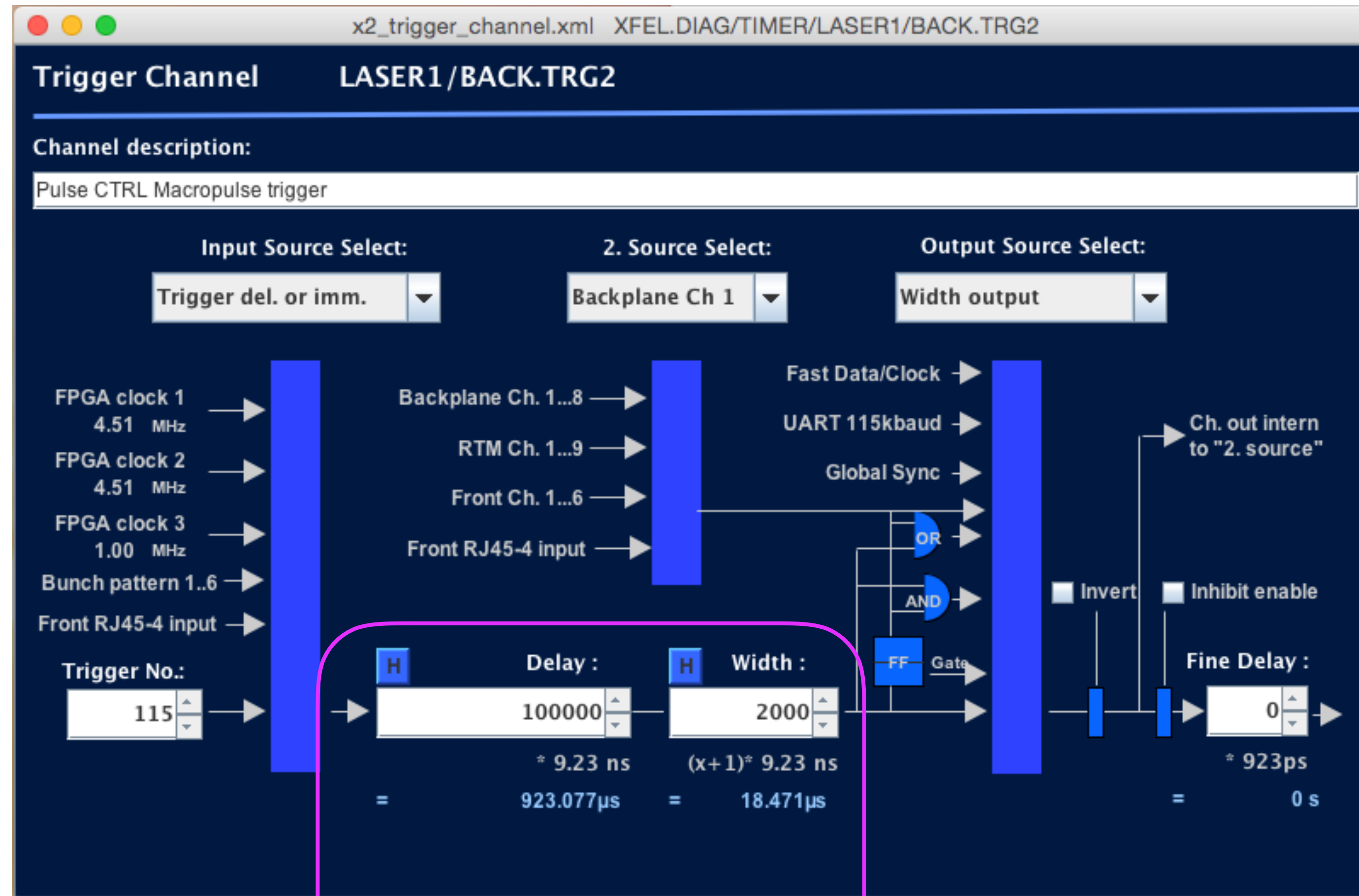
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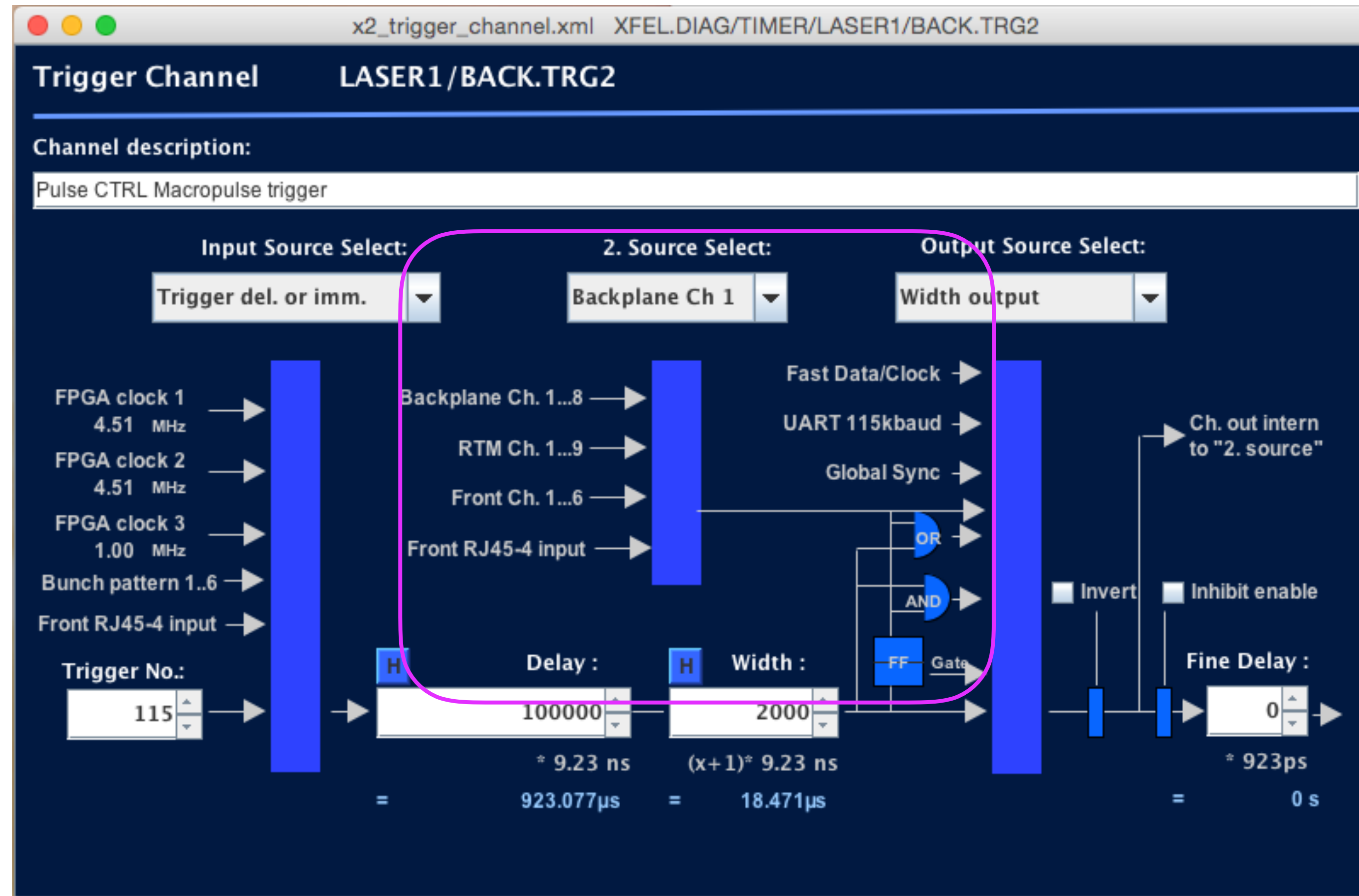
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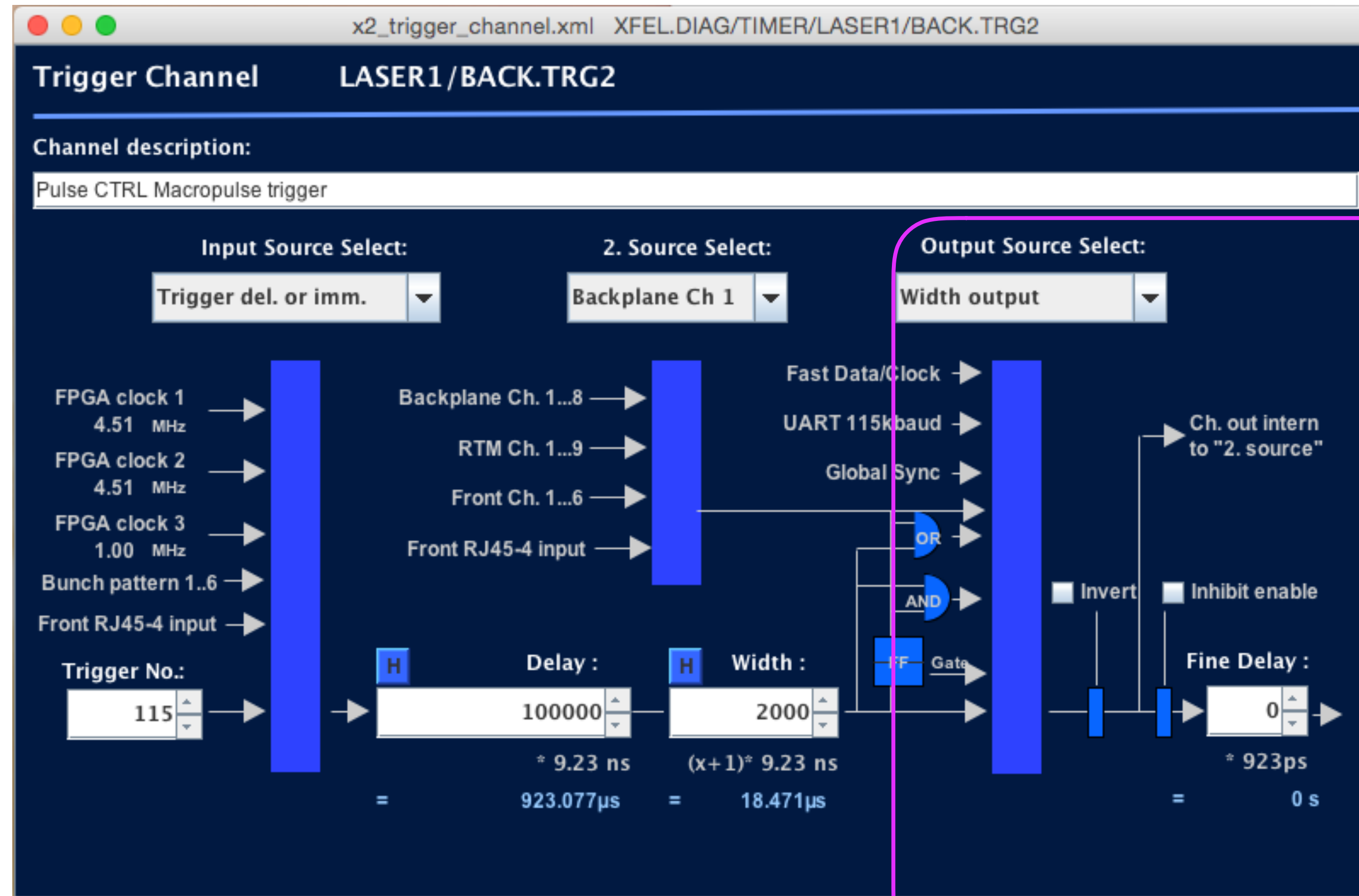
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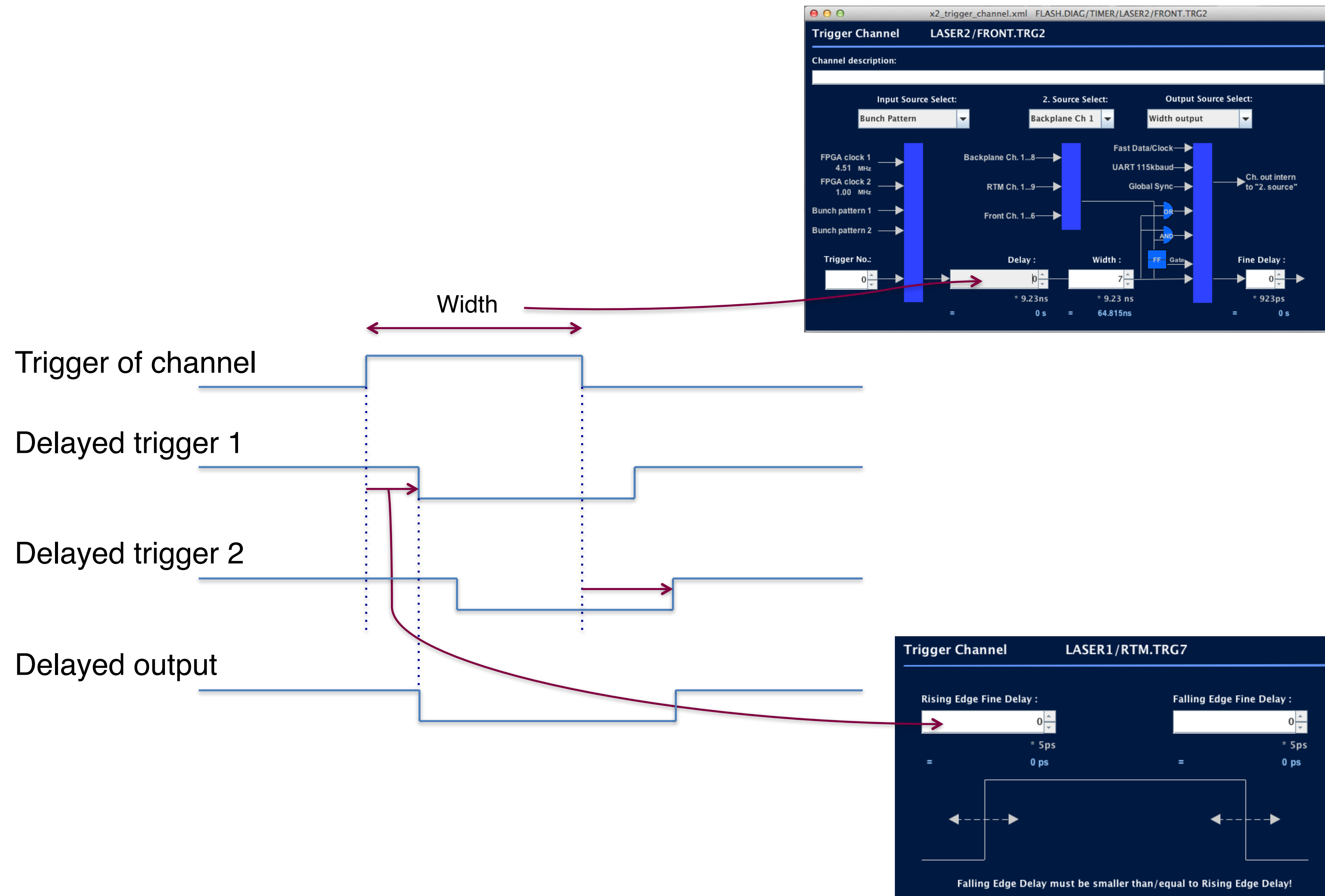
Select source:

- Single delayed & width
- Combination w/ 2nd Ch.: AND, OR, FlipFlop
- Serial data

Output can be:

- Inverted
- Inhibited
- Fine Delay: .92 ns steps

3 Channels with 5 ps resolution on RTM



Summary

- 10 ps RMS jitter and drift after 4 km
- Provides:
 - Triggers with delays and width (9.23 ns resolution, 24 bit)
 - 3 Channels with 5 ps resolution on optional RTM
 - Wide range phase stable clocks with and without FPGA
 - Distributes data words and tables w/ reliable delivery
 - Divider synchronization with main rep rate
 - 23 Outputs on: front, backplane, RTM, RTM backplane
 - Very flexible bunch generation and distribution
- User panels for complex functions
- Timing server has ~1900 DOOCS properties (incl. 160 archived channels)
- Designed by DESY & Stockholm Uni, Available from N.A.T: `NAMC_psTimer`