Digital and analog I/O solutions in MicroTCA.

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Workshop on beamline instrumentation for scientists and engineers; at DESY Hamburg

MicroTCA TECHNOLOGY LAB
A HELMHOLTZ INNOVATION LAB

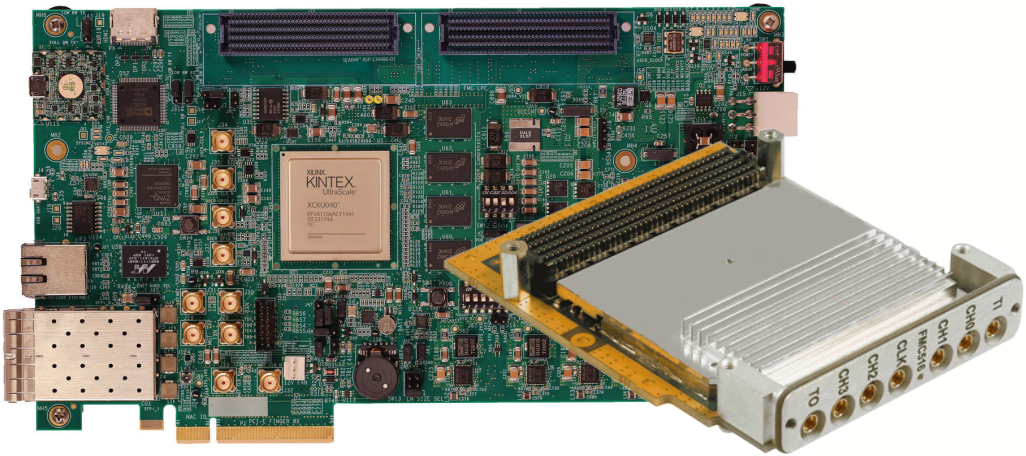
DESY

Outline

- Modular electronics - standards
- Hardware (FPGA, ADC and DAC, GPIO boards)
- FPGA firmware
- Software (Python library, CLI, Oscilloscope)
- Applications
- Custom developments

Standards

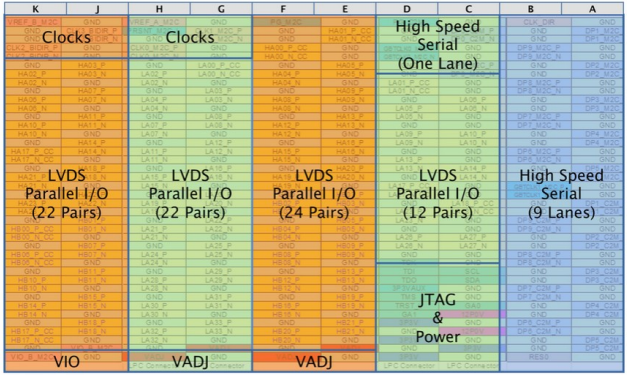
Standards involved: FMC



from https://www.samtec.com/standards/vita/fmc and
https://www.curtisswrightds.com/products/cots-boards/io-communication/analog-io/fmc-516.html

Standards involved: FMC

FMC standard is very-low level, requires custom logic in FPGA



from http://vita.mil-embedded.com/articles/creative-uses-fmc/

Standards involved: AMC

Basic building block of a MicroTCA system;
short form of the specification publicly available:
`https://www.picmg.org/openstandards/advanced-mezzanine-card/`

Bild 1: Das AMC-Modul-Interface zum Carrier

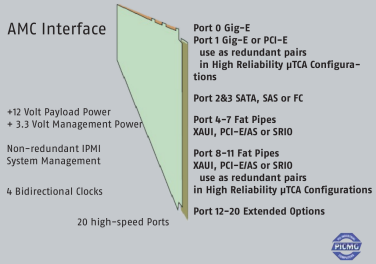


Tabelle 1: Verwendung der AMC-Ports

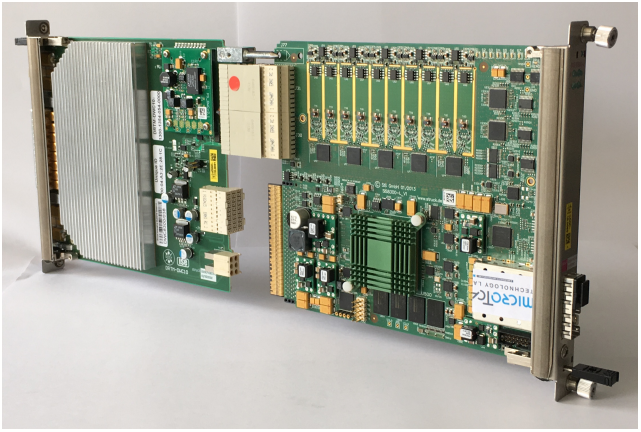
Connector Region		AMC Port#	AMC.1	AMC.2	AMC.4
Basic Side	Clocks	TCLKA			
		TCLKB			
		FCLKA			
	Common Options	0	GbE AMC.2 Typ E1 unassigned	or	GbE AMC.2 Typ E2
		1			GbE AMC.2 Typ E2
		2	AMC.3 SATA/SAS/FC		
		3	AMC.3 SATA/SAS/FC		
	Fat Pipe	4	Typ 1 Typ 2 Typ 4 Typ 8		Typ 6 10 GbE / AMC.4 x4 SRIO
		5			
		6			
		7			
Extended Side	Extended Fat Pipe	8	Typ 1 Typ 2 Typ 3 Typ 4 Typ 5		10 GbE / AMC.4 x4 SRIO
		9	GbE GbE GbE GbE		
		10	GbE GbE GbE		
		11	GbE		
	Extended Options	12-15	Ports 12 to 15 and 17 to 20 are reserved for rear I/O		
		TCLKC/D			
		17-20			

from `http://www.powerbridge.de/download/catalogues/2018-03%20MTCA%20Flyer%20Rev.%202.0.pdf`

Standards involved: RTM

Two main classes, analog and digital; more on
`https://techlab.desy.de/support/zone_3_recommendation`.

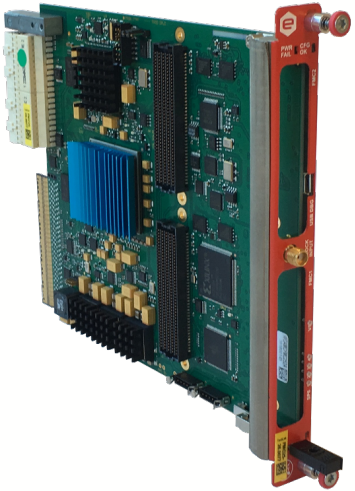
Digital variant electrically similar to FMC, different mechanical form factor.

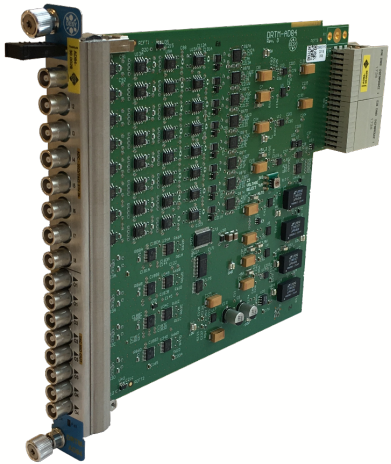


Hardware

DAMC-FMC25

- Double width, mid-size AMC
- RTM Class D1.1 support
- 2x FMC: ANSI/VITA 57.1 HPC
- Spartan-6 FPGA
- Virtex-5 data-processing FPGA





DRTM-AD84

- Double width MicroTCA.4, rear-transition module (RTM)
- Class D1.0 compatible
- 8 ch ADC, 16-bit, 10 MSPS, $\pm$1V
- 4 ch DAC, 16-bit, 1 MSPS, $\pm$1V and $\pm$3V output
- SW-switchable 50ohm on input
- SW-switchable antialiasing filter
- revD available, revE (with various improvements) before production

DFMC-UNI-IO

- LPC FMC mezzanine (VITA 57.1)
- Up to 48 digital I/O pins
- SW-selectable 3.3V or 5V levels
- Alternate functions available:
  - two 12-Bit DAC (0-5V, 50 mA drive)
  - two 12-Bit ADC (0-5V, 250 kSPS)
  - two power channels (9 V, 1A each)
  - standard RS232 ($\pm$ 12V levels)

DFMC-AD16

- LPC FMC mezzanine (VITA 57.1)
- 16 ADC channels with 18 bits
- Sample Rate: upto 200 kSPS
- Input over shielded RJ45 conn.
- Converter: AD7608 or AD7609
- Input Impedance: 1 MOhm
- Input Voltage: ± 5 V or ± 10 V

Firmware and Software

Firmware support

For each of the boards mentioned before there is a Board-Support Package (BSP) in our (MSK) repository. This allows easy creation of custom applications.

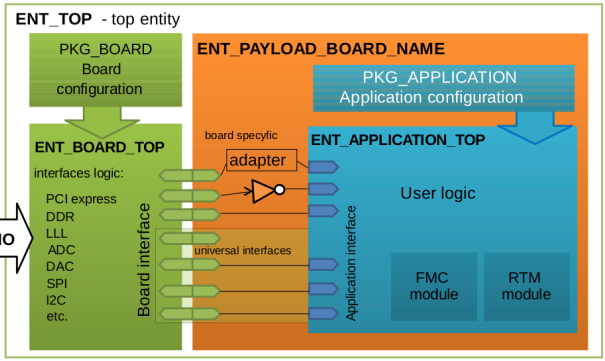
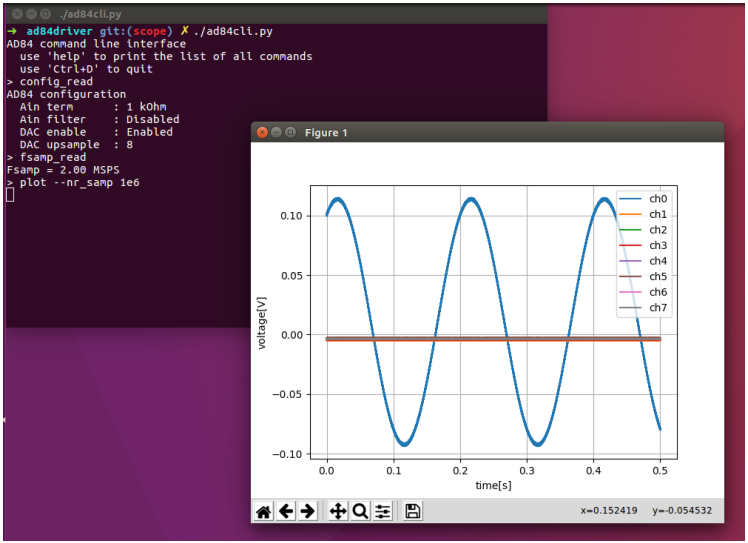


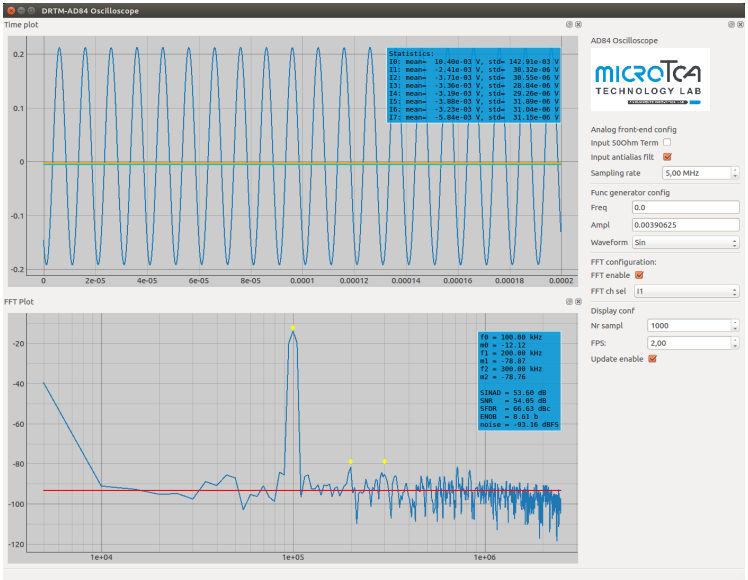
Figure 2: VHDL code block structure

from `http://icalepcs.synchrotron.org.au/papers/wepgf074.pdf` and
`https://accelconf.web.cern.ch/AccelConf/ICALEPCS2015/posters/wepgf074_poster.pdf`

Software: AD84 CLI



Software: AD84 Oscilloscope



AD84 ”package” contains:

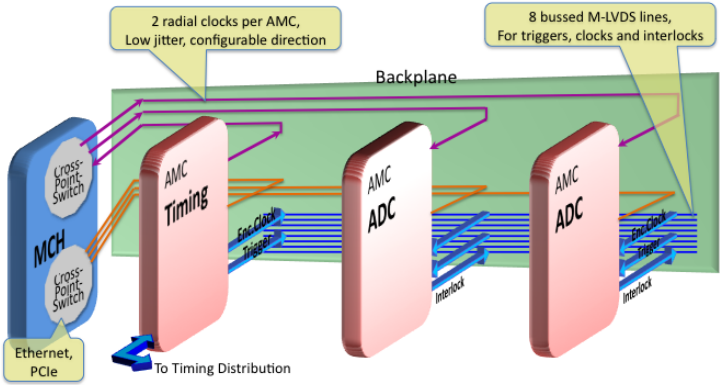
- Hardware: DRTM-AD84 and DAMC-FMC25 with data-acquisition firmware
- Linux drivers (supports Ubuntu 14.04 LTS and 16.04 LTS)
- Python library
- Command-line interface
- GUI Oscilloscope

DEMO:
command-line interface & oscilloscope

Application example

Application: board synchronization

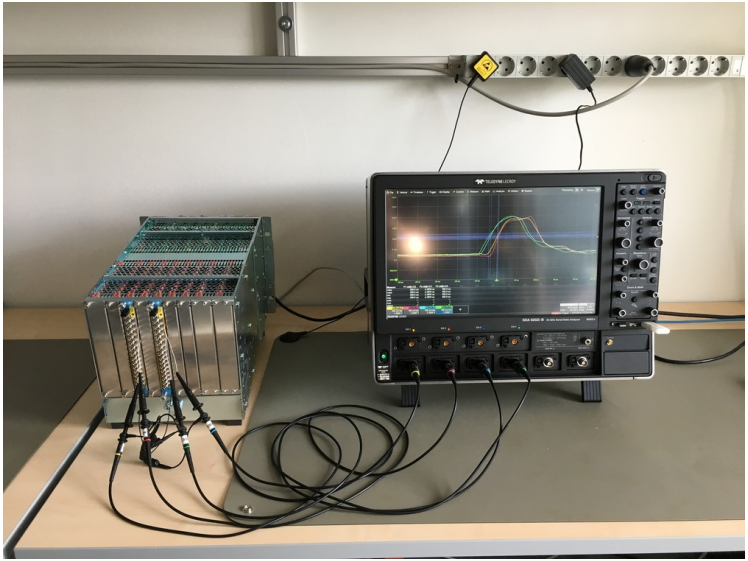
MicroTCA crate provides clocks connections (called TCLKA and TCLKB) to each slot.
One part of the MCH (MicroTCA Carrier Hub) acts as a cross-point switch for the clocks.



from `http://tesla.desy.de/doocs/MTCA/MTCA.4.html`

Application: board synchronization

Clock skew (TCLKA) measurement setup



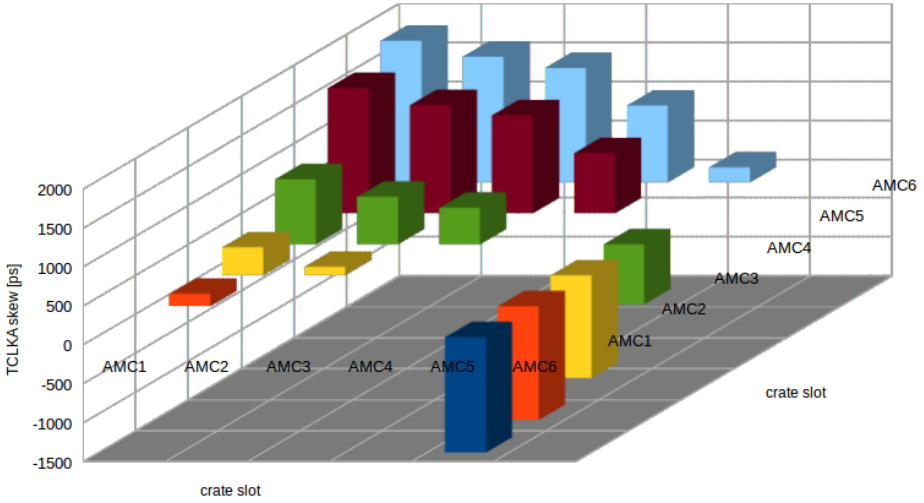
Application: board synchronization

Measurements of clock (TCLKA) skew (in ps) between different slots in MTCA crate:

from\to	AMC1	AMC2	AMC3	AMC4	AMC5	AMC6
AMC1		159	361	837	1610	1819
AMC2			107	612	1386	1615
AMC3				470	1256	1468
AMC4					773	985
AMC5	-1478	-1461	-1318	-769		193
AMC6						

Application: board synchronization

Graphical representation of the skew measurements:

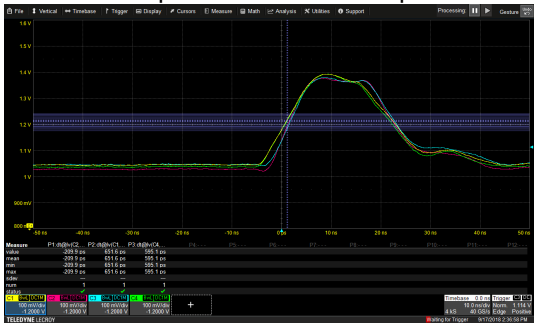


Application: board synchronization

Clock skew can be removed on AMC board in FPGA with built-in PLL (Phase-Locked Loop) or DCM (Digital Clock Manager)

before - clock phase not corrected

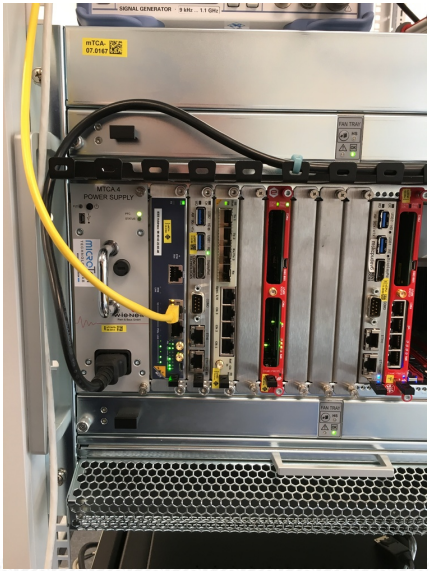
after - clock phase tuned to the specific slot



Custom developments

Custom developments: example

We started with our standard infrastructure:

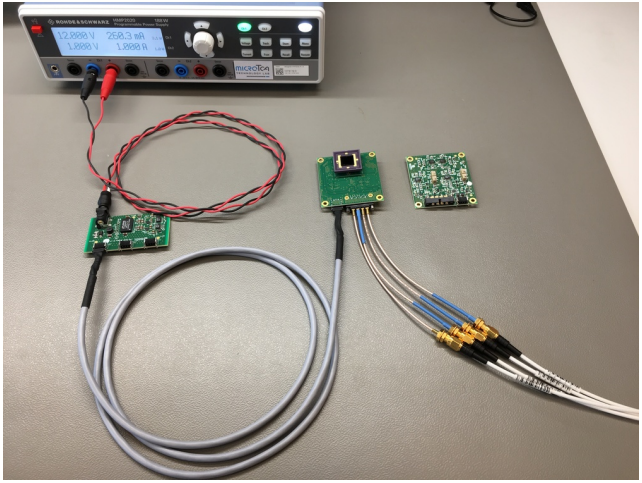


Custom developments: example

DRTM-AD84 as a general purpose analog input board:

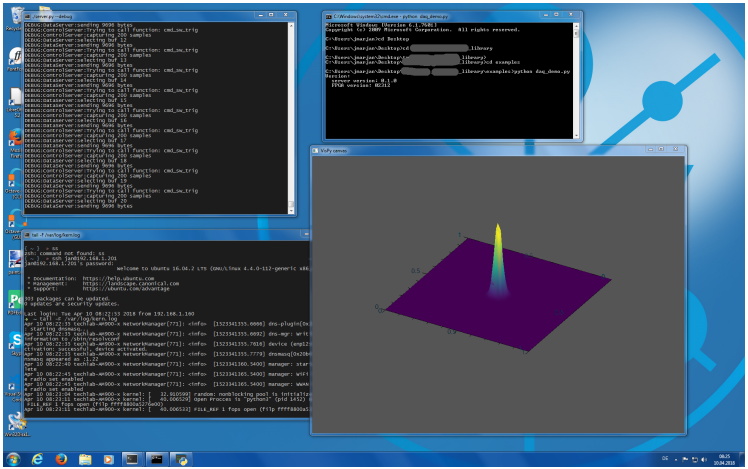
Custom developments: example

Some external electronics was developed specifically for the application:



Custom developments: example

User's software interfaces with our server running on in-crate CPU, and we have also developed some demo applications:



Thank you for you attention!